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SEVENTH EDITION
Transistor manual
CIRCUITS
APPLICATIONS
CHARACTERISTICS
THEORY

Transistor manual

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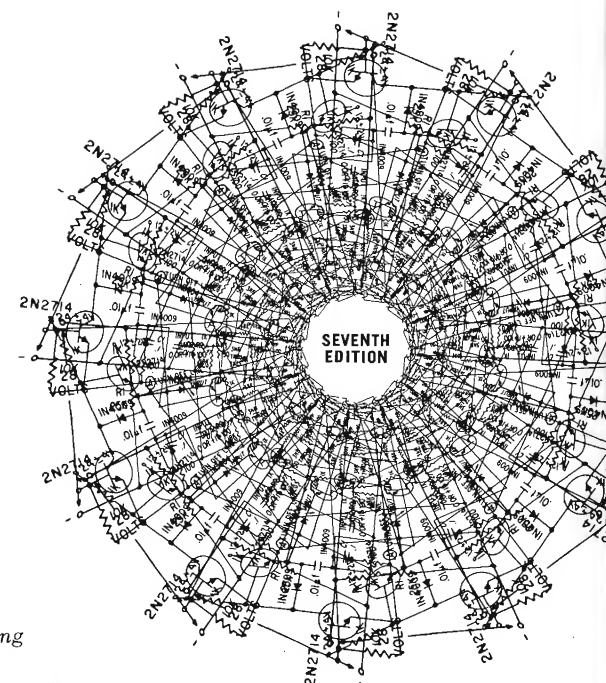
The circuit diagrams included in this manual are for illustration of typical transistor applications and *are not intended as constructional information.* For this reason, wattage ratings of resistors and voltage ratings of capacitors are not necessarily given. Similarly, shielding techniques and alignment methods which may be necessary in some circuit layouts are not indicated. Although reasonable care has been taken in their preparation to insure their technical correctness, no responsibility is assumed by the General Electric Company for any consequences of their use.

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FOREWORD

The growth to maturity of the semiconductor industry is paralleled by the growth of this General Electric Transistor Manual. First published in 1957, the present Manual's more than 600 pages is roughly 10 times the size of the first edition. The contents, however, retain the same basic orientation which is that of a highly practical circuit book, one that can be used to advantage by electronic design engineers as well as students, teachers, and experimenters.

This seventh edition contains new and updated material which accounts for more than 80% of the contents. For instance: more high frequency material has been added; the chapter on switching has been completely rewritten; the number of circuits in the manual has been almost tripled; also, the chapter for experimenters has been greatly enlarged.

This is a book written not by theorists, but by experienced men who are devising the practical solutions to some of the most challenging, difficult problems encountered in electronic engineering.

As solid state devices contribute more and more to the wonderful age of automated industry and electronic living, we at General Electric sincerely hope that this Manual will provide insight and understanding on how semiconductors might do the job better and more economically.

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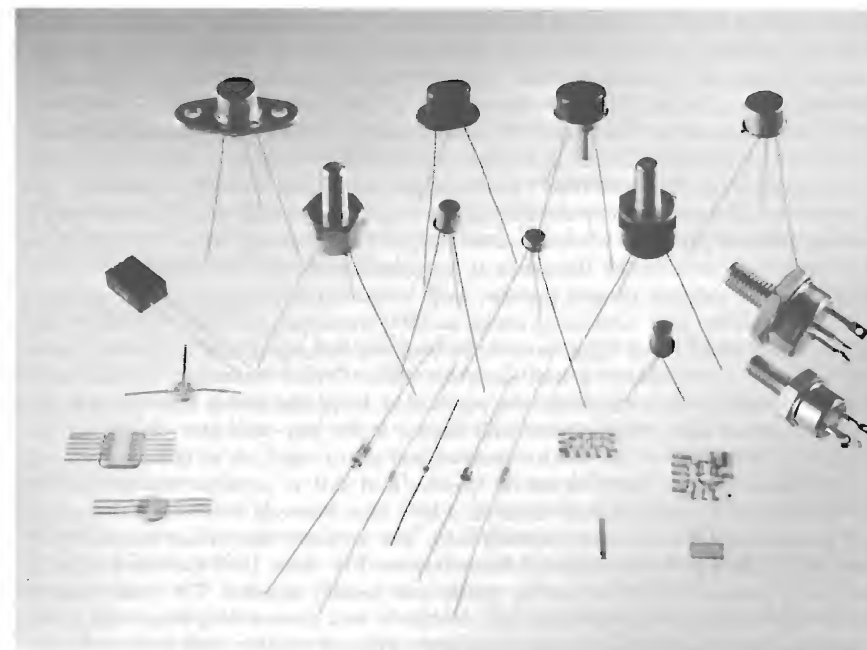
BASIC SEMICONDUCTOR THEORY

CHAPTER 1

A FEW WORDS OF INTRODUCTION

Pushing the frontiers of space outward along the "space spectrum" toward both infinities has caused to be born in this century whole new technologies. Those related to outer space, and those related to "inner space." But not one stands alone, independent of another. All are related. It is this relationship, accumulating as it has down through the ages that has brought with it the *transistor*.

Just as the vast reaches of outer space — that infinite "land" of the sun and moon, the star constellations and the "milky way," Mars, Venus, and all of the other mysteries that exist there — has caused man throughout his history to wonder and ask questions, so too has he wondered and asked about the vast reaches of "inner space" — the world of the atom. But it has only been recently, during the 19th and 20th centuries in fact, that some of his questions about inner space have been answered. Much to his credit, many questions man has answered by mere observation and mathematical calculation. Further to his credit he has devised "seeing eye" aids to help push the space boundaries still farther out.

GENERAL ELECTRIC DEVICES

Problems of "seeing" exist at both ends of space, and it is just as difficult to look "in" as it is to look "out." Just as the outer space astronomer depends on his powerful

magnifying aids to help him see, hear, and to measure, to gather information and data in order to comprehend; so too does the inner space "astronomer" depend on his magnifying aids. Microscopes, mass spectrometers, x-ray and radiography techniques, electric meters, oscilloscopes, and numerous other intricate equipment help him to measure the stuff, the matter, that makes up inner space. From his search has developed many new technical terms. In fact, whole new technical languages have come into existence: electron, hole, neutron, neutrino, positron, photon, muon, kaon, the Bohr atom, quantum mechanics, Fermi-Dirac statistics. Strange terms to many, but terms of the world that exist at one end of the infinite space spectrum, the atomic world.

Atomic physics as we know it today started far back in 400 B.C.[1] when the doctrine of atoms was in vogue in the Greek world of science. And no matter how unsophisticated the atomic theories at the time, it *was* a beginning. The idea of "spirit" particles too small for the unaided human eye to see was then postulated. It would take many centuries before the knowledge of the physicist, the statistician, the metallurgist, the chemist, the engineer — both mechanical and electronic — could and would combine to bring into being a minute, micro-sized crystal that would cause to evolve a completely new and unusually complicated industry, the semiconductor industry.

The history of the *semiconductor* is, in fact, a pyramid of learning, and if any one example were to be cited, of the practical fruits of scientific and technical cooperation over the ages, and especially over the past 100 or so years, near the head of the list would surely be the *transistor*.

In 1833, Michael Faraday,[2] the famed English scientist, made what is perhaps the first significant contribution to semiconductor research. During an experiment with silver sulphide Faraday observed that its resistance varied inversely with temperature. This was in sharp contrast with other conductors where an increase in temperature caused an increase in resistance and, conversely, a decrease in temperature caused a decrease in resistance. Faraday's observation of negative temperature coefficient of resistance, occurring as it did over 100 years before the birth of the practical transistor, may well have been the "gleam in the eye" of the future.

For since its invention in 1948[3] the transistor has played a steadily increasing part not only in the electronics industry, but in the lives of the people as well. First used in hearing aids and portable radios, it is now used in every existing branch of electronics. Transistors are used by the thousands in automatic telephone exchanges, computors, industrial and military control systems, and telemetering transmitters for satellites. A modern satellite may contain as many as 2500 transistors and 3500 diodes as part of a complex control and signal system. In contrast, but equally as impressive, is the two transistor "pacemaker," a tiny electronic pulser. When imbedded in the human chest and connected to the heart the pacemaker helps the ailing heart patient live a nearly normal life. What a wonderful device is the tiny transistor. In only a few short years it has proved its worth — from crystal set to regulator of the human heart.

But it is said that progress moves slowly. And this is perhaps true of the first hundred years of semiconductor research, where time intervals between pure research and practical application were curiously long. But certainly this cannot be said of the years that followed the invention of the transistor. For since 1948 the curve of semiconductor progress has been moving swiftly and steadily upward. The years to come promise an even more spectacular rise. Not only will present frequency and power limitations be surpassed but, in time, new knowledge of existing semiconductor materials . . . new knowledge of *new* materials . . . improved methods of device fabrication . . . the micro-miniaturization of semiconductor devices . . . complete micro-circuits . . . all, will spread forth from the research and engineering laboratories to further influence and improve our lives.

Already, such devices as the tunnel diode and the high-speed diode can perform

with ease well into the UHF range; transistors, that only a short time ago were limited to producing but a few milliwatts of power, can today produce thousands upon thousands of milliwatts of power; special transistors and diodes such as the unijunction transistor, the high-speed diode, and the tunnel diode can simplify and make more economical normally complex and expensive timing and switching circuits. Intricate and sophisticated circuitry that normally would require excessive space, elaborate cooling equipment, and expensive power supply components can today be designed and built to operate inherently cooler within a substantially smaller space, and with less imposing power components. All this is possible by designing with semiconductors. In almost all areas of electronics the semiconductors have brought immense increases in efficiency, reliability, and economy.

Although a complete understanding of the physical concepts and operational theory of the transistor and diode are not necessary to design and construct transistor circuits, it goes without saying that the more *device knowledge* the designer possesses, whether he be a professional electronics engineer, a radio amateur, or a serious experimenter, the more successful will he be in his use of semiconductor devices in circuit design. Such understanding will help him to solve special circuit problems, will help him to better understand and use the newer semiconductor devices as they become available, and surely will help clarify much of the technical literature that more and more abounds with semiconductor terminology.

The forepart of this chapter, then, is concerned with semiconductor terminology and theory as both pertain to diodes and junction transistors. The variety of semiconductor devices available preclude a complete and exhaustive treatment of theory and characteristics for all types. The silicon controlled rectifier (SCR) is well covered in other General Electric Manuals;[4,5] treatment of the unijunction transistor (UJT) will be found in Chapter 13 of this manual, and tunnel diode circuits are shown in Chapter 14.[6] Other pertinent literature will be found at the end of most chapters under *references*. Information pertaining to other devices and their application will be found by a search of text books and their accompanying bibliographies. The "year-end index" (December issue) of popular semiconductor and electronic periodicals is another excellent source. Public libraries, book publishers, magazine publishers, and component and device manufacturers are all "information banks" and should be freely used in any search for information and knowledge.

SEMICONDUCTORS

Semiconductor technology is usually referred to as *solid-state*. This suggests, of course, that the *matter* used in the fabrication of the various devices is a solid, as opposed to liquid or gaseous matter — or even the near perfect vacuum as found in the thermionic tube — and that conduction of electricity occurs within solid material. "But how," it might be asked, "can electrical charges move through solid material as they must, if electrical *conduction* is to take place?" With some thought the answer becomes obvious: the so-called solid is *not* solid, but only partially so. In the microcosmos, the world of the atom, there is mostly space.[7] It is from close study of this intricate and complicated "little world," made up mostly of space, that scientists have uncovered the basic ingredients that make up solid state devices — the *semiconductors*.

Transistors and diodes, as we know them today, are made from semiconductors, so-called because they lie between the metals and the insulators in their ability to conduct electricity. A simple illustration of their general location is shown in Figure 1.1. Shaded areas are transition regions. Materials located in these areas may or may not be semiconductors, depending on their chemical nature.

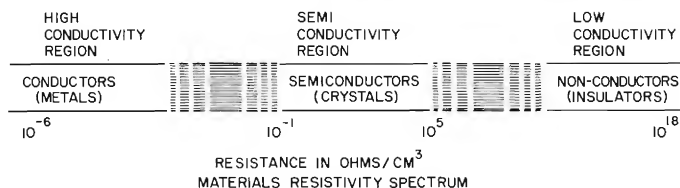
There are many semiconductors, but none quite as popular at the present time as germanium and silicon, both of which are hard, brittle crystals by nature. In their

SEMICONDUCTORS ARE LOCATED IN REGION BETWEEN CONDUCTORS AND INSULATORS

Figure 1.1

natural state they are impure in contrast, for example, to the nearly pure crystalline structure of high quality diamond. In terms of electrical resistance the relationship of each to well known conductors and insulators is shown in Table 1.1.

MATERIAL	RESISTANCE IN OHMS PER CENTIMETER CUBE (R/CM^3)	CATEGORY
Silver Aluminum	10^{-6} 10^{-5}	Conductor
Pure Germanium Pure Silicon	50-60 50,000-60,000	Semiconductor
Mica Polyethlene	10^{12}-10^{13} 10^{15}-10^{16}	Insulator

Table 1.1

Because of impurities, the R/CM^3 for each in its natural state is much less than an ohm, depending on the degree of impurity present. Material for use in most practical transistors requires R/CM^3 values in the neighborhood of 2 ohms/CM^3. The ohmic value of pure germanium and silicon, as can be seen from Table 1, is much higher. *Electrical conduction, then, is quite dependent on the impurity content of the material,* and precise control of impurities is the most important requirement in the production of transistors. Another important requirement for almost all semiconductor devices is that *single crystal* material be used in their fabrication.

ATOMS

To better appreciate the construction of single crystals made from germanium and silicon, some attention must be first given to the makeup of their individual atoms. Figure 1.2(A) and (C) show both as represented by Bohr models of atomic structure, so named after the Danish physicist Neils Bohr (1885-1962).

Germanium is shown to possess a positively charged nucleus of +32 while the silicon atom's nucleus possesses a positive charge of +14. In each case the total positive charge of the nucleus is equalized by the total effective negative charge of the electrons. This equalization of charges results in the atom possessing an effective charge that is neither positive nor negative, but neutral. The electrons, traveling within their respective orbits, possess energy since they are a definite mass in motion.* Each electron in its relationship with its parent nucleus thus exhibits an energy value and

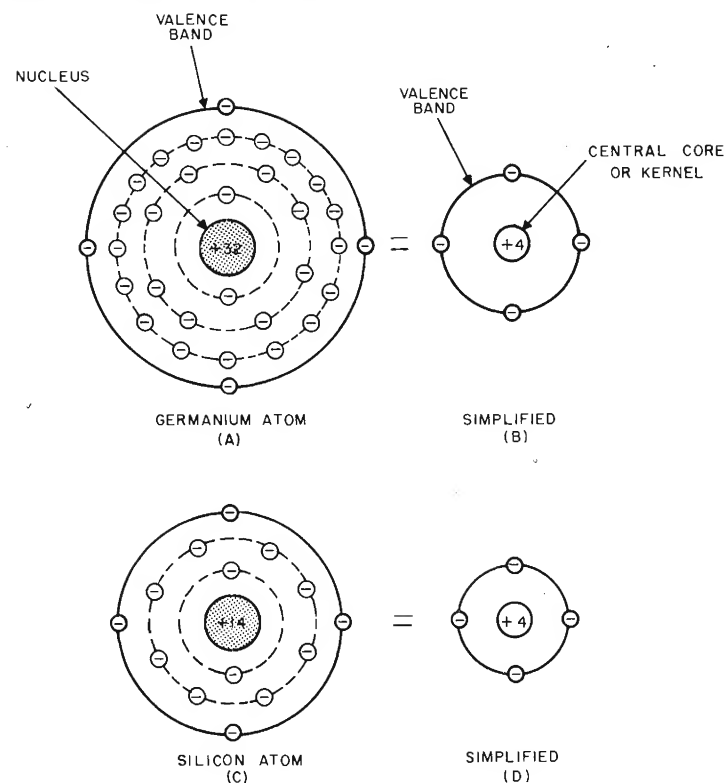
*Rest mass of electron = 9.108×10^{-28} gram.

BOHR MODELS OF GERMANIUM AND SILICON ATOMS

Figure 1.2

functions at a definite and distinct *energy level.* This energy level is dictated by the electron's momentum and its physical proximity to the nucleus. The closer the electron to the nucleus, the greater the holding influence of the nucleus on the electron and the greater the energy required for the electron to break loose and become free. Likewise, the further away the electron from the nucleus the less its influence on the electron.

Outer orbit electrons can therefore be said to be stronger than inner orbit electrons because of their ability to break loose from the parent atom. For this reason they are called *valence electrons,* from the Latin valere, to be strong. The weaker inner orbital electrons and the nucleus combine to make a *central core* or *kernel.* The outer orbit in which valence electrons exist is called the *valence band* or *valence shell.* It is the electrons from this band that are dealt with in the practical discussion of transistor physics.

With this in mind the complex atoms of germanium and silicon as shown in (A) and (C) of Figure 1.2 can be simplified to those models shown in (B) and (C) and used in further discussion. It should be mentioned that although it is rare for inner orbital electrons — those existing at energy levels below that of the valence band — to break loose and enter into transistor action, they can be made to do so if subjected to heavy x-rays, alpha particles, or nuclear bombardment and radiation.

When an electron is freed from the valence band and moves into "outer *atomic* space," it becomes a conduction electron, and exists in the *conduction band.* Electrons

possess the ability to move back and forth between valence and conduction bands.

VALENCY

The most important characteristic of most atoms is their ability to unite with other atoms. Such an atom is said to possess *valency*, or be a *valent atom*. This ability is dependent on those electrons that exist in the parent atom's valence band, leaving the band to move into the valence band of a neighboring atom. Orbits are thus enlarged to encompass two parent atoms rather than only one; the action is reciprocated in that electrons from the neighboring atom also take part in this mutual combining process.

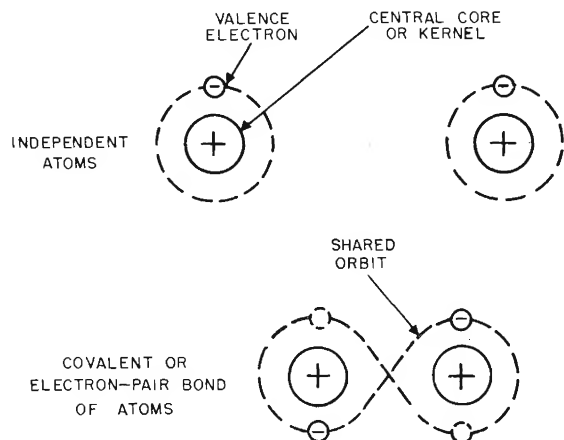



Figure 1.3

In short, through orbit sharing by interchange of orbital position, the electrons become mutually related to one another and to the parent cores, binding the two atoms together in a strong spaced locking action. A *covalent bond* (cooperative bond; working together) or *electron-pair bond* is said to exist. This simple concept when applied to germanium and silicon crystals will naturally result in a more involved action, one the reader may at first find difficult to visualize. This important and basic atomic action can be visualized as shown in Figure 1.3.

SINGLE CRYSTALS

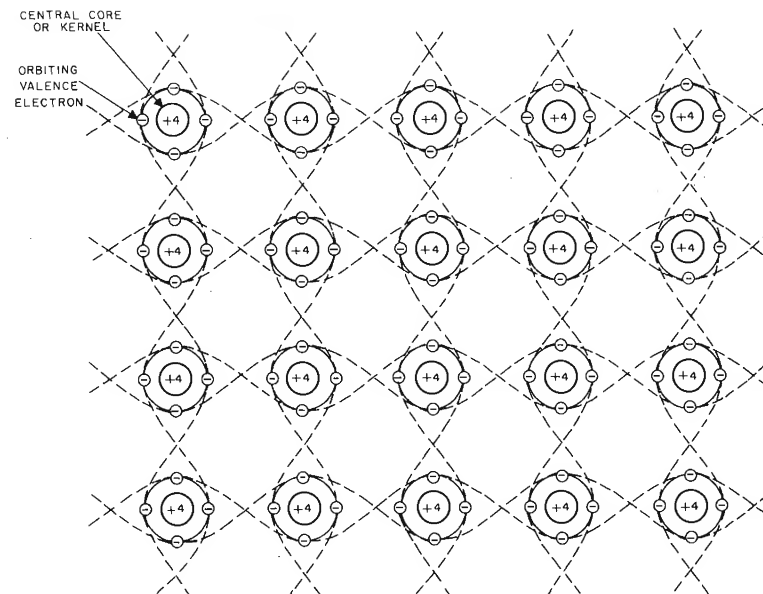
In the structure of pure germanium and pure silicon single crystals the molecules are in an ordered array. This orderly arrangement is descriptively referred to as a diamond lattice, since the atoms are in a lattice-like structure as found in high quality diamond crystals.[8] A definite and regular pattern exists among the atoms due to space equality. For equal space to exist between all atoms in such a structure, however, the following has been shown to be true: the greatest number of atoms that can neighbor any single atom at equal distance and still be equidistant from one another is *four*.[9] Figure 1.4 is a two dimensional presentation of a germanium lattice structure showing covalent bonding of atoms. (Better understanding and more clear *spatial visualization* – that is, putting oneself in a frame of mind to "mentally see" three dimensional figures, fixed or moving with time – of Figure 1.4 may be had by construction of a three dimensional diamond lattice model using the technique shown in Figure 1.5.

TWO DIMENSIONAL CRYSTAL LATTICE STRUCTURE

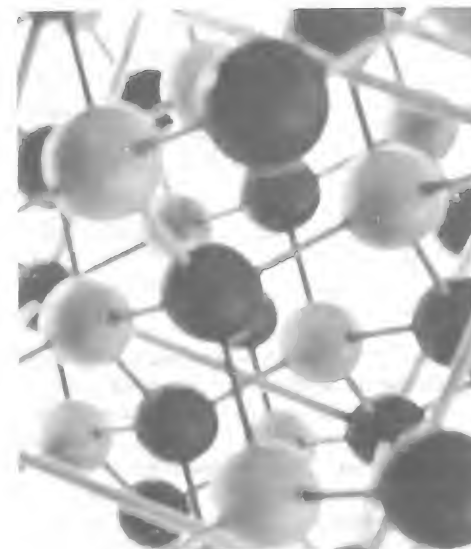
Figure 1.4

TYPICAL MODEL OF ATOMIC CRYSTAL LATTICE STRUCTURE
(TYPIFIES SPATIAL VISUALIZATION)

Figure 1.5

Spatial visualization differs in individuals, and where some will have little trouble forming a clear mental picture of complex theoretical concepts, others will have difficulties. Whether electrons and holes and atoms in all their involved movements are mentally pictured in terms of more graphic objects such as marbles, moth balls, baseballs, automobiles, or whatever else that might come to mind, is of little consequence and may even be helpful.) Figure 1.4 could just as well represent a silicon lattice since the silicon atom also contains four electrons in its outer valence band. With all valence electrons in covalent bondage, no excess electrons are free to drift throughout the crystal as electrical charge carriers. In theory, this represents a perfect and stable diamond lattice of single crystal structure and, ideally, would be a perfect insulator.

CRYSTAL FLAWS

But such perfect single crystals are not possible in practice. Even in highly purified crystals imperfections exist making the crystal a poor conductor rather than a non-conductor. At the start of the manufacturing process modern and reliable transistors require as near perfect single crystal material as possible. That is, crystal that exhibits an orderly arrangement of equally spaced atoms, free from structural irregularities. Crystal imperfections fall into three general classes, each acting in its own way to influence transistor action.

ENERGY

Both light and heat cause imperfections in a semiconductor crystal. Disturbance by light striking the crystal is dependent on the frequency and magnitude of light energy absorbed. This energy is delivered in discrete and definite amounts known as *quanta* composed of particles known as *photons*.

Heat, or thermal, disturbance is also absorbed by the crystal, in the form of vibrating waves. Interference is such that when the waves are absorbed, electronic action is impaired through atomic vibration of the lattice structure; the effect is crystal heating and destruction of the "perfectness" of the crystal. Thermal waves interfere with charge movement, causing the charges to be scattered and diffused throughout the crystal. In effect, the electrons are buffeted and jostled in various and indiscriminate and indefinite directions as defined by the laws of quantum-mechanics.[9] Because of this severe thermal encounter, the electrons *gain* thermal kinetic energy which is of extreme importance in the practical operation of diodes and transistors.

ELECTRONIC

Too many or too few electrons also cause crystal imperfections. In short, in perfect single crystal all electrons are assumed to be locked in covalent bond. Those that are not are *free* and therefore constitute a form of imperfection. (Figures 1.6 and 1.7).

ATOMIC

Any atomic disorder in the lattice structure causes the crystal to be less than perfect. Crystals of this nature are said to be *polycrystal*. They are characterized by breaks in covalent bonds, extra atoms not locked in place by covalent bonds (interstitial atoms), and missing atoms that leave gaps in an otherwise orderly crystal structure (atomic vacancies). Such imperfections interfere with proper transistor action by not readily allowing charge carriers to move freely.

Interference to carrier movement also occurs when the perfect lattice structure appears as being interrupted. This can be viewed as crystal discontinuity, or as two separate crystals not properly "fit" so as to form a perfect single crystal; the two crystals appear at the point of joining as being improperly oriented to each other. This form of imperfection is referred to as a *grain* or *grain boundary*. Flaws of this nature cause impurities to be generated with consequent impairment of the perfect crystal.

Electrons set free from covalent bondage move at some given velocity and for some given time before arriving at a destination; the travel time involved is referred to as *lifetime*. While free and in motion the electron will experience numerous collisions within the crystal, with the result that electrons will not experience equal lifetimes. Where an electron's lifetime is limited and cut short, the cause is theorized to be an imperfection mechanism known as a *recombination center* (sometimes called a "deathnium center"). A recombination center acts to capture and hold an electron until an opposing carrier arrives to affect recombination and thus empty the center, to capture and then immediately release an electron, or to release an electron that has existed within the center thus producing a hole. The impurity causing the center determines at what energy level capture takes place. The electron involved may not necessarily be a *free* charge, but one from a covalent bond. In any case, the center acts as an intermediate "holding" point of charge carriers.

Another imperfection more common to silicon than to germanium is the *trap*. A variation of the recombination center, the trap as the name implies captures a carrier and holds it; emptying occurs only upon release of the first carrier, which may be held in the trap up to several minutes. Trapping is unlikely in germanium at normal temperatures, but does appear around $-80°C$. In silicon, trapping is common at room temperatures ($25°C$).[10]

The effects of the various imperfections in semiconductor crystals are many, and not always easily explained. Although much is already known about semiconductor imperfections, it is generally recognized that other imperfection mechanisms, as yet not known, may exist. Of importance, however, is that those working with diodes and transistors recognize that imperfections are both good and bad. They both hinder and help, depending of course on the imperfections involved. Semiconductors would not be possible without imperfections, yet by their very nature they act in many devious and obscure ways.

CONDUCTIVITY IN CRYSTALS

As already mentioned, to be of practical use transistors require crystal material of greater conductivity (lower R/CM^3) than found in highly purified germanium and silicon. Conductivity can be increased by subjecting the crystal to heat, to radiation, or by adding *impurities* to the crystal when it is formed.

THERMAL

Heating the crystal will cause the atoms which form the crystal to vibrate. Occasionally one of the valence electrons will acquire enough energy *(ionization energy)* to break away from its parent atom and move through the crystal. Since the atom has lost an electron, it will thus assume a positive charge equal in magnitude to the charge of the electron. In turn, once an atom has lost an electron it can then acquire another electron from one of its neighboring atoms. This neighboring atom may, also in turn, acquire an electron from one of its neighbors. It is evident that each *free* electron which results from the breaking of a covalent bond will produce an electron deficiency which can move through the crystal as readily as the free electron itself. It is convenient to consider these electron deficiencies as positively charged particles called *holes*. Each time a covalent bond is broken and a negative electron set free, a positive hole is simultaneously generated. This process is known as the *thermal generation* of *hole-electron pairs*. The average time either charged carrier, the hole or the electron, exists as a free or mobile carrier is known as *lifetime*. Should a free electron join with or collide with a hole, the electron will fill the existing electron deficiency which the hole represents and both the hole and the electron will cease to exist as free charge carriers. This joining or colliding process is known as *recombination*.

RADIATION

Transistor crystal material is very sensitive to radiation. Neutron bombardment, gamma rays, beta rays, both slow and high energy particles in various forms can effect semiconductor material. Their influence is to increase crystal lattice imperfections. Atoms, normally in space locked position within the crystal, are knocked out of position and into interstitial positions where they come to rest. What was a perfect lattice structure at that particular location in the crystal becomes imperfect by the generation of atomic vacancies as well as extra atoms. The result is a drastic reduction of minority carrier lifetime, and a change in conductivity. Moreover, how conductivity changes depends on the nature of the semiconductor material; that is, whether n-type, p-type, silicon, germanium, and so on.

IMPURITIES

Conductivity can also be increased by adding impurities to the semiconductor crystal when it is formed. This is often referred to as *doping.* And *doping level* refers to the amount of impurities added. These impurities, added in the form of atoms, replace a few of the existing semiconductor atoms that make up the crystal lattice structure. An impurity atom, depending on its nature (see Table 2), may either *donate* a free electron to the crystal structure or it may *accept* a free electron from another atom in the structure.

N-Type Material

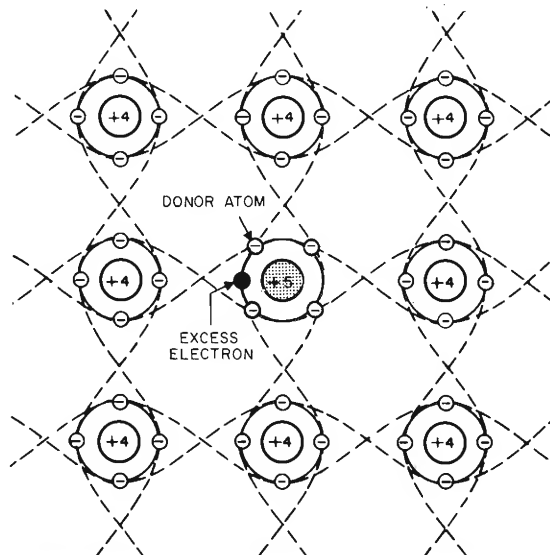
As shown in Figure 1.6 should the replacement impurity atom contain 5 electrons in its valence band, four will be used to form covalent bonds with neighboring semiconductor atoms. The fifth electron is *excess,* or *extra.* It is therefore free to leave its parent atom. When it leaves it does not leave behind a space, or hole, since the four remaining electrons join covalently with electrons of the neighbor atoms and thus satisfy all localized valency requirements. The donor atom is therefore locked in position in the crystal. It cannot move. With the loss of the electron the donor's charge balance is upset causing it to ionize. The donor impurity atom, therefore, can be viewed as a fixed-in-position positive ion.

N-TYPE MATERIAL

Figure 1.6

Since, in practice, imperfections exist in the crystal, to some extent holes also will exist. But since the electrons greatly outnumber the holes, the crystal is negative in nature and called *n-type* semiconductor. Inasmuch as electrons and holes are present in the crystal, both will contribute to the conduction process. Electrons, predominating, are the *majority carriers*; holes the *minority carriers.*

P-Type Material

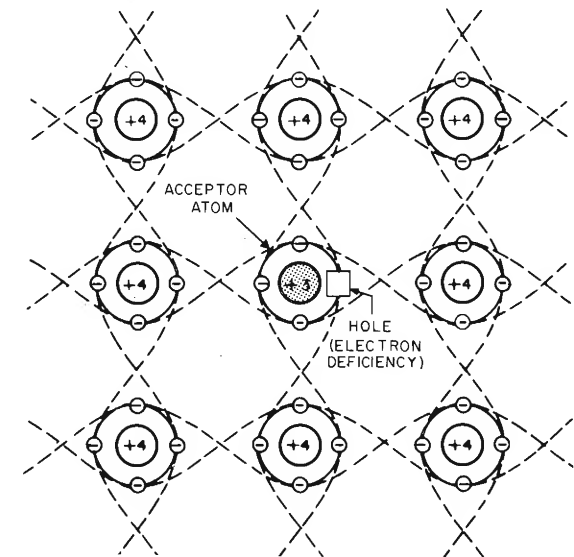
Should, on the other hand, as shown in Figure 1.7, the replacement impurity atom contain only 3 electrons in its valence band, all three will be used up in covalent bonds with neighboring semiconductor atoms. Since a lack, or deficiency, of one electron prevails an empty space will exist causing one bond to be unsatisfied. This empty space in the impurity atom's valence band is called a *hole* and is positive in nature. As such, it is able to accept an electron from the crystal in order to satisfy the incomplete bond. As in the case of the donor atom, this action contributes to locking the acceptor in its lattice position. It cannot move. The gaining of an electron upsets the acceptor's charge balance causing it to ionize; thus, the acceptor impurity atom, like the donor, can also be viewed as a fixed-in-position ion, but one of negative charge. Since, in this case, a hole has been generated elsewhere in the crystal, positive holes predominate and the material is called *p-type.*

P-TYPE MATERIAL

Figure 1.7

In p-type material, just as in n-type, both holes and electrons exist and contribute to the conduction process. Holes, predominating, are the *majority carriers*; electrons the *minority carriers.* With two oppositely charged carriers in existence in both n and p materials, two conduction (current) paths of opposite direction must exist. Both are of great importance to transistor action.

To summarize, solid-state conduction takes place in semiconductor crystals by the movement of charge carriers known as holes and free-electrons. These holes and electrons may originate either from donor or acceptor impurities in the crystal, or from the thermal generation of hole-electron pairs. During the manufacture of the crystal, it is possible to control conductivity and make the crystal either n-type or p-type by

adding controlled amounts of donor or acceptor impurities (Table 1.2). On the other hand, thermally generated hole-electron pairs cannot be controlled except by varying the crystal temperature.

ELEMENT (SYMBOL)	GROUP IN PERIODIC TABLE	NUMBER VALENCE ELECTRONS	APPLICATIONS IN SEMICONDUCTOR DEVICES
Acceptors boron (B) aluminum (Al) gallium (Ga) indium (In)	III	3	Trivalent (3), or acceptor, elements are used to form p-type semiconductors. A trivalent atom replaces a quadravalent atom in the lattice structure; lacking one electron in its valence band the trivalent atom is thus able to accept one electron from a neighboring quadravalent atom to produce a hole.
Semiconductors germanium (Ge) silicon (Si)	IV	4	Quadravalent (4) elements are basic semiconductor materials. When combined with controlled amounts of trivalent or pentavalent material, p-type or n-type transistor crystal, respectively, is formed.
Donors phosphorus (P) arsenic (As) antimony (Sb)	V	5	Pentavalent (5), or donor, elements are used to form n-type semiconductors. A pentavalent atom replaces a quadravalent atom in the lattice structure; containing an excess electron in its valence band it is thus able to donate one free electron to the crystal lattice structure.

MATERIALS USED IN THE CONSTRUCTION OF TRANSISTORS AND OTHER SEMICONDUCTOR DEVICES

Table 1.2

TEMPERATURE

Carriers move through a semiconductor by two different mechanisms: *diffusion* or *drift*. In either case temperature plays a singularly important part. Atomic activity is said to cease at absolute zero, but this is only an assumption. At absolute zero temperature (−273.165°C) a finite amount of kinetic energy is known to exist. This ever-so-small activity is known as zero-point energy and in modern physics can be located only by extremely involved methods. It is well known that charged carriers in semiconductor material are strongly influenced by temperature and that as temperature increases so too does the atomic activity. Atomic movement and motion is ever present, and the extent to which such activity and agitation occurs is only a matter of degree. In any lattice structure where all atoms are strongly bound together by covalent bonds, the atoms are continually shaking and vibrating in their lattice positions due

to thermal effects. It is important to keep in mind that the atoms, whether semiconductor or impurity, at all times remain locked in their lattice position due to the covalent bonds. Any motion of the atom, no matter how extreme, is a vibratory and elastic motion. The atom's position does not change unless a flaw exisits in the crystal.

Electrons moving in their orbits also vibrate and become excited with temperature. With continued temperature increase, their vibration becomes more violent to the extent that those possessing the most energy, break loose from parent atoms and fly out into the spaces of the lattice structure. This is especially true of valence band electrons, since by nature they possess more energy and can operate at higher energy levels. When such an electron flies free, a hole is generated and any free electron may join this hole.

Too, as mentioned under Crystal Flaws, thermal effects are characterized by the absorption of the thermal waves which interfere with electron movement. If it were possible to look into the crystal, a constant movement and motion would be seen; action of a highly complex nature, not easy to visualize nor to depict. On a grand scale, therefore, at any given temperature there is always atomic activity occurring in semiconductor material; the lower the temperature the less the activity, the higher the temperature the greater and more violent the activity.

CONDUCTION: DIFFUSION AND DRIFT

DIFFUSION

Since many charge carriers are actively moving throughout the crystal, at any given location a concentration of carriers may occur. Whenever there is a difference in carrier concentration in adjacent regions of the crystal, carriers will move in a random fashion from one region to another. Moreover, more carriers will move from regions of higher concentration to regions of lower concentration than will move in the opposite direction. In the simplest illustration, this permeation, or spreading out of carriers, throughout the crystal is shown in Figure 1.8 and is known as *diffusion*. The process is not easily explained in terms of a single electron's movement. It can be thought of as a sporadic, or random, or unorganized electron movement when the crystal is free from the influence of an electric field.

The action of diffusion is an omnipresent process in a semiconductor, dependent on the impurity content, and on temperature.

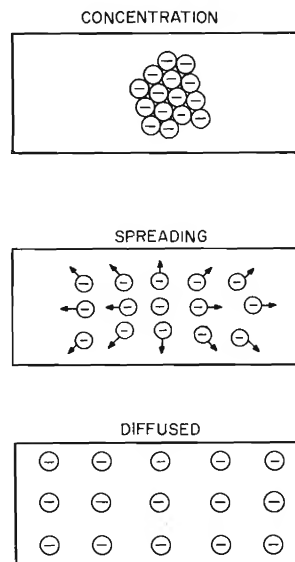
The principles of diffusion, that is, the atomic penetration of one material by another, are used in semiconductor manufacture to advantage, being widely used to form pn junctions in semiconductors. Briefly, the process consists of exposing germanium or silicon to impurity materials known as *diffusants*, generally in a furnace. Both time and temperature are of extreme importance, as well as the type of impurity diffusant (indium, antimony, etc.) used. Since each diffusant exhibits an individual diffusion constant (D), the time and temperature required for a diffusant to reach a given depth of penetration into the semiconductor will vary. Indium, for example, is a slow diffusant while antimony is much faster.

DRIFT

Even when subjected to an electric field the process of diffusion persists. The action is somewhat more defined and orderly, however, in that the field's influence causes charge movement to occur parallel to the direction of the field. This is often referred to as *drift mobility* and implies both thermal and electric field influences acting on the charge carriers.

Drift is a process that accelerates charge movement within the crystal. Should a battery, for example, be connected across the crystal, a definite and deliberate movement of carriers will begin. Direction of movement will depend on the polarity of the

CONCENTRATION

SPREADING

DIFFUSED

ELECTRON DIFFUSION IN SEMICONDUCTOR

Figure 1.8

electric field generated by the battery. Where before the fields existence carrier movement was random and sporadic – and a more or less overall state of electrostatic equilibrium existed – with voltage applied, equilibrium is upset; charge carriers are influenced, and electrical conduction takes place. This is illustrated in Figure 1.9(B) where a single conduction path in n-type semiconductor material is shown. (Figures 1.9 and 1.10 are illustrative only. Since they are two-dimensional models, presented to help explain a highly involved, and in many cases difficult to explain theory, they should not be taken too literally.)

All atoms, semiconductor and donor impurity, are locked in their lattice positions by covalent bonds as shown in Figure 1.9(A). Atoms cannot and do not leave these fixed positions. Prior to closing the switch electrons are in a continuous state of thermal diffusion throughout the crystal. Closing the switch produces an electric field throughout the crystal which influences the diffusing electrons to drift around the circuit.

Referring to Figure 1.9(B), as electron 1 enters the semiconductor through the left negative ohmic contact, electron 4 simultaneously leaves at the positive end. A balance is thus maintained between the crystal and the external circuit by this equal exchange of electrons into and out of the crystal. Electron 1 joins the hole left by the departure of electron 2 into conduction. Since the donor atoms contain extra electrons, these are also freed into the conduction process, or conduction band, to roam the crystal.

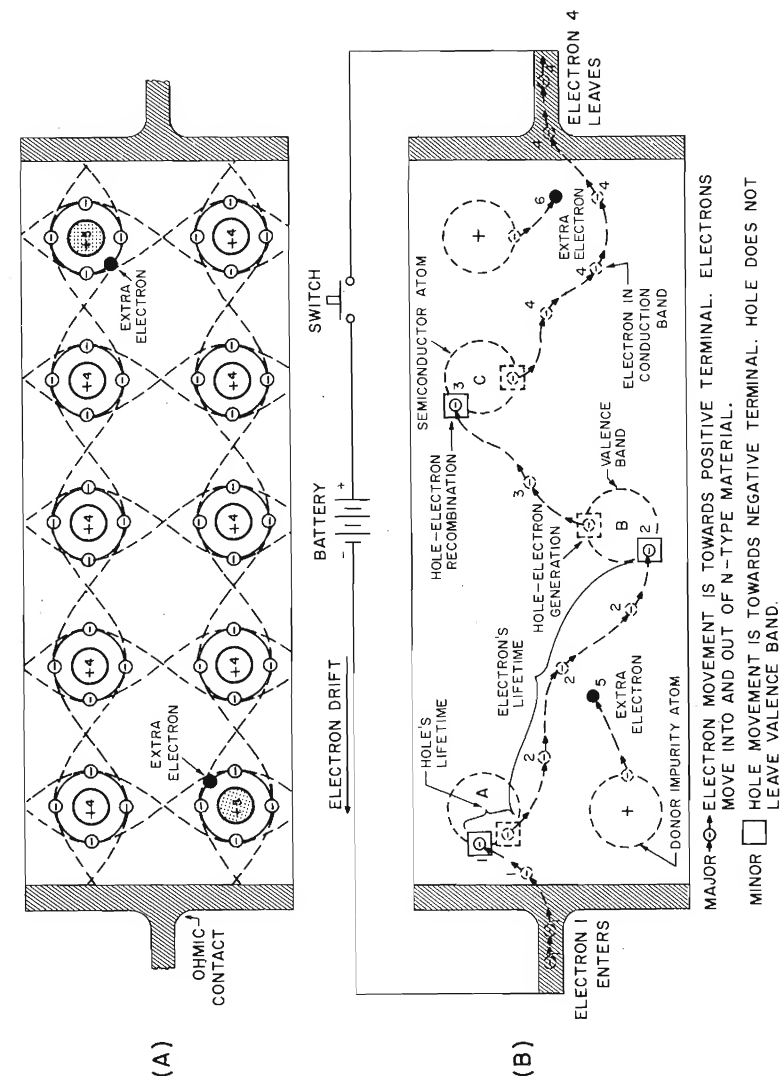
During this instant several things, all important to transistor action, happen: a hole-electron pair is *generated*, free charge carriers (electron and hole) exist for a *lifetime* to produce a portion of the overall conduction process, and, free charge carriers (electron and hole) unite together in *recombination*. Here, in essence, is the process of conduction in a semiconductor – *generation*, *lifetime*, and *recombination*. (It is important to keep in mind, that in this process, only the valence electrons possess the ability to leave the valence bands of their parent atoms and roam throughout the

DRIFT IN N-TYPE SEMICONDUCTOR

Figure 1.9

(A)

(B)

MAJOR □ HOLE MOVEMENT IS TOWARDS NEGATIVE TERMINAL. HOLE DOES NOT LEAVE ATOM'S VALENCE BAND.

MINOR ELECTRON MOVEMENT IS TOWARDS POSITIVE TERMINAL. ELECTRONS MOVE INTO AND OUT OF P-TYPE MATERIAL.

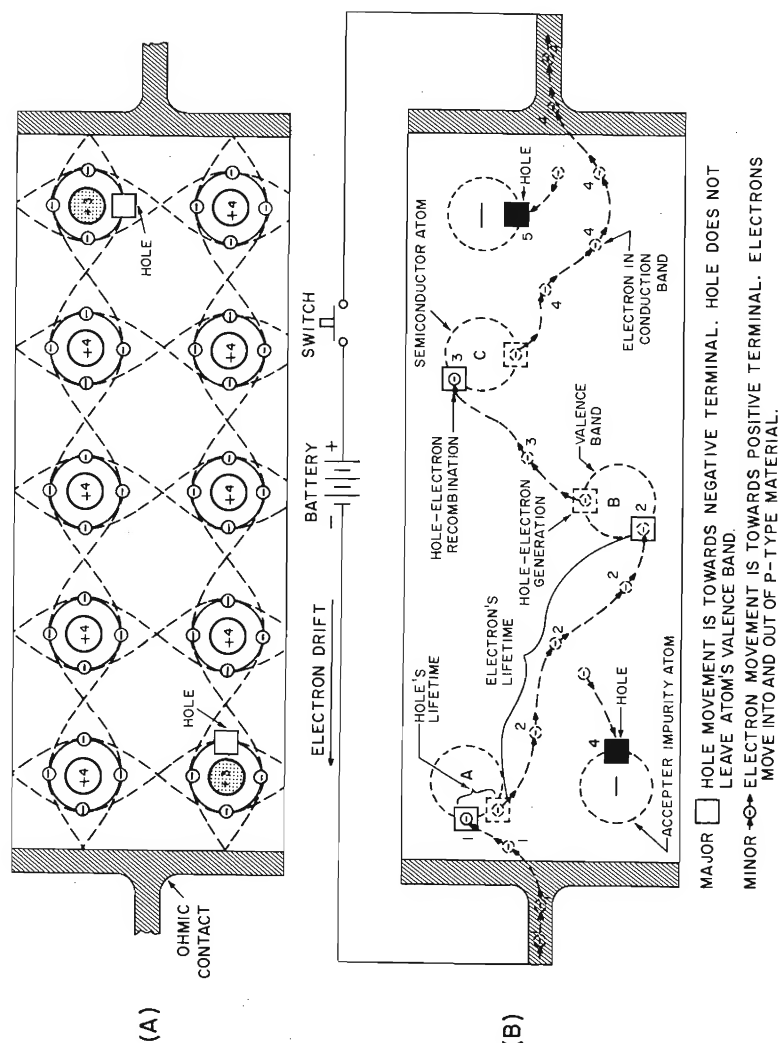



Figure 1.10

DRIFT IN P-TYPE SEMICONDUCTOR

crystal; holes, being what they are – electron deficiencies – remain at the level of the valence band. Holes, therefore, cannot and do not exist outside of semiconductor material.) In Figure 1.9(B) hole activity can be better followed by starting with electron 4 leaving atom C.

Electron movement, then, is an actual movement from negative to positive around the *total* circuit while hole movement is from positive to negative, but only inside the crystal.

Figure 1.10 depicts conduction in p-material. As shown in Figure 1.10(A) all semiconductor and acceptor impurity atoms are locked in their lattice positions by covalent bonds. Since the impurity atoms are acceptors, holes predominate. Electrons, although in the minority within the crystal, are still basic to the conduction process. In Figure 1.10(B), starting at the positive terminal, hole movement can be followed through the crystal towards the negative terminal. Note that the impurity atoms accept electrons from some other bond in the crystal, thus causing the acceptors to ionize and become negative. These electrons moving to the acceptors leave other holes behind. The process is not unlike that depicted for n-type material except that in p-material a greater number of holes exist in the semiconductor to contribute to current conduction. Hole migration, then, is from positive to negative in the crystal; while electron conduction is from negative to positive. Just as in n-type material, conduction within the crystal is by generation, lifetime, and recombination of charge carriers.

For the single conduction paths illustrated in Figures 1.9(A) and 1.10(B) it is interesting to note that if the electrons and holes are counted, keeping in mind that electrons 1 and 4 equal one charge,* the following results.

	Electron	Holes
n-type semiconductor	*1–2–3–⑤–⑥ Major conduction	1–2–3 Minor conduction
p-type semiconductor	1*–2–3 Minor conduction	1–2–3–④–⑤ Major conduction

Circled numbers indicate *extra* electrons and holes.

PN JUNCTIONS (DIODES)

Connecting the p-type and n-type materials of Figure 1.9 and 1.10 in series with a single battery, as shown in Figure 1.11, is no different – from the viewpoint of the external circuit – than connecting two resistors in series, with one exception. The nature of conduction within each semiconductor material will be different, as already explained. In the case of Figure 1.11, as voltage is increased a linear relationship will prevail in accordance with Ohm's law.

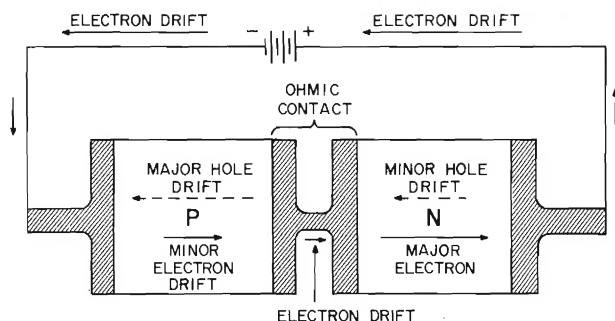
Should the center ohmic contact be removed and an actual contact made between p and n materials, action both inside the crystal and as viewed by the external circuit will then differ radically from Figure 1.11. This change of character is brought about by the forming of p and n materials into a *pn junction.* (Note the word "forming" is used, not "connected." Reliable and efficient pn junctions cannot be made by placing pieces of p and n materials together. Tightly pressing, or even welding the materials allows only small area surface contact to be made. Too, the exposed surfaces can be contaminated by airborne impurities. For optimum control of conduction, pn junction structure must be single crystal in nature. This means that single crystal material must be continuous from n material through the junction and into the p material. This is

P-TYPE AND N-TYPE MATERIAL CONNECTED IN SERIES

Figure 1.11

accomplished by chemical means. Suffice to say that pn junction fabrication is highly complex and specialized, and beyond the scope of this Manual. Figure 1.12, therefore, is illustrative only.)

Prior to the p and n materials being joined, atomic activity within each is random. Figure 1.12(A) is representative of this state. Since holes predominate in the p material and electrons in the n, each material – although electrically neutral unto itself – will exist at a different charge level from the other because of differences in nature and impurity content. When the two dissimilar materials form, as shown in Figure 1.12(B), an energy exchange occurs as the materials try to equalize. This exchange is shown by electrons 1 and 2 moving across to fill the holes in the p-type material. At this instant of brief conduction the donor and acceptor atoms change their charge states and ionize. This is shown in Figure 1.12(C). (It should be kept in mind that this is a two-dimensional, highly simplified illustration, and all action is in reality three-dimensional with many more charged carriers involved.)

The electrical neutrality of both p and n materials (existing at different charge levels), upset by this brief but dynamic exchange of electrons, tend to align with each other (alignment of Fermi levels). During the forming, hole-electron recombinations readily occur, and as the action progresses a limited area empty of free charge carriers is produced. This "no free-charge land" is called by many names: *barrier, depletion region, dipole layer, junction barrier, potential barrier* and sometimes *space charge region.* But mostly it is referred to as a *pn junction* or *junction diode.*

It would seem that during this brief forming process that all existing free charge carriers should combine. If this did occur, assuming equal impurity content, a single piece of neutralized crystal would result; it would be neither p nor n in nature. After a few recombinations take place in the vicinity of the junction area, and a "no free-charge land" produced, conduction decreases as an electric field builds up, generated by – and located between – the newly created positive ions in the n-type material and negative ions in the p-type material. Figure 1.12(D) attempts to illustrate the pn junction after forming.

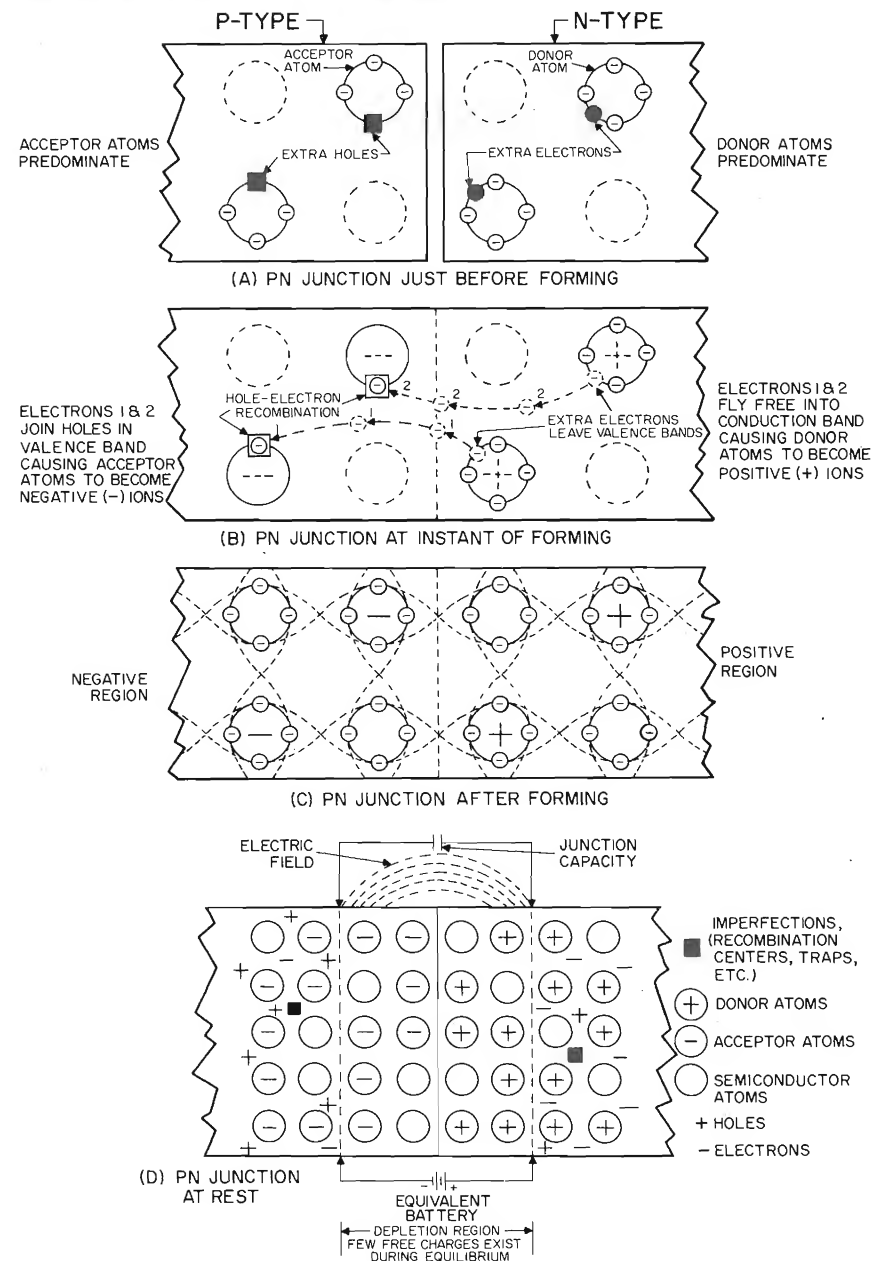
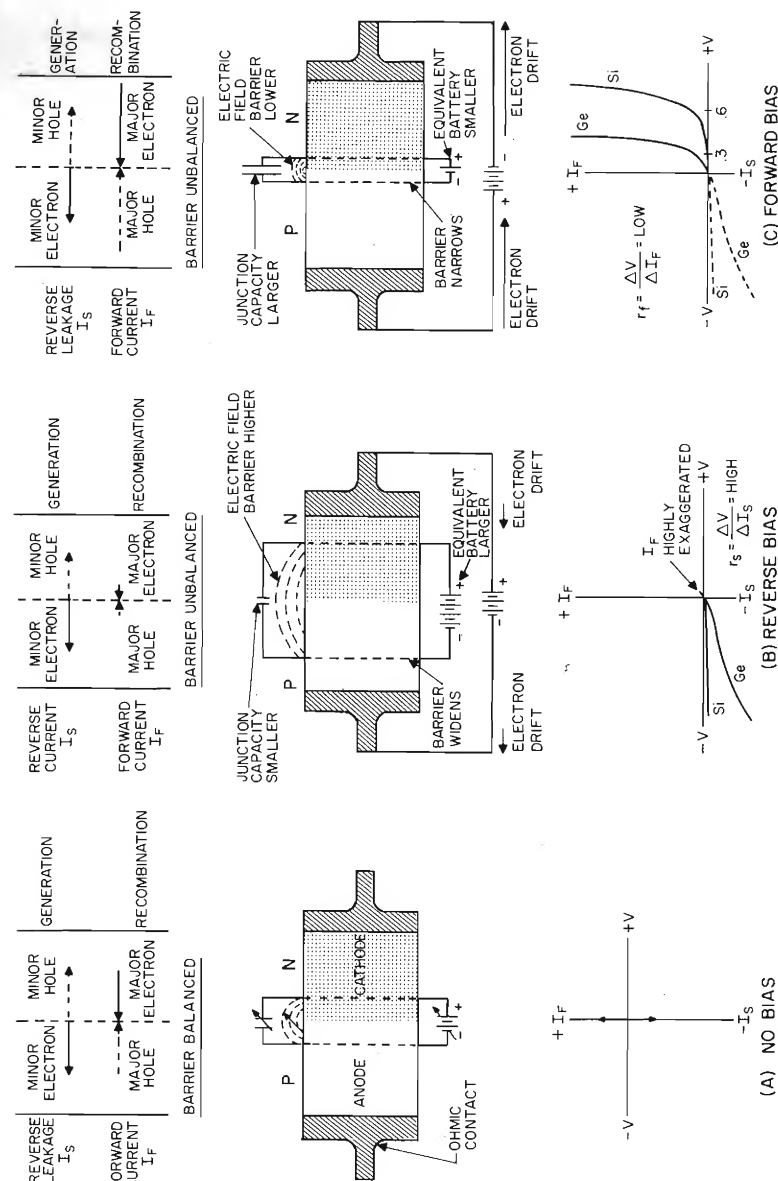
Total recombinations cannot occur, however, because of thermal generation of hole-electron pairs, hole-electron recombinations, and the effects of recombination centers and trap imperfections. All combine in a highly complex process to bring about a *barrier balance.* The eventual culmination of this forming process can be viewed as a balance of major and minor conduction currents as shown in Figure 1.13(A). Perfect barrier balance is never completely possible because of external influences. Much like the balancing of a set of delicate scales when a state of equilibrium exists,

PN JUNCTION FORMING

Figure 1.12

PN JUNCTION BIAS
Figure 1.13

so it is with a pn junction. Although a depletion area exists, and in theory no charge movement across the barrier is taking place, in reality the barrier balance is such that occasional charge carriers do diffuse to opposite regions to cause opposing currents to exist. At any instant currents may be equal or unequal in magnitude since temperature is always present.

JUNCTION CAPACITY

With each side of the barrier at an opposite charge with respect to the other, each side can be viewed as the plate of a capacitor. In short, the pn junction possesses capacity. As illustrated in Figure 1.13 junction capacity changes with applied voltage. Figure 1.14 graphically shows junction capacity variation with reverse voltage for two different device junctions.

Depending on the application, junction capacity can be an advantage, or a detriment. To illustrate the former, the FM Tuner in Chapter 15 uses a reverse biased 1N678 to accomplish Automatic Frequency Control (AFC) of the oscillating converter. The diode, in this case, is being used as a dc voltage controlled variable capacitor. As a detriment, in high frequency amplifier applications where small capacity effects are more apparent, the same junction capacity would not be desirable since it limits the transistor's upper useful frequency of operation. Further, in intermediate and high frequency amplifier applications excessive collector-base capacity can cause positive feedback and undesirable oscillation. On the other hand, should the capacity be such that it is within the limits of the associated tuning circuit's required LC ratio, it might be used to advantage as part of the capacitive component. Chapter 2 discusses in greater detail device capacities in general, and their effects on high frequency performance.

The barrier's electric field is often referred to — and can be visualized — as a *space charge equivalent battery*. Since the field spans a specific distance it is said to have *width*, and since the field possesses an intensity it is said to have *height*. These effects can be expressed in volts. A pn junction made from germanium, for example, can be thought of as having an equivalent battery field voltage of about 0.3 volt; a junction made from silicon, about 0.6 volt. Both the width and height can be changed by applying an external voltage to the crystal. Herein lies the real importance for the existence of the pn junction in its relation to external circuitry. Depending on the polarity of the applied voltage, the crystal will either *pass* or *block* current. In short, it will *rectify*.

CURRENT FLOW

In the field of electronics one of the first great bewilderments of many students is that of current flow. Not necessarily the physics of it, but its direction. One school of thought has current flowing in the direction of *electron drift*, negative to positive. Another has agreed that current flows positive to negative. This is known as *conventional current flow*. The fact that two different and opposing flow directions are recognized in electronics has always been confusing for students in general to cope with. The arrival of the transistor compounded the confusion since it brought with it current flow by *hole movement*, from positive to negative. Add to the foregoing such diverse terms as: forward current, reverse current, saturation current, leakage current, etc., and it is understandable why semiconductors on first encounter can be confusing.

The question itself of "which way does the current flow?" is academic. In practical circuit design it can even be a trivial consideration, except where accurate communications is involved; of real importance is that one try to be consistent. Consistency is not always easy, however, when dealing with the semiconductor "world of opposites."

DIODE "CONCEPT"

With the "opposite" natures of npn and pnp transistors, the opposite voltage polari-

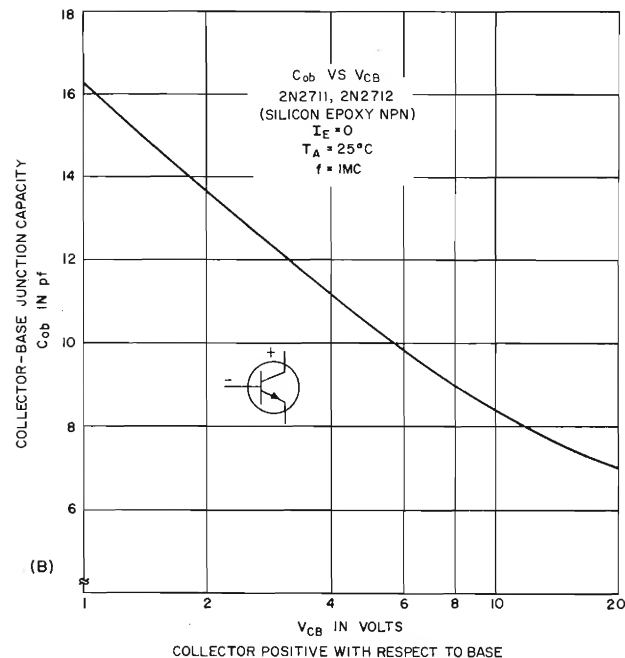
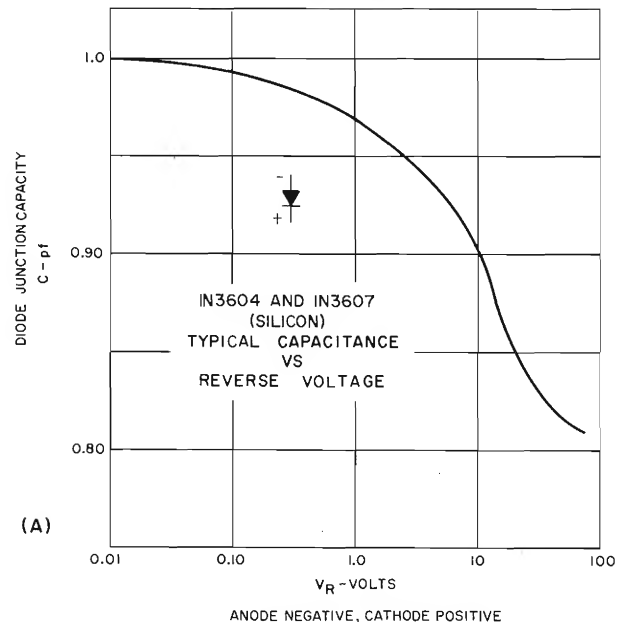
1.0
0.90
0.80
DIODE JUNCTION CAPACITY
C - pf
IN3604 AND IN3607
(SILICON)
TYPICAL CAPACITANCE
VS
REVERSE VOLTAGE
(A)
0.01 0.10 1.0 10 100
V_R - VOLTS
ANODE NEGATIVE, CATHODE POSITIVE

TRANSISTOR AND DIODE JUNCTION CAPACITY

Figure 1.14

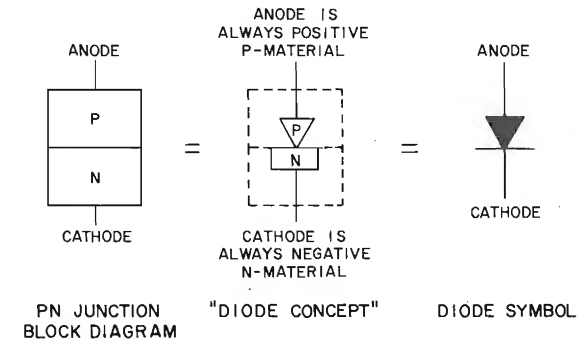
ties each require, and the opposite natures of hole and electron movement taking place within a transistor at the same instant, it is not surprising to find even seasoned circuit designers, especially in their first encounters with solid state devices, bewildered with transistor action. One way to overcome this first confusion and induce some sense into practical circuit work is to apply the "diode concept" approach as an aid. This precludes, however, thinking in terms of charge carrier movement, for the moment at least, and requires visualizing by *conventional current* flow, positive (+) to negative (−). The "diode concept" presents a pn junction as shown in Figure 1.15.

"DIODE CONCEPT" OF PN JUNCTION

Figure 1.15

It is only necessary to keep in mind

1. Anode is always positive p material.
2. Cathode is always negative n material.
3. Conduction (passing of current) occurs when positive potential is applied to positive p anode and negative potential to negative n cathode (*forward* bias).
4. Blocking occurs when negative potential is applied to positive p anode and positive potential to negative n material (*reverse* bias).

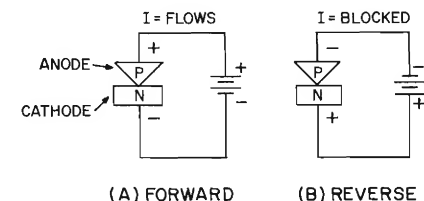
Figure 1.16 illustrates these simple points.

BIAS OF PN JUNCTION

Figure 1.16

BIAS: FORWARD AND REVERSE

At this point it would be helpful to replace the junction diode, which, it should be remembered is a unilateral (one-way) device, with a resistor, which is a passive bilateral (two-way) component. The electrical difference between the two can be shown by graphically plotting voltage vs. current.

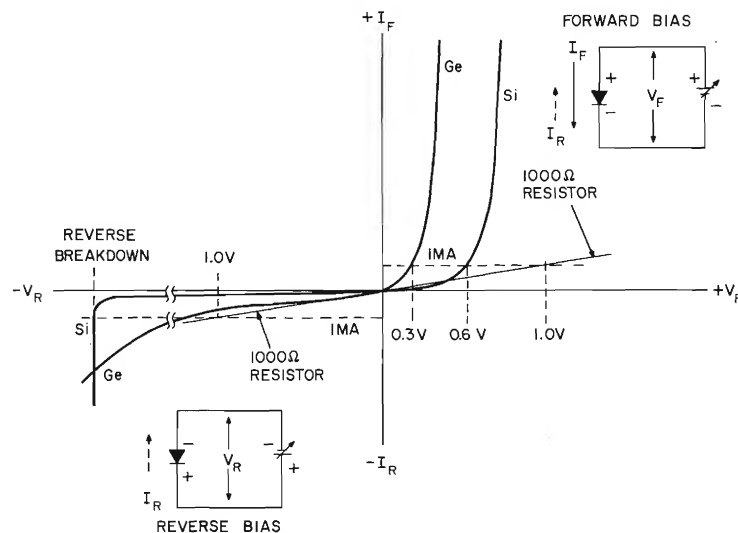
Connecting a 1000 ohm resistor in the simplest form of electric circuit, a series circuit, using a current meter (or a zero center galvanometer), and a 1 volt power supply, a current will flow causing the meter to deflect to $I = E/R = 1/1000 = 1$ ma; should the battery polarity be reversed and a second reading taken, the current flow would again cause the meter to deflect to 1 ma, but in the opposite direction. Recording a series of voltage vs. current readings from zero voltage, first with the battery connected in one direction, say the *forward* direction; then in the opposite direction, say the *reverse* direction, will show a linear relationship between voltage and current. This is illustrated in Figure 1.17. As shown, whether the resistor is forward or reverse biased, a linear plot results. The variable battery, in theory at least, sees an *unchanging* positive resistance of 1000 ohms. This is not true, as shown in Figures 1.13(B,C) and 1.17, when a pn junction diode is subjected to forward and reverse voltages.

DC CHARACTERISTICS OF RESISTOR, GERMANIUM DIODE, AND SILICON DIODE UNDER INFLUENCE OF FORWARD AND REVERSE BIAS VOLTAGE

Figure 1.17

Figures 1.13(B,C) and 1.17 represent the classical semiconductor diode curve. As with other phenomena of the physical sciences, the pn junction is also governed by natural laws of growth and decay. Charge diffusion across the barrier, charge lifetimes, charge concentration, and temperature, all influence the shape of the curve. As with many of the other phenomena in nature, the pn junction curve, under conditions of variable bias, is characterized by "natural" logarithms, and the following well known pn junction equation applies.

$$I_F = I_S\,(\epsilon^{qV/KT} - 1)$$

where

I_F = forward current
I_S = reverse, or saturation current
ϵ = natural log 2.71828
q = electron charge 1.6×10^{-19} coulomb

V = applied bias voltage
K = Boltzmann's constant (1.38×10^{-23} watt sec/°K)
T = absolute temperature in degrees Kelvin (at room temperature $K = 300$)

At room temperature the exponent $KT/q = 0.026$ volt, thus

$$I_F = I_S\,(\epsilon^{0.026V} - 1)$$

Forward bias corresponds to positive values of V while reverse bias conditions correspond to negative values of V. In the case of reverse bias (negative V) the exponential term will diminish. Since the barrier is widened and charge movement at a minimum, current flow will be small and relatively fixed by thermal energy absorbed by the crystal; for this reason I_S is often referred to as reverse *saturation* current since it is a fixed variable, controlled only by design of the junction and thermal influences. I_F will therefore diminish towards zero, and I_S remain relatively constant. With $I_F \cong$ zero, I_S small, and negative bias V large, the junction resistance will be very high.

With forward bias (positive V) the exponential term rapidly increases. This causes I_F to take on the classical "natural" look. With I_F large and V small, the junction resistance will be correspondingly very small. In practice I_S is considered a *leakage* current tending to subtract from I_F. In germanium, reverse leakage is about 1000 times greater than in silicon.

TRANSISTOR

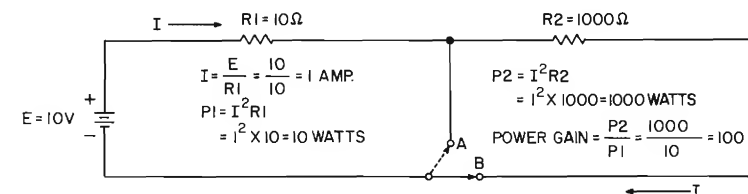
If it were possible to simulate the circuit in Figure 1.18, useful work could be performed. Connecting resistor R1 in series with the 10 volt battery by placing the switch in position A would cause an ampere of current to flow, resulting in a power dissipation in R1 of 10 watts. If, when throwing the switch to position B, the same 1 ampere could be made to flow through R2, a hundred-fold gain in power dissipation would result. Forgetting the drop in R1 and concentrating on R2, if R2 were in a position to offer a large portion of the dissipated power to an external load where *useful* work could be performed, Figure 1.18 could be considered an *active* circuit because of its ability to amplify power. This, in effect, is accomplished by the transistor.

TRANSFER + RESISTOR = TRANSISTOR

Figure 1.18

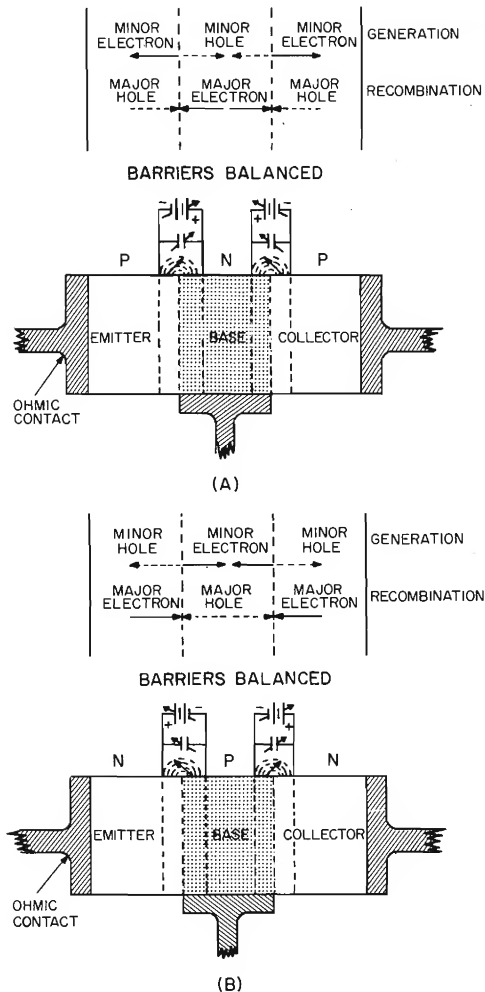
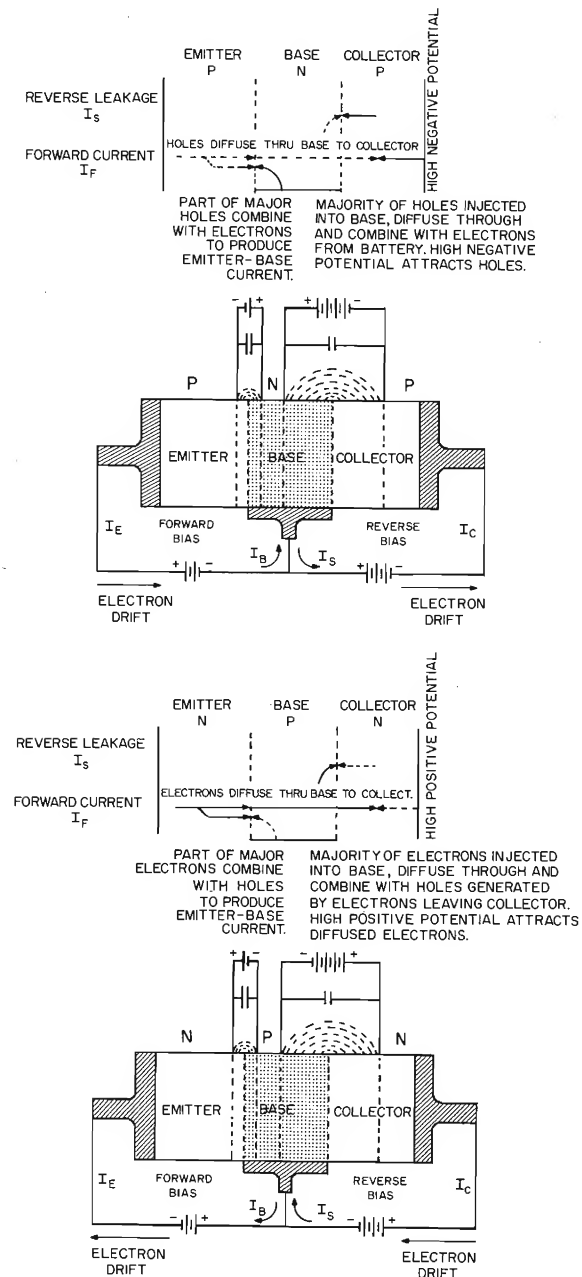
By placing a second pn junction adjacent to the first, with the connecting semiconductor material common to both junctions, as shown in Figure 1.19, and by forward biasing one junction and reverse biasing the other junction, the conditions of power gain are possible. Depending on which side of the existing pn junction the second junction is formed, will determine the transistor's type, PNP or NPN. And as shown in Figure 1.20 the type will determine the polarity of the bias voltages. Figure 1.22 shows the generally accepted circuit symbols used for NPN and PNP transistors.

JUNCTION TRANSISTOR

Figure 1.19

Transistors operate by the mechanisms of *injection*, *diffusion*, and *collection*. It will be noted in Figure 1.20 that the three elements are labelled emitter, base, and collector, regardless of type. Should the emitter-base portion of the transistor be forward biased, a drift-movement of charges will begin. Majority carriers, holes or electrons, depending on the transistor type, will enter the base region to recombine with opposite carriers. In effect these majority carriers can be thought of as being emitted from the emitter and injected into the base region. Those charges escaping recombination near the junction area will penetrate further into the base region. Once in the base, carriers spread out by the process of diffusion. Applying a reverse bias of sufficient magnitude from collector to base, as shown, will cause the carriers diffused throughout the base region to continue into the collector region. Majority carrier movement will therefore have taken place, originating within a low resistance region (emitter-base junction) and by diffusion and collection through a high resistance region (base-collector junction). The transistor therefore meets the conditions of Figure 1.18.

BIASED JUNCTION TRANSISTOR
(COMMON BASE CONNECTION)
Figure 1.20

TRANSISTOR CIRCUITS AND CHARACTERISTICS

Figure 1.21

Since the transistor is a three element, three lead device it is possible to use it in any of three different, and useful, configurations. The identification of each of these individual circuits is derived from the element "common" to both input and output. Figure 1.21 illustrates this, showing the three configurations: common base, common emitter, and common collector; an often used variation is "grounded" emitter, "grounded" base, etc., since the common element is usually returned to the signal ground point in a circuit.

ALPHA

Since fewer carriers reach the collector than leave the emitter region, the collector current I_C will be *less* than the emitter current I_E. The ratio I_C/I_E defines the *total* forward current gain of the transistor as viewed from an external circuit, and is called *alpha* (α). This parameter is seldom greater than 1, and in practice falls between 0.95 to better than 0.99.

Within the device several mechanisms contribute to the transistor's α. First, and of great importance in controlling alpha, is the *emitter efficiency* γ, i.e., how efficiently the emitter injects carriers into the base region. The greater the forward emitter current moving from emitter to base, in contrast to opposing "leakage" current, the higher γ will be. This is brought about by a greater concentration of majority carriers existing in the emitter than are present in the base region.

A second mechanism contributing to the transistor's overall α is called the *base transport factor* β^*. As carriers diffuse through the base after being injected from the emitter, some will recombine in the base to form base current I_B. These carriers can be considered lost since they will never reach the collector region. If few recombinations are to occur in the base region, either the diffusion length of the injected carriers must be such that they penetrate across the base to the collector region, or the width of the base must be made narrower. Base width as it relates to carrier penetration is therefore critical if the greatest number of carriers injected into the base are to reach the collector region. Transport factor β^* is also a controllable mechanism of importance in transistor action.

The mechanism of carrier collection by the collector region is known as *collector multiplication factor* α^*. In general, it gives an indication of the level of current injection from base to collector region and is a function of the relationship existing between majority carriers present in the collector to those being injected. Normally, α^* is equal to unity.

By proper selection of each mechanism, through control of the nature and size of p and n materials that make up the transistor, the α is controllable.

Alpha (α) is sometimes called dc alpha, or α_F, to indicate forward current transfer ratio, the dc current gain of the device itself. Since this is a static dc measurement, it tells little of the gain or impedance characteristics of the transistor when subjected to signal conditions in an actual circuit. It does, however, offer some indication as to the merit of the transistor as an *active* device; that is, whether it is capable of power gain.

Under dc conditions, dc alpha (α_F) is usually designated α_{FB} for the common-base configuration. The capital letters F and B point out that static dc conditions prevail, and that the *forward* current gain of a common-*base* circuit is being defined. By the matrix method of circuit analysis small-signal gain is abbreviated h_{fb}, and sometimes as h_{21}. This is discussed in Chapter 2.

BETA

As shown in Figure 1.21 for the common-base circuit, if the emitter current $I_E = 1$ and $I_C = \alpha$ the base current $I_B = 1 - \alpha$. Connecting the transistor into a common-emitter configuration and feeding signal into the base, forward gain would

then be

$$\frac{I_C}{I_B} = \frac{\alpha}{1 - \alpha}. \quad \text{As an example, if } \alpha = .99, \quad \frac{.99}{1 - .99} = \frac{.99}{.01} = 99$$

thus the CE configuration is more useful in that it produces more gain than the common-base circuit. The $\alpha/1 - \alpha$ ratio is referred to as *beta*, or β. The static dc forward current gain of a transistor in the common-emitter configuration is designated as "dc beta," β_F, h_{21_E}, or h_{FE}. The latter two terms come from the matrix method of circuit analysis.

It should be noted that if α is high, the base current term $1 - \alpha$ is quite small. Therefore, the higher the transistor's alpha, the higher the impedance looking into the base of a common-emitter configuration. Hence, by virtue of its combination of high input impedance and high gain, the common-emitter configuration more readily meets general amplifier requirements. (Chapter 6 discusses frequency limitations of CB and CE configurations under *Gain Bandwidth Product.*)

BASE-EMITTER BIAS ADJUSTMENT

A useful rule-of-thumb common to both NPN and PNP transistors is presented in Figure 1.22 for adjustment of base-emitter bias. Difficulty is often encountered in the first practical transistor circuit work in recognizing that

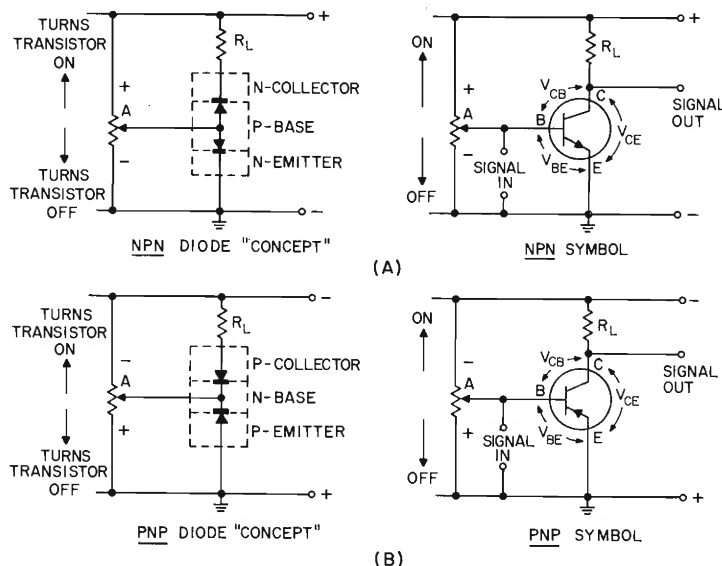
1. Moving the base towards the collector voltage supply turns the transistor *on*.
2. Moving the base away from the collector voltage supply turns the transistor *off*.

BASE-EMITTER BIAS ADJUSTMENT TURNS TRANSISTOR "ON" OR "OFF"

Figure 1.22

As shown in Figure 1.22(A) by the "diode concept" method, when the base connected slider A is moved toward the positive voltage supply, the anode of the base-emitter diode goes positive with respect to the cathode. Since this forward biases the diode, it conducts (I_B) and the transistor turns *on* allowing collector current (I_C) to

flow. Moving slider A away from the positive supply voltage decreases forward bias across the base-emitter diode causing the diode, hence the transistor, to turn *off*.

TRANSISTOR SWITCH

When turned fully on, the transistor is said to be operating in the *saturation* region. When turned fully off, it is said to be operating in the *cut-off* region. (The region between is often referred to as the *transition* region.) The transistor can therefore be used as a *switch* by simply biasing the base-emitter diode junction *off* (cut-off) or *on* (saturation). Chapter 6 offers a detailed discussion of Switching Characteristics.

TRANSISTOR AMPLIFIER

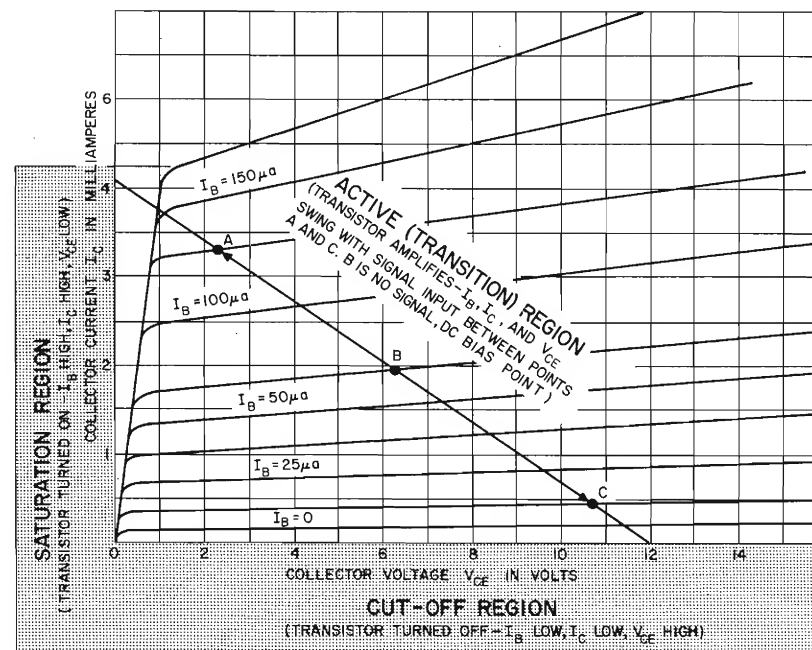
Adjusting base-emitter bias to some point approximately midway between cut-off and saturation will place the transistor in the *active*, or *linear*, region of operation. When operating within this region, the transistor is able to *amplify*. Figure 1.23 locates the cut-off, active, and saturation regions of transistor operation on a typical set of collector characteristic curves. For amplifier operation, base-emitter dc bias will be approximately 0.3 volt for germanium and 0.6 volt for silicon, shown as point B in Figure 1.17.

TYPICAL COMMON-EMITTER COLLECTOR CHARACTERISTICS

Figure 1.23

SYMBOLS AND ABBREVIATIONS

Chapter 2 discusses the transistor as a small-signal low and high frequency device. It should be noted that parameter symbols differ from those in Chapter 1 where only dc conditions are considered. Inasmuch as the transistor encounters a variety of electrical conditions, a variety of symbols is necessary to describe these conditions. Direct

current, no signal conditions — as discussed in this chapter — are defined by all capitals; ac rms signal conditions by capital and lower case subscripts; instantaneous conditions use all lower case letters. Examples of this mixture follows.

DIRECT CURRENT (no signal)	ALTERNATING CURRENT (rms conditions)	ALTERNATING CURRENT (instantaneous conditions)
I_B, V_{CB}, I_E, etc.	I_b, V_{cb}, I_e, etc.	i_b, v_{cb}, i_e, etc.

More complete information on Letter Symbols and Abbreviation for Semiconductors is given in Electronic Industries Association (EIA) document RS-245. This is available from the Engineering Department of EIA, 11 West 42nd Street, New York 36, New York, at a nominal cost. Additional symbol information is presented in Chapter 19 of this Manual.

LEAKAGE

As previously mentioned, the real importance of the pn junction is its ability to pass or block current flow; that is, to function as a unilateral device. But this suggests a perfect junction. In practice this is not the case.

Generation of hole-electron pairs by thermal influences causes a reverse leakage to exist in any pn junction. Referred to as either I_{CO} or I_{CBO} in transistors (measured from collector-to-base with emitter open, hence subscript CBO), leakage is generated in four ways.

One component originates in the base region of the transistor. At any temperature, a number of interatomic energy bonds will spontaneously break into hole-electron pairs. When a voltage is applied, holes and electrons drift in opposite directions and can be seen as I_{CO} current. When no voltage is present, the holes and electrons eventually recombine. The number of bonds that will break can be predicted theoretically to double about every 10°C in germanium transistors and every 6°C in silicon. Theory also indicates that the number of bonds broken will not depend on voltage over a considerable voltage range. At low voltages, I_{CO} appears to decrease because the drift field is too small to extract all hole-electron pairs before they recombine. At very high voltages, breakdown occurs.

A second component of I_{CO} is generated at the surface of the transistor by surface energy states. The energy levels established at the center of a semiconductor junction cannot end abruptly at the surface. The laws of physics demand that the energy levels adjust to compensate for the presence of the surface. By storing charges on the surface, compensation is accomplished. These charges can generate an I_{CO} component; in fact, in the processes designed to give the most stable I_{CO}, the surface energy levels contribute much I_{CO} current. This current behaves much like the base region component with respect to voltage and temperature changes. It is described as the surface thermal component in Figure 1.24.

A third component of I_{CO} is generated at the surface of the transistor by leakage across the junction. This component can be the result of impurities, moisture, or surface imperfections. It behaves like a resistor in that it is relatively independent of temperature but varies markedly with voltage.

The fourth component of I_{CO} is generated in the collector depletion region. This component is the result of hole-electron pair formation similar to that described as the first I_{CO} component. As the voltage across the collector junction is increased, the depletion region will extend into the base and collector regions. The hole-electron pairs generated in the base portion of the depletion region are accounted for by the first I_{CO} component discussed, but those generated in the collector portion of the depletion region are not included. The number of pairs generated in the collector portion of the depletion region and, thus, the I_{CO} from this region depend on the volume of the depletion region in the collector. Inasmuch as this volume is a function of collector and base resistivity, of junction area, and of junction voltage, the fourth component of I_{CO} is voltage dependent. In an alloy transistor, this component of I_{CO} is negligible

CROSS SECTION OF NPN PLANAR PASSIVATED TRANSISTOR SHOWING REGIONS GENERATING I_{CO}
(A)

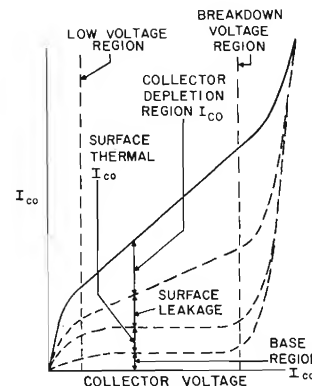
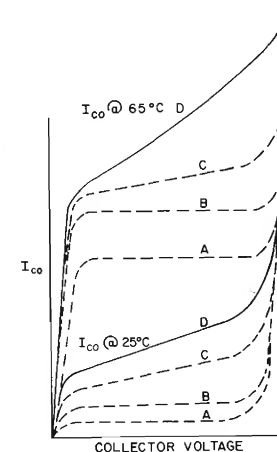
NOTE:
CURVES A INDICATE THE BASE REGION I_{CO}
CURVES B INDICATE THE SUM OF BASE REGION AND SURFACE THERMAL I_{CO}
CURVES C INCLUDE THE SURFACE LEAKAGE COMPONENT
CURVES D INCLUDE THE COLLECTOR DEPLETION REGION I_{CO} AND INDICATE THE MEASURED I_{CO}

VARIATION OF I_{CO} COMPONENTS WITH COLLECTOR VOLTAGE
(B)

VARIATION OF I_{CO} COMPONENTS WITH TEMPERATURE
(C)

Figure 1.24

since the collector depletion layer extends only slightly into the collector region due to the high base resistivity and low collector resistivity. In a mesa or planar structure, where the collector region is not too heavily doped, the depletion region extends into the collector, and this fourth I_{CO} component may be appreciable. Since this mechanism of I_{CO} generation is hole-electron pair formation, this component will be temperature sensitive as well as voltage dependent.

Figure 1.24(A) shows the regions which contribute to the four components. Figure 1.24(B) illustrates how the components vary with voltage. It is seen that while there is no way to measure the base region and surface energy state components separately, a low voltage I_{CO} consists almost entirely of these two components. Thus, the surface leakage contribution to a high voltage I_{CO} can be readily determined by subtracting out the low voltage value of I_{CO}, if the collector depletion layer contribution is small.

Figure 1.24(C) shows the variation of I_{CO} with temperature. Note that while the surface thermal component, collector depletion region component and base component of I_{CO} have increased markedly, the surface leakage component is unchanged. For this reason, as temperature is changed the high voltage I_{CO} will change by a smaller percentage than the low voltage I_{CO}.

Figure 1.25 shows typical variation of I_{CO} (I_{CBO}) with temperature for germanium, voltage and temperature for silicon.

REVERSE LEAKAGE VS. TEMPERATURE

Figure 1.25

BIAS STABILITY

In actual transistor circuit design one of the more important aspects of the design is dc biasing (see Chapter 4). Since stable circuit operation is highly dependent on temperature, thermal influences that may effect the transistor and therefore circuit performance must be considered in design of the dc bias circuit.

The three most important transistor parameters to be considered are dc forward current gain h_{FE}, reverse leakage I_{CBO}, and base-emitter voltage V_{BE}. All vary with temperature. All effect bias stability and must be accounted for if stable operation is to result.

Figure 1.26 shows typical variation of dc current gain h_{FE}, and ac current gain h_{fe} vs. temperature. Since dc gain h_{FE} is here defined as I_C/I_B, and since I_C is approximately equal to h_{FE} ($I_B + I_{CO}$), it can be seen that h_{FE} is dependent on I_{CO}. (I_B represents the current measured if an ammeter is inserted in the base.) If the base is open circuited ($I_B = 0$), collector current will continue to flow of magnitude $I_C = h_{FE\ OPEN}\ I_{CO}$, since I_{CO} is diverted through the emitter. The $h_{FE\ OPEN}$ term is defined as $\alpha N/1 - \alpha N$ where αN (alpha N) is the ratio of collector to emitter currents with *zero* collector to base voltage, at an emitter current approximately the value of $h_{FE\ OPEN}\ I_{CO}$. As defined here, h_{FE} is infinite when $I_B = 0$. Dc gain h_{FE} will rapidly increase with temperature because of I_{CO}.

In contrast, ac current gain h_{fe} is relatively independent of I_{CO} and generally increases about 2 to 1 from −55° to +85°C. Figure 1.26 illustrates the variation of both h_{FE} and h_{fe} with temperature.

VARIATION OF h_{FE} AND h_{fe} VS. TEMPERATURE

Figure 1.26

Normal semiconductor properties tend to disappear at high temperatures with the result that transistor action ceases. This temperature usually exceeds 85°C and 150°C in germanium and silicon transistors, respectively.

When a transistor is used at high junction temperatures, it is possible for regenerative heating to occur which will result in thermal run-away and possible destruction of the transistor. For maximum overall reliability, circuits should be designed to preclude the possibility of thermal run-away under the worst operating conditions. Thermal run-away is discussed in detail in Chapter 4.

A major problem encountered in the operation of transistors at low temperatures is the reduction in both the ac and dc current gain. Figure 1.26 shows the variation of h_{FE} with temperature for the 2N525 and indicates that at −50°C the value of h_{FE}

drops to about 65% of its value at 25°C. Most germanium and silicon transistors show approximately this variation of h_{FE} and h_{fe} with temperature. In the design of transistor circuits, the decrease of h_{FE} and h_{fe}, and the increase of V_{BE} (see Figure 4.2) at the lower temperatures must be accounted for to guarantee reliable circuit operation. This is discussed in Chapter 6.

Variation of reverse leakage I_{CBO} with temperature has already been discussed under Leakage. Further and more specific information will be found in Chapters 4 and 6. Variation of base-emitter voltage V_{BE} with temperature is covered in Chapter 4 and illustrated in Figure 4.2.

THERMAL SPECTRUM

Figure 1.27 illustrates a portion of the thermal spectrum. Comparison temperature scales appear in degrees Centigrade and degrees Fahrenheit. The illustration is attempting to show, in pictorial terms, the present semiconductor storage, operating, and circuit design limits, and compare these limits with other known points throughout the temperature spectrum.

Melting point temperatures of a variety of metals used in semiconductor manufacture are also included, as well as prime semiconductor materials, germanium and silicon. Many other materials important to semiconductor manufacture do not appear because of space limitations.

Shaded areas point up the three generally accepted semiconductor circuit application categories: *entertainment*, *industrial*, and *military*. All overlap to some degree depending on individual circuit design specifications; and in some instances circuit applications from an "outer" category will fall within a less severe "inner" category.

In any circuit application involving semiconductors, consideration of temperature is vital. As previously mentioned, reliable operation of a transistor over a wide temperature range requires that bias voltage and current remain reasonably stable. At the outset of any circuit design a temperature range should be chosen over which the circuit must reliably function. If the circuit is to be used in an electronic musical instrument for home entertainment, for example, temperature limits from 0°C to 55°C should more than suffice. This range allows some safety factor to insure against severe temperature ambients that might occur. It would be required, from the standpoint of reliability, that as temperature changed, circuit parameters such as frequency, gain, power, distortion, etc., would not shift from a specified design center by more than some allowed amount (% tolerance). Knowing his design centers, and ambient temperature limits, the designer is then faced with selecting semiconductor devices, associated circuit components, and a circuit design to meet the requirements. Figure 1.27 shows, that should the application fall within an "inner" category either germanium or silicon transistors could be used. If temperature limits are increased, reliability would be more difficult to "design in" with germanium devices. In this case either more stringent circuit techniques must be called on, or lower leakage silicon devices used.

TRANSISTOR ABUSES

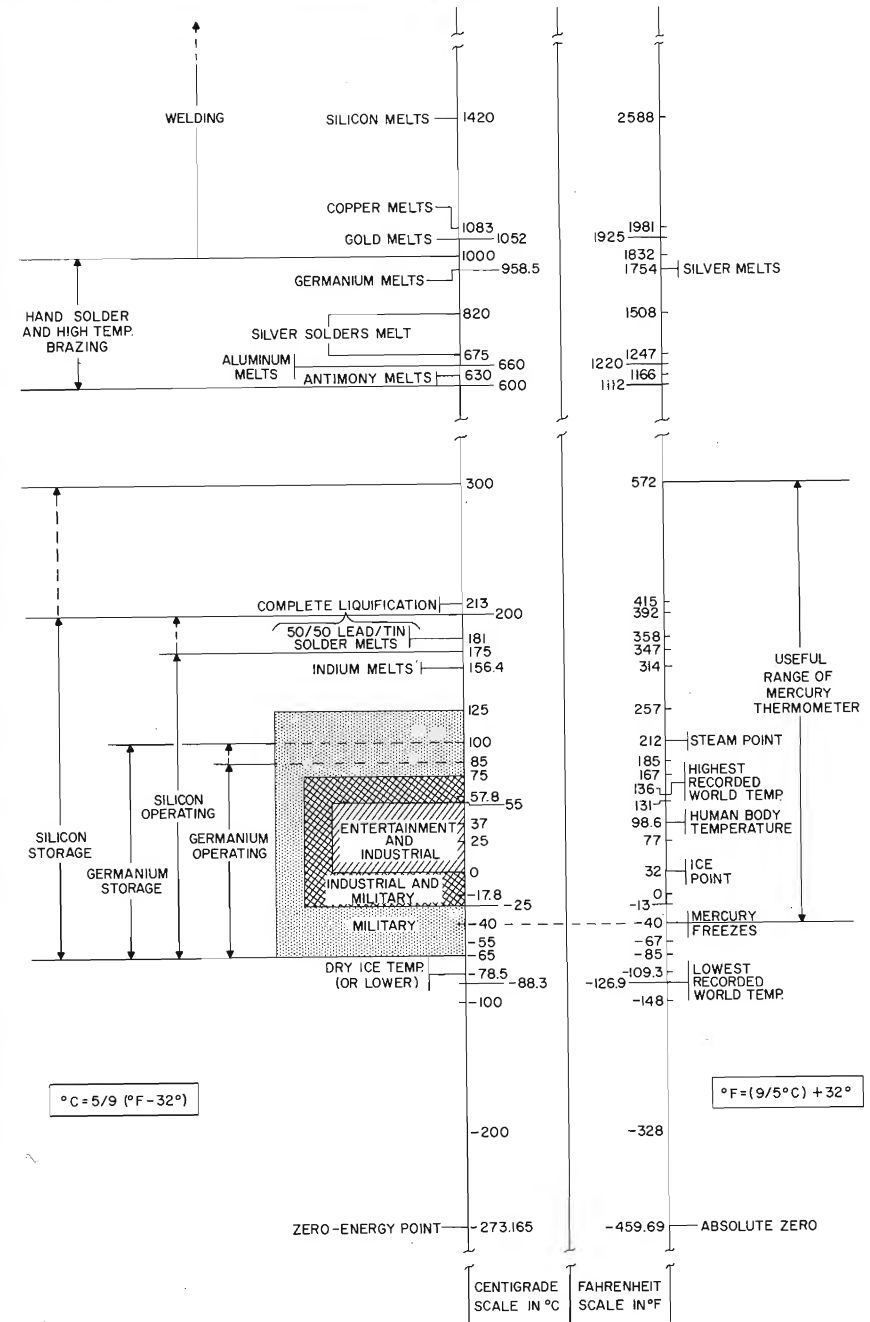
A manufacturer publishes a transistor specification sheet (Chapter 19) not only to describe his devices, but more importantly, to warn the user of its *limitations*. Naturally, in publishing *his device specification* the manufacturer assumes the user to be somewhat familiar with the type of device described as well as the area of its application. Where this knowledge is known to be lacking, additional information in the form of application notes, technical tips, article publication in technical periodicals, promotion material, manuals, and other sundry bits of educational material is usually prepared.

THERMAL SPECTRUM

Figure 1.27

It scarcely needs mentioning, however, that the manufacturer, no matter how carefully he prepares his specification sheet, cannot guarantee his device against handling abuses. Such abuses fall under two main headings: mechanical and electrical.

Over the years transistors have acquired the reputation for being highly reliable and rugged. Continuous reliability studies substantiate this built-in "toughness" – up to a point. It is these "points" or limitations that the designer must become familiar with if he is to design reliable semiconductor circuits.

Following are some of the more common handling abuses that transistors are subjected to.

MECHANICAL

Dropping – Semiconductor material is hard and brittle and can be damaged by high impact shock. For example, dropping a transistor 4½" onto a hardwood bench subjects the device to around 500g; a drop of 30" onto concrete may increase the impact shock from 7000 to 20,000g; snapping a transistor into a clip causes a shock of 600g; and the simple act of clipping a transistor's lead may generate a shock wave of several thousand g. Any high impact shock, therefore, can cause fracture of the semiconductor material, or lead breakage, resulting in complete ruin of the transistor.

Lead Bending – Several sharp back and forth bends of a wire will usually cause it to break, or at least fracture. This is especially true of transistor leads at the point where they enter, or attach to, the header. Some leads when bent during testing and handling may easily break later since the "bending life" of the lead has already been spent. Plated leads when subjected to excessive bending and twisting can generate cracks at the header; such cracks offer openings for moisture to enter and contaminate the device thereby causing gradual degradation of gain and voltage characteristics. To insure against the foregoing it is always well to remember: allow at least 3⁄32" to ⅛" clearance between the header and the start of a lead bend.

Overheating – If, during soldering, the maximum specified junction temperature of a device is exceeded, the device can be destroyed. Heat transmitted over connecting leads and printed circuit board leads to the header can also be destructive. Junctions can be shorted. Lead connections may open. Unequal expansion between header and package may break the hermetic seal. Safety precautions include: removal of the transistor from the immediate socket to which heat is being applied, keeping in mind that the heat can quickly travel along connecting wires to neighboring sockets; use heat shunts (clips, pliers, etc.) connected between the heat source and the device; and, a soldering iron of adequate heat delivery for the job to be done. Most small-signal transistor circuit work can be accomplished by use of a 20 to 50 watt iron. Larger irons can be used, of course, with increased chance of device damage. At any rate, it is always best to "heat shunt" to insure against damage. And, solder cleanly and quickly.

Ultrasonic Cleaning – Depending on the frequency of the cleaning apparatus, sympathetic vibration can induce unusually high stresses into transistor leads. Lead breakage occurring at a particular frequency range can cause internal opens. Where ultrasonic cleaning of transistorized equipment is being considered, the maximum average PSI (pounds per square inch) level in the tank when cleaning action is taking place should be determined.

In most cases, an average level of 3 PSI will adequately clean most equipment without damaging the semiconductors; energy levels exceeding this value tend to induce damage, especially to semiconductors fabricated by germanium techniques (alloy, grown junction, mesa). PSI level can be somewhat increased for equipment using transistors fabricated by the latest silicon planar techniques. Close monitoring of PSI energy level is always good practice, in any case.

ELECTRICAL

Excessive Voltage – Absolutely do not exceed the absolute maximum voltages (usually specified at 25°C) as given by the manufacturer. In signal amplifier circuits this means peak-to-peak voltage swings should not exceed the transistor's inter-element absolute maximum voltages. A good rule is to use a supply voltage equal to half the maximum voltage rating. Maximum inter-element voltages can also be exceeded by voltage transients (inductive or capacitive kicks, etc.) when connecting a transistor into a "hot" circuit; when removing or replacing a transistor in a circuit it is always safest to turn the power off first. Transistor testing by use of an ohmmeter can also cause damage by application of excessive voltage. Since the emitter-base reverse breakdown voltage for most transistors is from 1 to 5 volts, the transistor can easily be damaged when subjected to the high voltage (many ohmmeters use 22½ volt batteries) ranges of an ohmmeter. When measuring breakdown voltage, always use a current limiting resistor. Voltage spikes can cause a build-up of impurities concentrated at a point in the collector and emitter junctions and can result in *punch-through* (internal short from collector to emitter) across the base region.

Excessive Power – Exceeding the maximum junction temperature of a transistor can permanently change the gain, the breakdown voltage, and can cause opens and shorts in the transistor. To guard against such damage, when testing for gain at excessive power dissipation levels, use a protective heat sink or test with a low duty cycle pulse.

Miscellaneous – When a transistor is used in the common emitter configuration, opening the base lead while voltages are still applied can result in junction heating, thermal-run-away, and eventual burn-up of the transistor. The right conditions of applied voltage, current gain and reverse leakage can be destructive, particularly to germanium transistors where leakage currents may be a 1000 or more times greater than in silicon. With the base disconnected, collector-to-emitter leakage (I_{CEO}, base open) equals the collector-to-base leakage (I_{CBO}, emitter open) magnified by the transistor's forward current gain (β). High values of I_{CEO} can flow when inductive collector loads, exhibiting low resistance paths, are part of the associated circuitry. Where current limiting is not a part of the external circuitry, supply power should be disconnected whenever the base is opened circuited.

SOME THINGS TO REMEMBER IN THE APPLICATION OF TRANSISTORS

AGING

Allow sufficient latitude in circuit design to accommodate some change in transistor's parameters with time. This is particularly important in high reliability circuit design.

CURRENT

Generally, above a few milliamperes current *gain* decreases as operating current increases (see Figure 6.7).

Limit collector current (I_C) so that maximum power dissipation will not be exceeded.

Limit collector current (I_C) in breadboards by using a resistor or a fuse.

FREQUENCY

$f_{MAX.}$, the maximum frequency of oscillation, is the upper frequency limit of operation of a transistor.

Frequency cutoff for CE or CC circuits depends on forward current gain. ($f_{hfe} = f_{hfb}/h_{fe}$).

Collector capacitance (C_{ob}, C_{oe}) contributes to poor transistor high frequency response.

Collector capacitance varies inversely as $1/VC^2$ for alloy devices and as $1/VC^3$ for diffused devices (mesa, planar, etc.).

Transistor rise time (t_r) and fall time (t_f) are dependent on the base control charge required to cause the transistor to conduct, as well as upon the currents driving the transistor into or out of saturation.

Fall time (t_f) is also limited by barrier capacitance (C_C).
To *minimize* storage and fall time, do not overdrive the transistor or let it saturate.

To eliminate oscillations in narrow band amplifiers, neutralize the transistors or load down the tank circuits sufficiently.

LEAKAGE

Leakage currents increase exponentially with temperature (double every 8°C to 10°C of temperature increase).

In switching circuits, remember that both the collector and the emitter leakage currents flow in the base lead.

In common emitter circuits, I_{CE} can vary from I_{CBO} to $h_{FE} \times I_{CBO}$.

Beware of unstable leakage currents at fixed temperature and voltage, due most likely to contamination.

Minimize circuit resistance between base and emitter consistent with stage gain.

MANUFACTURING RATINGS

Compare ratings of different manufacturers of same transistor type number when considering second source or replacement.

Apply derating factors to the manufacturer's ratings to insure reliable circuit operation.

MECHANICAL

Use heat shunts when soldering.

Do not connect or disconnect transistors with power on.

Do not use an ohmmeter for checking transistors unless a "safe" voltage/current range is used.

Keep sharp lead bends at least 3⁄32" to 1⁄8" away from the transistor body (header).

POWER

Do not store transistors at a temperature higher than the maximum rated junction temperature as specified by the manufacturer.

Use a thermal derating factor for temperatures above 25°C.

Use the *proper* thermal derating factor for small signal transistors; this is about 1 — 10 mw/°C. For power transistors .25 — 1.5 W/°C.

Thermal resistance (R_T, Θ_R) given by the manufacturer does not include the heat sink thermal resistance.

In a switching circuit, the *peak* power during the transition should not be excessive.

Limit collector power dissipation to avoid thermal runaway (use of emitter resistance helps).

Maximum power dissipation is not always dependent on the device; the circuit (or system) may limit the maximum power at which a device may be operated.

TEMPERATURE

Limit maximum junction temperature to prevent excessive leakage currents.

Limit minimum junction temperature to minimize effects due to V_{BE} variation (negative temperature coefficient of 2 mv/°C for both germanium and silicon).

Choose low values of stability factors. For example, use some emitter resistance to improve stability. Also, keep the base-emitter shunting resistance in common-emitter circuits as low as gain considerations will permit.

Choose large values of collector current (I_C) to minimize the effect of ΔI_C due to temperature changes.

Use low values of source resistance driving the base circuit to keep the stability factor low.

Stabilize emitter current by using a large value of emitter resistance or by using a constant current supply source.

For large temperature changes, the use of a differential amplifier will reduce the effects of ΔV_{BE}.

When using diodes and transistors in a temperature compensation circuit, use a common heat sink for all devices.

Design for minimum h_{FE} over the operating temperature range.

Low stability factor does not improve a dc amplifier's performance.

VOLTAGE

Do not exceed V_{CB} maximum.

Do not exceed V_{BE} maximum (reverse breakdown voltage).

Do not exceed V_{CE} maximum.

Minimize circuit resistance between base and emitter.

In push-pull applications, keep $V_{CC} < 1/2\ V_{CB}$.

Minimize transient voltages in circuitry.

Reverse breakdown of silicon decreases with increasing temperatures.

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NOTES

SMALL-SIGNAL CHARACTERISTICS

Part 1 – Low Frequency Considerations

INTRODUCTION

The transistor, like the vacuum tube, is a non-linear device and since it is capable of gain, it can be defined as a *non-linear active device.*

Figure 2.1 illustrates that although slightly non-linear throughout its range, the transistor's non-linearities become very pronounced at the very low and very high current and voltage levels (below point A and above point B). Hence if, for example, an ac signal is applied to the base of a transistor in the absence of any dc bias, conduction would take place only during one half cycle of the applied signal and the amplified signal would be highly distorted. To avoid this problem, a dc bias operating point OP is chosen (see Figure 2.1 and Chapter 4 on Biasing). This bias moves the transistor's operation to the more linear portion of its characteristics. There the linearity, although not perfect, is acceptable, resulting in amplification with low signal distortion.

The application of a dc bias, in itself, is still not sufficient. A transistor could be biased right squarely in the middle of its linear range and be operated at such large signal swings (see Figure 2.1) that the signal encroaches upon the non-linear part of the characteristics, resulting in increased distortion once more. This is quite common, for example, in class A audio output (or driver) stages of radio or television receivers where normal signal levels make the transistor operate linearly, but higher volume music passages such as crescendos, fortissimos . . . tv commercials . . . may drive the transistor into cut-off and/or saturation. This would, of course, result in severe *clipping distortion.*

In a great number of transistor applications, normal operating signal levels are small. Examples of such applications are the RF and most IF amplifier stages of radar, radio, and television receivers. Even after detection, as in audio or servo preamplifiers, signal levels can be moderate.

In low-level stages, signal swings run from less than 1 μv to about 10 mv under normal operating conditions (for which these stages are generally designed). Therefore it is important to analyze the transistor under conditions when the *bias is such that the largest ac signal to be amplified is small compared to the dc bias current and voltage.* The transistor is then said to be operating in the *small-signal mode.* Transistors used in this way are normally biased at currents between 0.1 and 10 ma and voltages between 2 and 10 volts. Insufficient biases can cause distortion while excessive biases exhibit unnecessarily increased power dissipation and higher noise figures (the latter is primarily important in input stages). If the bias is sufficiently increased to make the stage operate in the high voltage non-linear region, distortion will once again be increased.

A simple analysis of transistors under large signal conditions requires a great deal of approximations. More accurate analysis is mathematically complex as one deals with non-linear equations. The restriction to small signal levels, will lead to more accurate equivalent circuits composed of linear circuit elements and internal linear generators. This allows the analyst the use of conventional linear-circuit analysis.

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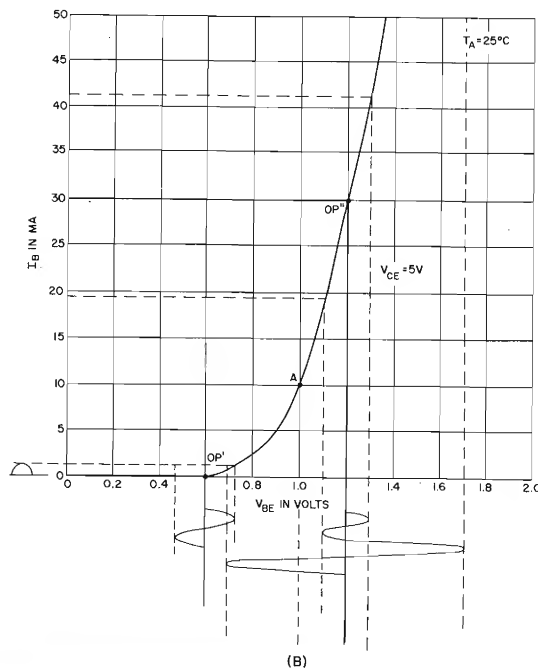
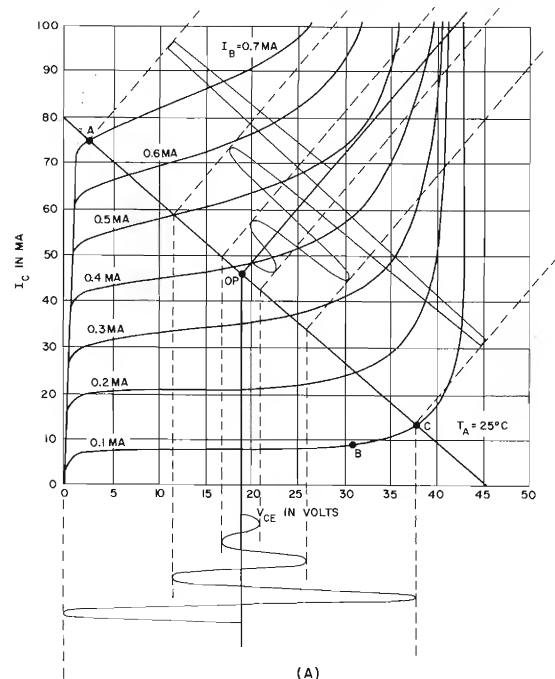
TYPICAL VI CHARACTERISTICS OF THE SILICON PLANAR 2N1613

Figure 2.1

TRANSISTOR LOW FREQUENCY EQUIVALENT CIRCUITS

There are three major approaches to the choice of equivalent circuits. First the device designer wants a circuit which he can simply relate to the device physics. Then there is the device manufacturer who wants to use an equivalent circuit whose parameters can be easily and inexpensively measured and controlled in the manufacturing process. The third party to this plot is the circuits engineer who must handle this equivalent circuit continually and who wants to use parameters fitting conveniently into his circuit design. These parameters should be easy to measure and, if possible, readily obtainable from the commonly used graphical characteristics. He is also interested in controls and limits to those parameters relating directly to his circuit's performance.

As a result of these varying interests several equivalent circuits have been developed over the years. Some of these have retained their importance in modern transistor circuits analysis, others have become less used and will only be mentioned for academic reasons. The important thing is that every one of the equivalent circuits must fully describe and accurately synthesize the device it represents.

Before getting into the discussion on the various equivalent circuits, it should be remembered that all equivalent circuits have three useful connections; i.e., common base, common emitter and common collector (see Chapter 1).

GENERIC EQUIVALENT CIRCUIT[1]

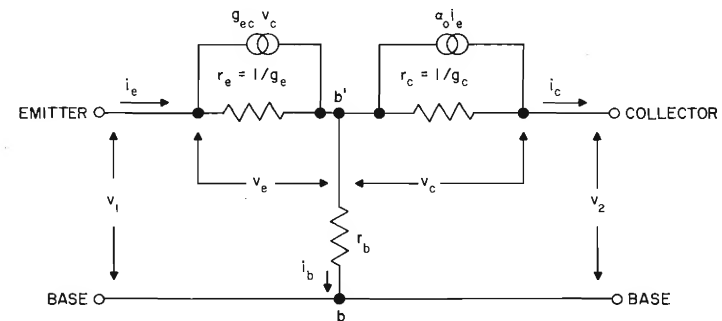
The device designer looks at the transistor from a physical mechanism viewpoint. The circuit engineer also finds an understanding of these basic mechanisms of great help, at least in the early stages of his circuit design work. The *generic* equivalent circuit is a circuit composed of parameters identified with the basic transistor mechanism and have been expressed in terms of the physical attributes of the device at a given bias point and ambient temperature.

GENERIC EQUIVALENT CIRCUIT

Figure 2.2

Emitter Diffusion Resistance, r_e

To relate the current and voltage of the emitter junction one can define a small-signal emitter resistance, r_e. This relationship is nonlinear and is expressed as a partial derivative with the collector voltage held constant. Thus,

$$r_e = \left[\frac{dV_e}{dI_e}\right] V_{c\ constant} = \frac{1}{g_e}$$

This small signal emitter resistance turns out to be proportional to the dc value of the

emitter current and is given by

$$r_e = \frac{KT}{qI_E m}$$

where T is the absolute temperature in degrees Kelvin ($T = °C + 273$), hence T is about 300 at room temperature; K is Boltzmann's constant (1.38×10^{-23} watt-sec/°C), and q is the charge of an electron (1.60×10^{-19} coulomb). m is a constant whose value is 1 for germanium and varies between 1 and 2 for silicon transistors.[2] Hence, $r_e \cong 26/I_E$ (I_E expressed in milliamperes) for a germanium transistor; which makes $r_e = 26$ ohms at 1.0 ma, for example. One can thus see that r_e changes with the dc bias operating point and the ambient temperature.

Base Resistance, r_b

The flow of current from the base terminal to the active region of the transistor is by majority carriers (electrons). These electrons flow by the drift process, so that there is an ohmic drop associated with this current. The resulting resistance is defined as the base resistance, r_b. The geometry of this base current path (base resistance), is very complex and can differ radically from one transistor structure to another.

Practically, this base resistance causes a power loss and a feedback path when the base is common to input and output. It will be seen later in the high frequency equivalent circuit analysis that since this resistance denies direct access to the *intrinsic* base point b′ (in Figure 2.2), it also obstructs efforts to accomplish broad-band neutralization. The base resistance also varies somewhat with temperature and bias.

Collector Resistance, r_c

The small-signal collector resistance, r_c, can be defined as the ac slope of the reverse biased collector junction at a particular voltage. This gives us

$$r_c = \left[\frac{dV_c}{dI_c}\right] I_{e\ constant} = \frac{1}{g_c}$$

This collector resistance is generally very high, in excess of 1 megohm, and is primarily sensitive to bias.

Emitter Feedback Conductance, g_{ec}

This feedback conductance results from the fact, that an increase in collector voltage results in an increase in emitter current even though the emitter voltage is held constant. The physical cause of this is the *base-widening* effect.[3][4] Schematically this is represented as a small-signal current generator across the emitter junction. The value of this current generator is proportional to the small-signal collector voltage, and since it relates current to voltage, it will have the dimension of transconductance, where

$$g_{ec} = \left[\frac{dI_e}{dV_c}\right] V_{e\ constant}$$

Current Amplification Factor, α

The cumulative effect of three basic mechanisms, emitter efficiency, transport factor, and collector efficiency results in the current amplification factor, α (see Chapter 1).

The relationship is

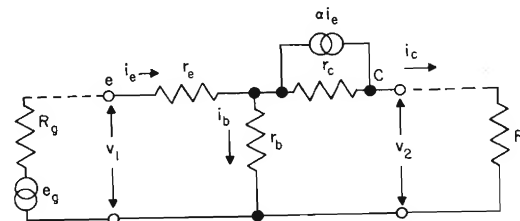
$$\alpha = \left[\frac{dI_c}{dI_e}\right] V_{c\ constant}$$

This α varies with dc emitter current and collector voltage and generally has values slightly smaller than unity. It is another parameter sensitive to bias and temperature changes.

The first disadvantage of the *generic* equivalent circuit is that the use of the feed-

back generator $g_{ec}v_c$ is a poor choice since v_c is not obtainable at the external terminals of the transistor. Another disadvantage of this equivalent circuit is that it has two current generators which essentially present two extra circuit meshes to our analysis.

T-Equivalent Circuit (tee)

This circuit has found widespread use in the literature due to its greater simplicity. It still maintains close touch with the physical transistor mechanisms and is easily analyzed. One schematic representation of the T-equivalent circuit is shown in Figure 2.3.

T-EQUIVALENT CIRCUIT (COMMON-BASE) WITH CURRENT GENERATOR
Figure 2.3

This particular representation has a current generator (αi_e) in the collector circuit. Although this current generator is in fact a third mesh, this circuit is relatively simple and has the advantage of great resemblance to the physical mechanism. The elements which comprise this circuit are identified with the branch of the circuit in which they are located. Thus here again we find a base resistance r_b, an emitter resistance r_e and a collector resistance r_c. It would be very confusing to identify these terms by other than these characteristic symbols. It must be understood, however, that these T-equivalent terms and the symbols used for the generic or any other equivalent circuit are *not at all* the same resistances. This is a very important factor and must be thoroughly understood to avoid ghastly confusion. To understand these differences, let us rigorously analyze both the generic and the T-equivalent circuits by writing their mesh equations and equating corresponding coefficients.

For the generic circuit shown in Figure 2.2, $v_c = (\alpha_o i_e - i_c) r_c$ and hence we have

$$i_e (r_e + r_b + g_{ec} r_e r_c \alpha_o) + i_c (- r_b - g_{ec} r_e r_c) = v_1$$
$$i_e (r_b + \alpha_o r_c) + i_c (- r_b - r_c) = v_2$$

For the T-equivalent circuit in Figure 2.3, we have

$$i_e (r_e + r_b) + i_c (- r_b) = v_1$$
$$i_e (r_b + \alpha r_c) + i_c (- r_c - r_b) = v_2$$

Equating corresponding coefficients we obtain the following relationship between the T-equivalent parameters and their generic counterparts.

$$r_b\ (\text{tee}) = r_b + g_{ec} r_e r_c$$
$$r_e\ (\text{tee}) = r_e - g_{ec} r_e r_c (1 - \alpha_o)$$
$$r_c\ (\text{tee}) = r_c (1 - g_{ec} r_e)$$
$$\alpha\ (\text{tee}) = \frac{\alpha_o - g_{ec} r_e}{1 - g_{ec} r_e}$$

By carefully defined valid approximations, the following simplifications can be made: first, in a good transistor α_o is close to unity. We can thus define a new param-

eter, beta (β), such that

$$\beta = \frac{1}{\Delta} = \frac{1}{1 - \alpha_o}$$

(The present standard terminology defines β as h_{fe} and α as h_{fb}).

If $g_{ec} = \frac{g_e}{2\Delta} = \frac{1}{2\Delta r_c}$

then $g_{ec}\, r_c = \frac{1}{2\Delta} = \frac{\beta}{2} = \frac{h_{fe}}{2}$

and $g_{ec}\, r_e = \frac{\beta r_e}{2 r_c} = \frac{h_{fe}\, r_e}{2 r_c}$

A typical value of the parameter β is approximately 50, corresponding to an alpha (α_o) of 0.98. The emitter resistance r_e is rarely greater than 100 ($r_e \cong 26/I_E$, hence above 0.25 ma r_e will be less than 100 ohms). The collector resistance r_c is usually very large, in the order of one or more megohms. Hence, we can further approximate

$$g_{ec}\, r_e << 1$$

Finally with these approximations, the simplified, yet sufficiently accurate tee-equivalent parameters can be expressed as follows in terms of their generic counterparts:

$$r_b\,(\text{tee}) = r_b + \frac{\beta r_e}{2}$$

$$r_e\,(\text{tee}) = \frac{r_e}{2}$$

$$r_c\,(\text{tee}) = r_c$$

$$\alpha\,(\text{tee}) = \alpha_o$$

It is important to note that the base resistance r_b in the tee-equivalent circuit is the sum of the extrinsic base resistance and Early's feedback term.[3] [4] Extrinsic base resistance is generally of the order of several hundred ohms. The feedback term for high alpha transistors may be several thousand ohms and dominates this expression. Thus the r_b of the tee-equivalent circuit does not reliably reflect the physical base resistance value. Let us demonstrate this by a practical example of a typical PNP germanium alloy junction transistor operated at a collector voltage of 5 volts, a collector current of 1 ma, and at an ambient temperature of 25°C. The generic parameters of this unit are

$r_e = \frac{KT}{qI_E} = 25$ ohms (r_e here is the diffusion resistance)

$r_b = 250$ ohms (r_b here is r_b', the base spreading resistance)

$r_c = 2$ megohms

$h_{fbo} = \alpha_o = 0.98$ hence

$$h_{fe} = \frac{1}{1 - h_{fbo}} = \frac{1}{1 - 0.98} = 50$$

The equivalent *tee-parameters* of this same transistor are

$r_e \cong \frac{25}{2} \cong 12.5$ ohms $h_{fb} \cong 0.98$ (r_e here is the "tee-equivalent emitter resistance")

$r_c \cong 2.0$ megohms $h_{fe} \cong 50$

$r_b \cong 250 + \frac{25 \times 50}{2} \cong 875$ ohms   (r_b here is the "tee-equivalent base resistance")

As one can plainly see there is very little resemblance between the generic r_b of 250 ohms and the tee-equivalent value of 875 ohms.

The main shortcomings of both the generic and the tee equivalent circuits are

that their elements are difficult, in some cases even impossible to measure directly. The electrical engineer then resorts to another analytical concept, consisting of measuring and analyzing the black-box parameters of the device, which avoids having to use any of the *internal* parameters.

"BLACK-BOX ANALYSIS" OF THE FOUR-TERMINAL LINEAR NETWORK

This concept consists of analyzing a device (or an entire circuit and/or a system) by writing two simultaneous equations expressing the input and output voltages in terms of the input and output currents. If the equations relating these currents and voltage are known, everything that is needed in a linear network calculation can be determined from them.

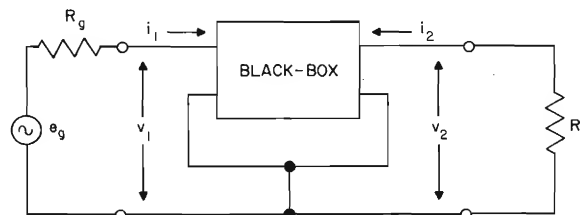
The transistor is a three-terminal device. One of these terminals will be used as common, the other two as input and output. In view of the wealth of information available on the analysis of four-terminal devices, however, (i.e., one pair of input and one pair of output terminals) it is more convenient to analyze the transistor as a *four-terminal* device. Figure 2.4 illustrates that the three-terminal network is just a special case of the four-terminal network, in which the common terminal serves in both the input and output portions of the circuit.

FOUR-TERMINAL LINEAR NETWORK REPRESENTATION OF THE TRANSISTOR (A THREE-TERMINAL DEVICE)

Figure 2.4

OPEN CIRCUIT IMPEDANCE PARAMETERS (z-PARAMETERS)

The generalized equations for the input and output voltages of a *black-box* are

$$v_1 = i_1 z_{11} + i_2 z_{12}$$

$$v_2 = i_1 z_{21} + i_2 z_{22} \qquad (2a)$$

The open circuit impedance parameters, by definition, require that to measure z_{11} and z_{21}, the output be open-circuited; while for the measurement of z_{12} and z_{22}, the input be open-circuited. Hence one can see that for the open-circuited output case, where $i_2 = 0$

$$z_{11} = \frac{v_1}{i_1} = \text{input impedance}$$

and

$$z_{21} = \frac{v_2}{i_1} = \text{forward transfer impedance}$$

while for the open-circuited input case, where $i_1 = 0$,

$$z_{12} = \frac{v_1}{i_2} = \text{reverse transfer impedance}$$

and

$$z_{22} = \frac{v_2}{i_2} = \text{output impedance}$$

The input and output currents in this case are independent variables.

All electrical properties, such as current gain, voltage gain, power gain, etc., can be calculated from these impedance parameters. The current gain A_i, for example, is given by

$$A_i = \frac{i_2}{i_1}.$$

From equation (2a) it can be seen that $v_2 = i_1 z_{21} + i_2 z_{22}$. Figure 2.4 shows that v_2 also equals

$$v_2 = -i_2 R_L$$

hence

$$-i_2 R_L = i_1 z_{21} + i_2 z_{22}$$

and

$$A_i = \frac{i_2}{i_1} = \frac{z_{21}}{z_{22} + R_L}$$

The z-parameters prove most useful to describe low impedance devices and/or circuits. This is mainly due to the fact that when measuring high impedances, one's test equipment must present ultra-high impedances to the device under test in order not to load it down. Hence for a low to medium impedance "to be measured" (up to several thousand ohms) a one megohm driving impedance can synthesize a virtual open-circuit. Another difficulty in the z-parameter measurement is that at higher frequencies a true open circuit becomes even more difficult to achieve due to device, as well as stray test circuit, capacitances.

SHORT CIRCUIT ADMITTANCE PARAMETERS (y-PARAMETERS)

The generalized equations for the input and output currents of the black-box are

$$i_1 = v_1 y_{11} + v_2 y_{12} \qquad (2b)$$
$$i_2 = v_1 y_{21} + v_2 y_{22}$$

where v_1 and v_2 are independent variables. Since these equations describe the short-circuit admittance parameters it suffices to short-circuit the output ($v_2 = 0$) in order to measure y_{11} and y_{21}. Thus

$$y_{11} = \frac{i_1}{v_1} = \text{input admittance}$$

and

$$y_{21} = \frac{i_2}{v_1} = \text{forward transfer admittance.}$$

To measure the output parameters, it suffices to short-circuit the input ($v_1 = 0$). Hence

$$y_{12} = \frac{i_1}{v_2} = \text{reverse transfer admittance}$$

and

$$y_{22} = \frac{i_2}{v_2} = \text{output admittance.} \qquad (2c)$$

Once again, knowing these parameters, all other electrical properties of the black-box can be derived. The y-parameters prove most useful to describe high impedance devices and/or circuits. This is due to the fact that it is easier to virtually short-circuit a high impedance circuit than a low impedance one. It must be realized that when one talks of open-circuit or short-circuit that this is only true with respect to ac signal frequencies, and that the necessity of applying dc biases prevents the application of

actual physical short or open circuits.

In general, since the transistor turns out to exhibit low input impedances and high output impedances, the use of z and y parameters becomes awkward, especially at high frequencies. As a result the *hybrid*, or *h*, parameters have been found to provide the most useful tool in modern transistor circuit analysis. This is primarily due to the fact that the h parameters are a combination of impedance and admittance parameters ideally fitting the low input and high output impedances of the modern transistor. As a result they are also the easiest parameters to measure at both low and high frequencies. Another advantage is that the h_{11}, h_{21}, and h_{22} terms approximate the actual typical operating conditions even though the latter do not occur with either input or output terminals shorted or open. (See Figures 2.8 and 2.9). For the h-parameters, the black-box equations read

$$v_1 = i_1 h_{11} + v_2 h_{12}$$
$$i_2 = i_1 h_{21} + v_2 h_{22}.$$

Hence when the output is short-circuited, ($v_2 = 0$),

$$h_{11} = \frac{v_1}{i_1} = \text{input impedance,} \qquad (2d)$$

and

$$h_{21} = \frac{i_2}{i_1} = \text{forward transfer current ratio;} \qquad (2e)$$

and with an open-circuited input circuit, ($i_1 = 0$),

$$h_{12} = \frac{v_1}{v_2} = \text{reverse transfer voltage ratio,}$$

and

$$h_{22} = \frac{i_2}{v_2} = \text{output admittance.}$$

When going from the general four-terminal analysis to the specific transistor parameter work, it is usual to drop numeric subscripts such as h_{11}, h_{12}, h_{21}, and h_{22} in favor of more descriptive letter subscripts. Therefore it has become customary for the first subscript letter to indicate whether the particular parameter is an input, output, forward transfer, or reverse transfer parameter; while the second subscript describes the transistor configuration. We will therefore refer to the common-emitter h-parameters as

h_{ie} = common-emitter input impedance
h_{fe} = common-emitter forward current transfer ratio
h_{re} = common-emitter reverse voltage transfer ratio
h_{oe} = common-emitter output admittance.

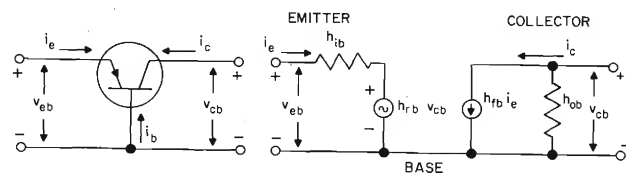
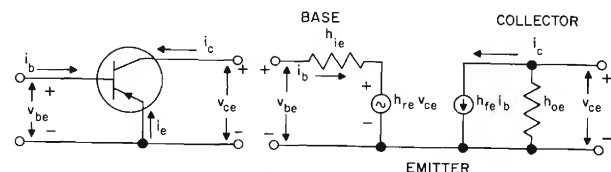
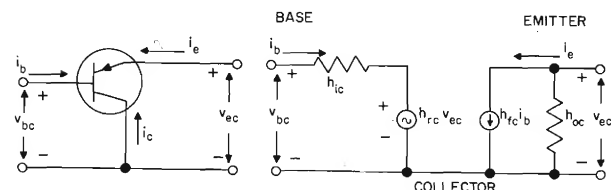
For the common-base parameters, these will be referred to as h_{ib}, h_{fb}, h_{rb}, and h_{ob}; while the common-collector parameters will be h_{ic}, h_{fc}, h_{rc}, and h_{oc}.

h-PARAMETER EQUIVALENT CIRCUIT

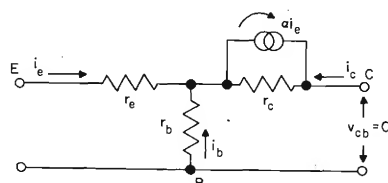
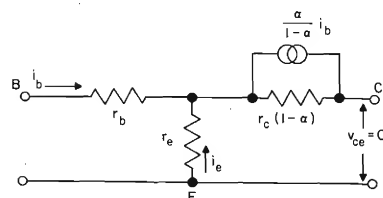
From the h-parameter equations, one can derive three equivalent circuits. See Figure 2.5 (A), (B) and (C).

T-EQUIVALENT CIRCUIT

Another useful equivalent circuit capable of describing the h-parameters is the *tee-equivalent* which enables one to get a physical picture of the inside of the black-box. In our previous discussion we saw that the tee-equivalent had certain shortcomings. The main one was described as caused by the feedback term which made the r_b and r_e terms look considerably different than their physical values. This is due to *space charge layer widening* as explained by Early.[3][4]

In the h-parameter analysis, however, the output circuit is short circuited ($v_2 = 0$, see equations (2d) and (2e)). In this *specific instance*, then, the feedback term dis-

(A)-COMMON-BASE

(B)-COMMON-EMITTER

(C)-COMMON-COLLECTOR

HYBRID-EQUIVALENT CIRCUITS

Figure 2.5

(A)-COMMON-BASE

(B)-COMMON-EMITTER

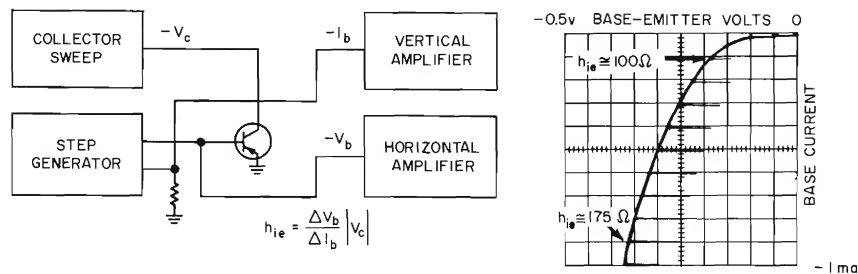
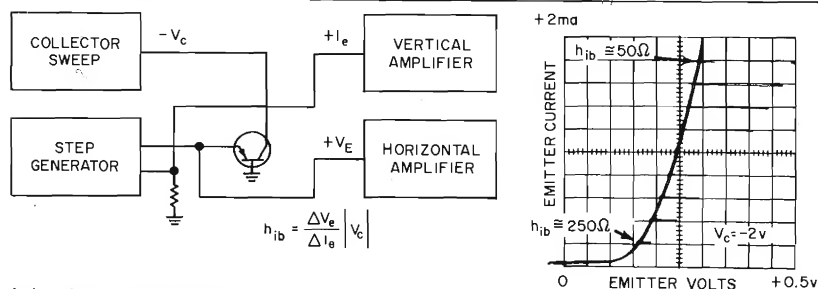
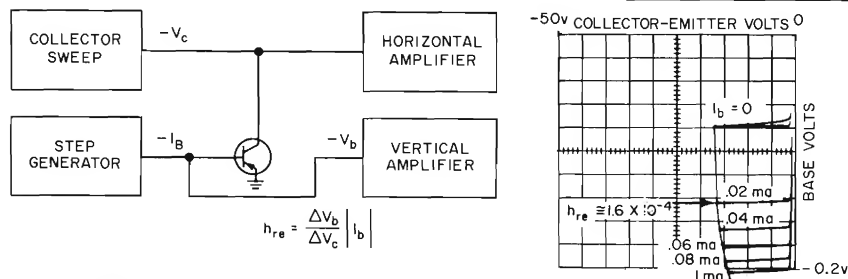
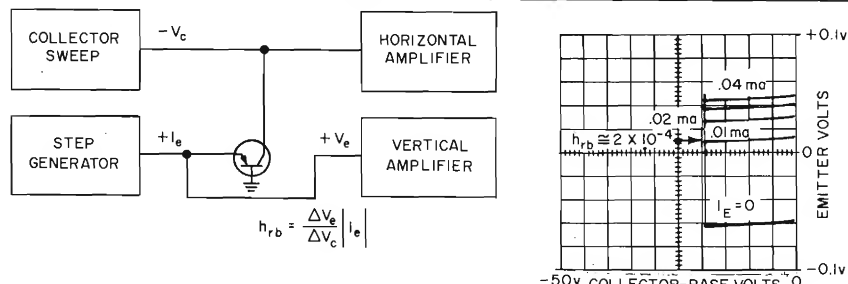
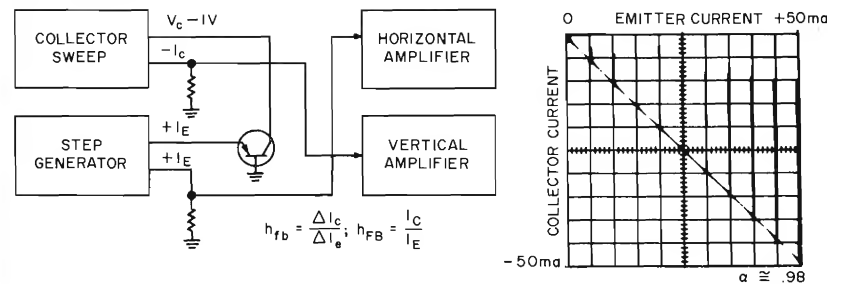
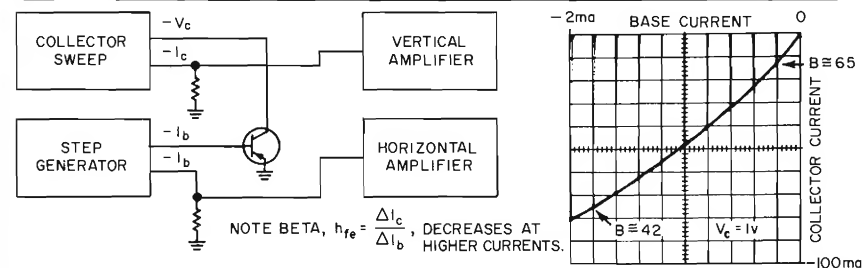
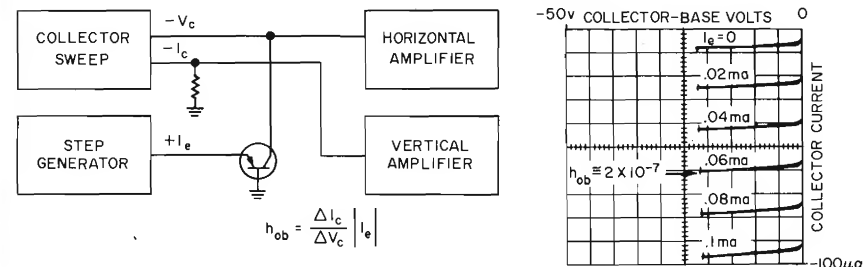
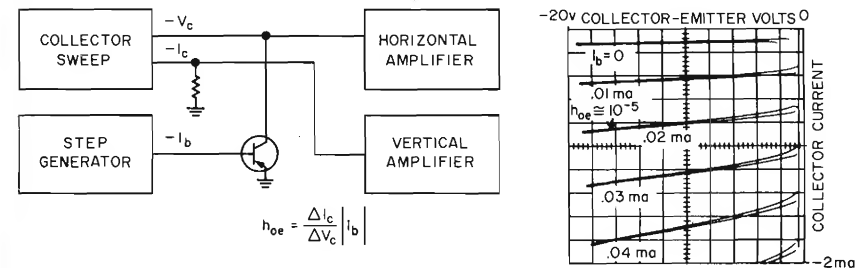
T-EQUIVALENT CIRCUITS

Figure 2.6

(NUMERICAL VALUES ARE TYPICAL FOR THE 2N525 AT 1 MA, 5V)

SYMBOLS IRE	SYMBOLS OTHER	COMMON EMITTER	COMMON BASE	COMMON COLLECTOR	T EQUIVALENT CIRCUIT (APPROXIMATE)
h_{ie}	$h_{11e}, \frac{1}{Y_{11e}}$	1400 OHMS	$\frac{h_{ib}}{1+h_{fb}}$	h_{ic}	$r_b + \frac{r_e}{1-\alpha}$
h_{re}	$h_{12e}, \mu_{bc}, \mu_{re}$	3.37 X 10^{-4}	$\frac{h_{ib} h_{ob}}{1+h_{fb}} - h_{rb}$	$1 - h_{rc}$	$\frac{r_e}{(1-\alpha) r_c}$
h_{fe}	h_{21e}, β	44	$-\frac{h_{fb}}{1+h_{fb}}$	$-(1+h_{fc})$	$\frac{\alpha}{1-\alpha}$
h_{oe}	$h_{22e}, \frac{1}{Z_{22e}}$	27 X 10^{-6} MHOS	$\frac{h_{ob}}{1+h_{fb}}$	h_{oc}	$\frac{1}{(1-\alpha) r_c}$
h_{ib}	$h_{11}, \frac{1}{Y_{11}}$	$\frac{h_{ie}}{1+h_{fe}}$	31 OHMS	$-\frac{h_{ic}}{h_{fc}}$	$r_e + (1-\alpha) r_b$
h_{rb}	$h_{12}, \mu_{ec}, \mu_{rb}$	$\frac{h_{ie} h_{oe}}{1+h_{fe}} - h_{re}$	5 X 10^{-4}	$h_{rc} - 1 - \frac{h_{ic} h_{oc}}{h_{fc}}$	$\frac{r_b}{r_c}$
h_{fb}	h_{21}, α	$-\frac{h_{fe}}{1+h_{fe}}$	−0.978	$-\frac{1+h_{fc}}{h_{fc}}$	$-\alpha$
h_{ob}	$h_{22}, \frac{1}{Z_{22}}$	$\frac{h_{oe}}{1+h_{fe}}$	0.60 X 10^{-6} MHOS	$-\frac{h_{oc}}{h_{fc}}$	$\frac{1}{r_c}$
h_{ic}	$h_{11c}, \frac{1}{Y_{11c}}$	h_{ie}	$\frac{h_{ib}}{1+h_{fb}}$	1400 OHMS	$r_b + \frac{r_e}{1-\alpha}$
h_{rc}	$h_{12c}, \mu_{be}, \mu_{rc}$	$1 - h_{re}$	1	1.00	$1 - \frac{r_e}{(1-\alpha) r_c}$
h_{fc}	h_{21c}, α_{eb}	$-(1+h_{fe})$	$-\frac{1}{1+h_{fb}}$	−45	$-\frac{1}{1-\alpha}$
h_{oc}	$h_{22c}, \frac{1}{Z_{22c}}$	h_{oe}	$\frac{h_{ob}}{1+h_{fb}}$	27 X 10^{-6} MHOS	$\frac{1}{(1-\alpha) r_c}$
α		$\frac{h_{fe}}{1+h_{fe}}$	$-h_{fb}$	$\frac{1+h_{fc}}{h_{fc}}$	0.978
r_c		$\frac{1+h_{fe}}{h_{oe}}$	$\frac{1-h_{rb}}{h_{ob}}$	$-\frac{h_{fc}}{h_{oc}}$	1.67 MEG
r_e		$\frac{h_{re}}{h_{oe}}$	$h_{ib} - \frac{h_{rb}}{h_{ob}}(1+h_{fb})$	$\frac{1-h_{rc}}{h_{oc}}$	12.5 OHMS
r_b		$h_{ie} - \frac{h_{re}}{h_{oe}}(1+h_{fe})$	$\frac{h_{rb}}{h_{ob}}$	$h_{ic} + \frac{h_{fc}}{h_{oc}}(1-h_{rc})$	840 OHMS

APPROXIMATE CONVERSION FORMULAE h-PARAMETERS AND T-EQUIVALENT CIRCUIT

Figure 2.7

(A) INPUT IMPEDANCE, h_{11e}, h_{ie}

(B) INPUT IMPEDANCE, h_{11b}, h_{ib}

(C) VOLTAGE FEEDBACK RATIO, h_{12e}, h_{re}

(D) VOLTAGE FEEDBACK RATIO, h_{12b}, h_{rb}

(E) ALPHA CURVE, α, h_{21b}, h_{fb}, h_{FB}

(F) FORWARD CURRENT TRANSFER RATIO, BETA, β, h_{21e}, h_{fe}, h_{FE}

(G) OUTPUT ADMITTANCE, h_{22b}, h_{ob}

(H) OUTPUT ADMITTANCE, h_{22e}, h_{oe}

(Courtesy of Tektronix, Inc.)

Figure 2.8 h-PARAMETERS AS OBTAINED ON TEKTRONIX MODEL 575 CURVE TRACER

appears and the tee-equivalent parameters are equal to those of the physical circuit. Hence in the circuits of Figure 2.6(A) and (B)

Alpha (α) is the fraction of the emitter current that becomes the collector current and is typically 0.90-0.999.

r_e is the incremental diffusion resistance of the forward biased emitter-to-base diode: $r_e \cong KT/qI_E \cong 26/I_E$ at room temperature.

r_b is the ohmic resistance of the base contact plus that of the active base region.

r_c is the incremental resistance of the reversed biased collector junction.

The common-base and common-emitter tee-equivalent circuits are shown in Figure 2.6(A) and (B).

The table in Figure 2.7 gives the equations as well as numerical values for the h-parameters of a typical transistor in the three configurations. This table also gives approximate conversion formulae between h-equivalent and T-equivalent parameters.

Figures 2.8(A) through 2.8(H) illustrate the graphical data of the h-parameters as obtained on the Tektronix 575 Transistor Curve Tracer.

Knowing any one set of established parameters, the others may be worked out, or more conveniently, obtained from Figure 2.9.

MATRIX INTERRELATIONS

Figure 2.9

TO ↓ / FROM →	[z]	[y]	[h]	[g]	[a]
[z]	$\begin{matrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{matrix}$	$\begin{matrix} \frac{y_{22}}{\Delta^y} & \frac{-y_{12}}{\Delta^y} \\ \frac{-y_{21}}{\Delta^y} & \frac{y_{11}}{\Delta^y} \end{matrix}$	$\begin{matrix} \frac{\Delta^h}{h_{22}} & \frac{h_{12}}{h_{22}} \\ \frac{-h_{21}}{h_{22}} & \frac{1}{h_{22}} \end{matrix}$	$\begin{matrix} \frac{1}{g_{11}} & \frac{-g_{12}}{g_{11}} \\ \frac{g_{21}}{g_{11}} & \frac{\Delta^g}{g_{11}} \end{matrix}$	$\begin{matrix} \frac{a_{11}}{a_{21}} & \frac{\Delta^a}{a_{21}} \\ \frac{1}{a_{21}} & \frac{a_{22}}{a_{21}} \end{matrix}$
[y]	$\begin{matrix} \frac{z_{22}}{\Delta^z} & \frac{-z_{12}}{\Delta^z} \\ \frac{-z_{21}}{\Delta^z} & \frac{z_{11}}{\Delta^z} \end{matrix}$	$\begin{matrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{matrix}$	$\begin{matrix} \frac{1}{h_{11}} & \frac{-h_{12}}{h_{11}} \\ \frac{h_{21}}{h_{11}} & \frac{\Delta^h}{h_{11}} \end{matrix}$	$\begin{matrix} \frac{\Delta^g}{g_{22}} & \frac{g_{12}}{g_{22}} \\ \frac{-g_{21}}{g_{22}} & \frac{1}{g_{22}} \end{matrix}$	$\begin{matrix} \frac{a_{22}}{a_{12}} & \frac{-\Delta^a}{a_{12}} \\ \frac{-1}{a_{12}} & \frac{a_{11}}{a_{12}} \end{matrix}$
[h]	$\begin{matrix} \frac{\Delta^z}{z_{22}} & \frac{z_{12}}{z_{22}} \\ \frac{-z_{21}}{z_{22}} & \frac{1}{z_{22}} \end{matrix}$	$\begin{matrix} \frac{1}{y_{11}} & \frac{-y_{12}}{y_{11}} \\ \frac{y_{21}}{y_{11}} & \frac{\Delta^y}{y_{11}} \end{matrix}$	$\begin{matrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{matrix}$	$\begin{matrix} \frac{g_{22}}{\Delta^g} & \frac{-g_{12}}{\Delta^g} \\ \frac{-g_{21}}{\Delta^g} & \frac{g_{11}}{\Delta^g} \end{matrix}$	$\begin{matrix} \frac{a_{12}}{a_{22}} & \frac{\Delta^a}{a_{22}} \\ \frac{-1}{a_{22}} & \frac{a_{21}}{a_{22}} \end{matrix}$
[g]	$\begin{matrix} \frac{1}{z_{11}} & \frac{-z_{12}}{z_{11}} \\ \frac{z_{21}}{z_{11}} & \frac{\Delta^z}{z_{11}} \end{matrix}$	$\begin{matrix} \frac{\Delta^y}{y_{22}} & \frac{y_{12}}{y_{22}} \\ \frac{-y_{21}}{y_{22}} & \frac{1}{y_{22}} \end{matrix}$	$\begin{matrix} \frac{h_{22}}{\Delta^h} & \frac{-h_{12}}{\Delta^h} \\ \frac{-h_{21}}{\Delta^h} & \frac{h_{11}}{\Delta^h} \end{matrix}$	$\begin{matrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{matrix}$	$\begin{matrix} \frac{a_{21}}{a_{11}} & \frac{-\Delta^a}{a_{11}} \\ \frac{1}{a_{11}} & \frac{a_{12}}{a_{11}} \end{matrix}$
[a]	$\begin{matrix} \frac{z_{11}}{z_{21}} & \frac{\Delta^z}{z_{21}} \\ \frac{1}{z_{21}} & \frac{z_{22}}{z_{21}} \end{matrix}$	$\begin{matrix} \frac{-y_{22}}{y_{21}} & \frac{-1}{y_{21}} \\ \frac{-\Delta^y}{y_{21}} & \frac{-y_{11}}{y_{21}} \end{matrix}$	$\begin{matrix} \frac{-\Delta^h}{h_{21}} & \frac{-h_{11}}{h_{21}} \\ \frac{-h_{22}}{h_{21}} & \frac{-1}{h_{21}} \end{matrix}$	$\begin{matrix} \frac{1}{g_{21}} & \frac{g_{22}}{g_{21}} \\ \frac{g_{11}}{g_{21}} & \frac{\Delta^g}{g_{21}} \end{matrix}$	$\begin{matrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{matrix}$

NOTE: Δ REPRESENTS THE DETERMINANT ($\Delta_Z = Z_{11} Z_{22} - Z_{21} Z_{12}$)

BASIC AMPLIFIER STAGE

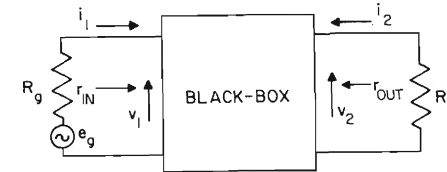
How do the actual dynamic transistor parameters such as r_{IN}, r_{OUT}, A_i, A_v, PG, etc., relate to the h-parameter measurements? Well, of course, when the source and load terminations simulate those of the measurement conditions of the h-parameters then $r_{IN} = h_{11}$, $r_{OUT} = 1/h_{22}$, etc. Figure 2.10 illustrates the black-box of a basic amplifier stage.

BLACK-BOX REPRESENTATION OF BASIC AMPLIFIER CIRCUIT

Figure 2.10

To keep this analysis general, in order to be able to apply it to all three transistor configurations we return to the use of h-parameters with numeric subscripts.

It has already been established that when $R_L = 0$ (short circuited output) the input resistance $r_{IN} = h_{11}$. For high values of load resistance, however, h_{11} can be significantly different than r_{IN} as can be seen by Figure 2.11. This follows from a matrix analysis of the h-parameters[5] which result in the following equations:

$$r_{IN} = \frac{(h_{11} + \Delta^h R_L)}{(1 + h_{22} R_L)} \qquad (2f)$$

$$r_{OUT} = \frac{(h^{11} + R_g)}{(\Delta^h + h_{22} R_g)}$$

$$A_i = \frac{i_2}{i_1} = \frac{h_{21}}{(1 + h_{22} R_L)}$$

$$PG = \left(\frac{i_2}{i_1}\right)^2 \left(\frac{R_L}{r_{IN}}\right) = \frac{h_{21}^2 R_L}{(1 + h_{22} R_L)(h_{11} + \Delta^h R_L)}$$

where

Δ^h is the determinant of h, $\Delta^h = (h_{11} h_{22} - h_{21} h_{12})$

INPUT RESISTANCE (r_{IN})

Figure 2.11 shows that for high values of load resistance ($R_L/r_e > 1$)

$$r_{IN} = h_{11} - \left(\frac{h_{12} h_{21}}{h_{22}}\right).$$

In terms of tee-parameters $r_{IN} = r_b + r_e \cong r_b$.

In the common-base and common-collector configurations, the input impedance increases for increasing R_L due to negative values of h_{21b} (h_{fb}) and h_{21c} (h_{fc}) as opposed to positive values for h_{21e} (h_{fe}).

OUTPUT RESISTANCE (r_{OUT})

Similarly, for high values of source resistance it has previously been established that the output admittance is equal to the h-parameter value of h_{22}, hence when

$$R_g \cong \infty,$$

$$r_{OUT} = \frac{1}{h_{22}}$$

But for low values of source resistance, when

$R_g \cong 0,$

$$r_{OUT} = \frac{h_{11}}{\Delta h} = \frac{1}{h_{22} - \left(\frac{h_{12}\,h_{21}}{h_{11}}\right)}$$

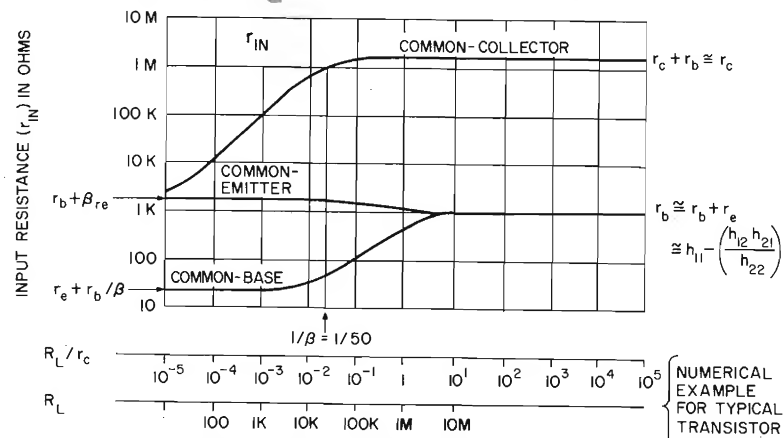
Figure 2.12 illustrates the behavior of r_{OUT} as a function of R_g.

INPUT RESISTANCE AS A FUNCTION OF LOAD RESISTANCE

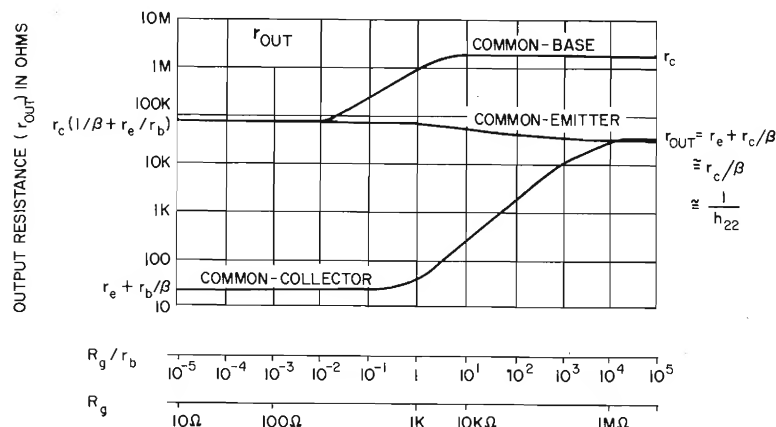
Figure 2.11

OUTPUT RESISTANCE AS A FUNCTION OF SOURCE RESISTANCE

Figure 2.12

As the source resistance is increased the output resistance (r_{OUT}) goes towards its *open-circuited-input* value of $1/h_{22}$. For low source resistances, the common-base and common-emitter values of r_{OUT} are identical and equal to $r_c\,(1/\beta + r_e/r_b)$. It should be noted, once again, that when departing from the h-parameter test conditions which stipulate that the output be short-circuited with respect to signal ($R_L = 0$), and the

input be open-circuited with respect to signal ($R_g = \infty$), the tee-equivalent values of r_b, r_e, and r_c (see limit conditions on Figures 2.11 and 2.12) are definitely affected by Early's feedback term and hence are not the generic values.

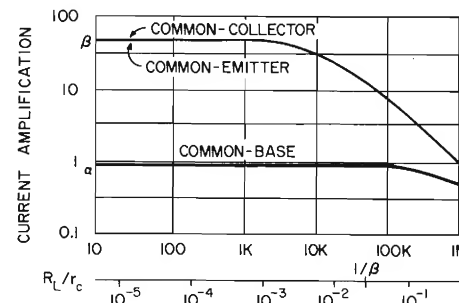
One other very important factor to note from these figures is that both the input and output resistances vary the least when the transistor is used in the common-emitter configuration.

CURRENT AMPLIFICATION VS. LOAD RESISTANCE

Figure 2.13

CURRENT AMPLIFICATION (A_i)

The forward current transfer ratio with the output short-circuited ($R_L = 0$) is

$$A_i = h_{21} = \frac{i_2}{i_1}$$

At the other extreme, when $R_L = \infty$, $i_2 = 0$ and the current amplification factor or *forward current transfer ratio*, as it is more exactly defined, is equal to zero. Figure 2.13 shows the typical behavior of A_i with variations of load resistance.

From Figure 2.13 it can be seen that the current amplification A_i is equal to beta (β) in both the common-emitter and common-collector configurations up to the point when R_L becomes comparable to r_c/β. The only difference is that their sign is different, as the common-emitter configuration does not exhibit a phase reversal between the input and output currents, hence we have $A_i = +h_{fe}$. In the common-collector configuration $A_i = -h_{fc}$, while in the common-base configuration $A_i = -h_{fb}$.

VOLTAGE AMPLIFICATION (A_v)

The voltage amplification factor for both the common-base and common-emitter configuration is about the same and is equal to r_c/r_b for high values of load resistance (see Figure 2.14). In the common-collector configuration, $A_v \cong 1$.

MAXIMUM POWER GAIN

It is obvious that no power gain can be obtained in either the open or short-circuited conditions, as either the input or output power would be zero. Hence there exists a maximum value of power gain, which is given by

$$PG_{MAX} = \frac{h_{21}^2}{(\sqrt{h_{11}\,h_{22}} + \sqrt{\Delta^h})^2}$$

at a value of R_L given by

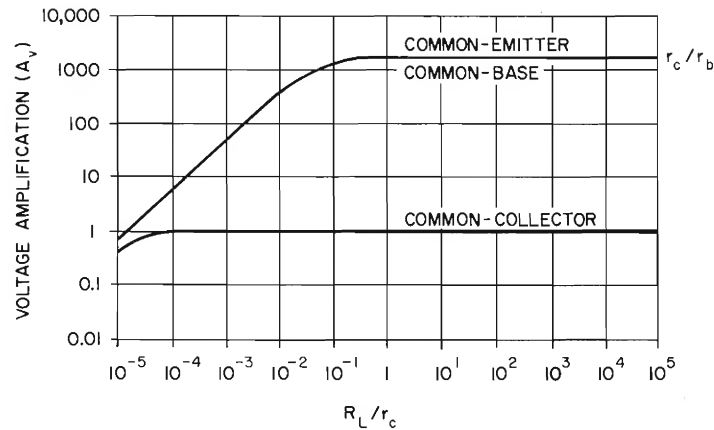
$$R_L = \sqrt{\frac{h_{11}}{h_{22}\,\Delta^h}}$$

VOLTAGE AMPLIFICATION FACTOR (A_v) AS A FUNCTION OF R_L

Figure 2.14

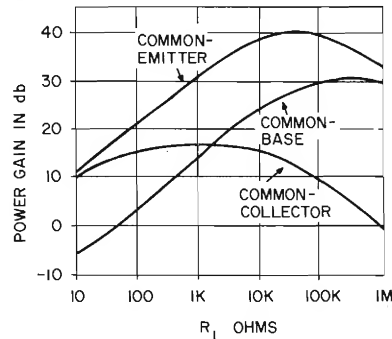
Figure 2.15 illustrates the behavior of a typical transistor. One can plainly see that the highest gain configuration is the common-emitter, with common-base second, and common-collector the lowest. It is also apparent that the power gain optimizes at different values of load resistance (R_L) for the three configurations.

POWER GAIN VS. LOAD RESISTANCE

Figure 2.15

TRANSDUCER GAIN

This gain is defined as the ratio of the output power to the maximum power available from the source. Thus it is a very useful figure of merit for specific source and load resistance conditions. The transducer gain is

$$TG = \frac{i^2 R_L}{e_g^2/4R_g} = \frac{4i_2^2 R_L R_g}{(v_1 + i_1 R_g)^2} = \frac{4A_i^2 R_L R_g}{(r_{IN} + R_g)^2} \qquad (2g)$$

ELECTRICAL PROPERTY	COMMON-EMITTER (CE)	COMMON-BASE (CB)	COMMON-COLLECTOR (CC)
R_L OPT	$\sqrt{h_{ie}/h_{oe}\Delta^h_e} = 47\ K\Omega$	$\sqrt{h_{ib}/h_{ob}\Delta^h_b} = 322\ K\Omega$	$\sqrt{h_{ic}/h_{oc}\Delta^h_c} = 1075\ \Omega$
Δ_h	$h_{ie}h_{oe} - h_{fe}h_{re} = 23 \times 10^{-3}$	$h_{ib}h_{ob} - (-h_{fb})h_{rb} = 5 \times 10^{-4}$	$h_{ic}h_{oc} - (-h_{fc})h_{rc} = -45$
r_{IN}	$\frac{h_{ie} + \Delta^h_e R_L}{1 + h_{oe}R_L} = 1100\ \Omega$	$\frac{h_{ib} + \Delta^h_b R_L}{1 + h_{ob}R_L} = 160\ \Omega$	$\frac{h_{ic} + \Delta^h_c R_L}{1 + h_{oc}R_L} = 48.5\ K\Omega$
r_{OUT}	$\frac{h_{ie} + R_g}{\Delta^h_e + h_{oe}R_g} = 47\ K\Omega$	$\frac{h_{ib} + R_g}{\Delta^h_b + h_{ob}R_g} = 322\ K\Omega$	$\frac{h_{ic} + R_g}{\Delta^h_c + h_{oc}R_g} = 1050\ \Omega$
A_i	$\frac{h_{fe}}{1 + h_{oe}R_L} = 19.5$	$\frac{(-h_{fb})}{1 + h_{ob}R_L} = -0.82$	$\frac{(-h_{fc})}{1 + h_{oc}R_L} = -43.8$
MPG	$\frac{h_{fe}^2 R_L}{(1 + h_{oe}R_L)(h_{ie} + \Delta^h_e R_L)} = 42\ db$	$\frac{(-h_{fb})^2 R_L}{(1 + h_{ob}R_L)(h_{ib} + \Delta^h_b R_L)} = 31.4\ db$	$\frac{(-h_{fc})^2 R_L}{(1 + h_{oc}R_L)(h_{ic} + \Delta^h_c R_L)} = 16.3\ db$

PROPERTIES OF THE IMAGE-MATCHED CONDITION

Figure 2.16

MAXIMUM POWER GAIN (MPG)

From equation (2g) it becomes apparent that there are optimum values of source and load resistances for which maximum power gain is obtained. These optimum terminations are found to match the input and output resistances of the transistor. When terminated such that $R_g = r_{IN}$ and $R_L = r_{OUT}$, the transistor is said to be *image-matched,* which is the condition of maximum (low frequency) power gain.

The table in Figure 2.16 gives the equations and typical values to determine such electrical properties as input resistance, output resistance, current gain and maximum power gain in the image-matched condition for the three configurations.

In practical low-frequency applications, the image-matched condition is not used very often as it generally entails the use of input and output matching transformers. In most applications, DC or RC coupling is used because of the lower component cost. This presents the transistor with rather restrictive source and load terminations. Consider a chain of *n*-transistor stages. Since the input impedance of each stage is a function of its load (see equation (2f)), a computation of the input impedance of any one stage would require the computation of the input impedance of all the stages following it. It can be shown, that except for the last few stages, the input impedance of each stage becomes nearly equal to that of the stage preceding it. Such a stage is called an *iterative* stage.

The iterative input impedance may be computed by setting $R_L = r_{IN}$. Note that this condition is virtually equal to the output-short-circuited condition of the h-parameter measurements since the ratio of R_L/r_c is smaller than 1×10^{-3} (see Figure 2.11). Hence our calculations show that

common-emitter input resistance is $r_{INe} \cong h_{ie}$

common-base input resistance is $r_{INb} \cong h_{ib}$

common-collector input resistance is $r_{INc} \cong -h_{fc}/h_{oc}$.

In general, for an *n*-stage amplifier, all but the last stage may be considered iterative for the CE and CB connections, while all but the last two stages of a CC chain are iterative. Since $R_L = r_{IN}$, the iterative power gain is given by

$$PG_{Iterative} = \frac{i_2^2 R_L}{i_1^2 r_{IN}} = \left(\frac{i_2}{i_1}\right)^2 = \frac{h_{21}^2}{(1 + h_{22} R_L)^2}$$

Substituting the iterative input impedance for R_L,

$$PG_{CE\,(Iterative)} \cong (h_{21e})^2 \cong 32.8 \text{ db}$$

$$PG_{CB\,(Iterative)} \cong (h_{21b})^2 \cong 0 \text{ db}$$

$$PG_{CC\,(Iterative)} \cong 1 \cong 0 \text{ db}$$

From the above, it can be concluded that only the common-emitter configuration offers any gain in the iterative amplifier case. The common-base configuration only offers a lower input impedance and higher output impedance, while the common-collector connection offers high input and low output impedances. Hence the latter two connections are rarely used and only in cases where special terminations are of paramount importance. An example design of an image-matched amplifier is illustrated in Figure 2.17.

Resistors R1 and R2 form a bias voltage divider to provide the dc base bias voltage. R3 provides the emitter potential to fix a dc operating point. Since the choice of bias components is the subject of the next chapter we will ignore the dc design considerations here and concern ourselves only with the signal operation of this stage. Hence capacitors C1 and C2 will be considered ac short circuits at all signal frequencies of interest, and points A and B are ac grounds. Transformers T1 and T2 match R_g to r_{IN} and R_L to r_{OUT}, giving us an "image-matched" amplifier. The only discrepancies between the calculated *maximum available power gain* and the gain obtained in

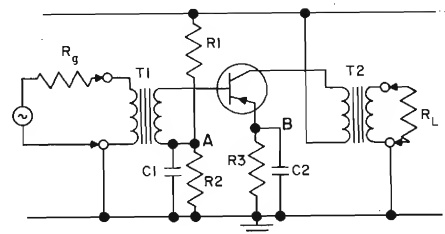



Figure 2.17 EXAMPLE OF IMAGE-MATCHED AMPLIFIER STAGE

this circuit can be found in the transformer insertion losses (efficiencies). Figure 2.16 describes the calculations of the properties of such a stage.

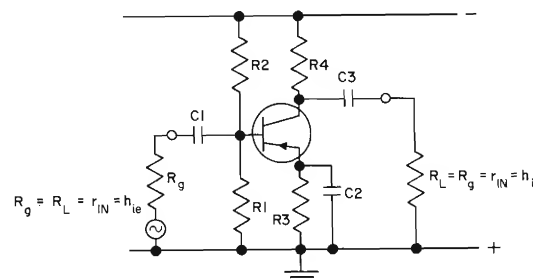



Figure 2.18 EXAMPLE OF ITERATIVE AMPLIFIER STAGE

In the design of an iterative stage (see Figure 2.18), all capacitors are considered ac short circuits again, while resistors R1, R2, R3 and R4 are primarily there to provide a stable dc operating point. Here R_L is equal to the input resistance of the next stage which is identical (by our definition of *iterative*) to that of our example amplifier. The source resistance R_g is equal to the circuit output resistance of the previous stage which again means it is equal to the output resistance of our example. In our iterative stage, the r_{in} is equal to h_{ie} which is typically 1400 ohms. Hence R_L and R_g are also 1400 ohms. Although r_{OUT} here can be calculated (as per Figure 2.16) to be about 45 K, the need to provide a dc collector load resistance (R4) of small enough resistance to stay in the linear bias region makes the effective circuit r_{OUT} equal to R4. Usually this resistance will not be too much larger than h_{ie}. As a result the typical calculated *iterative power gain* of 32.8 db must be adjusted to account for the power losses in R4 (and, of course, the small losses in the dc bias network components).

As might be expected from the earlier discussion, h-parameters vary with operating point. Specification sheets often carry curves showing variation of the small-signal parameters with bias current and voltage. Such curves are shown in Figure 2.19. These are specifically for the 2N525 and are plotted with respect to the values at an operating point defined by a collector potential of 5 volts and an emitter current of 1 ma.

Suppose, for example, the typical value of h_{ob} is required for the 2N525 at $I_e = 0.5$ ma and $V_c = 10$ volts. From Figure 2.7 the typical value of h_{ob} at 1 ma and 5 volts is 0.6×10^{-6} mhos. From Figure 2.19 the correction factor at 0.5 ma is 0.6 and the correction factor at 10 volts is 0.75. Therefore,

$$h_{ob}\,(0.5 \text{ ma, } 10 \text{ volts}) = 0.6 \times 10^{-6} \times 0.6 \times 0.75$$
$$= 0.27 \times 10^{-6} \text{ mhos.}$$

CHARACTERISTICS VS EMITTER CURRENT

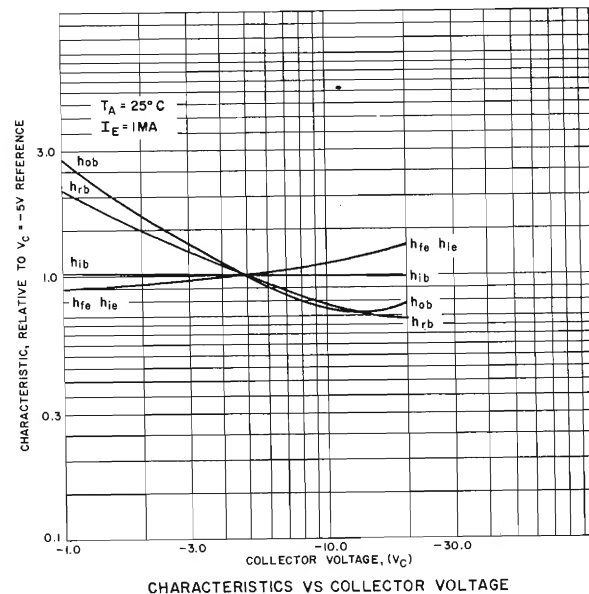
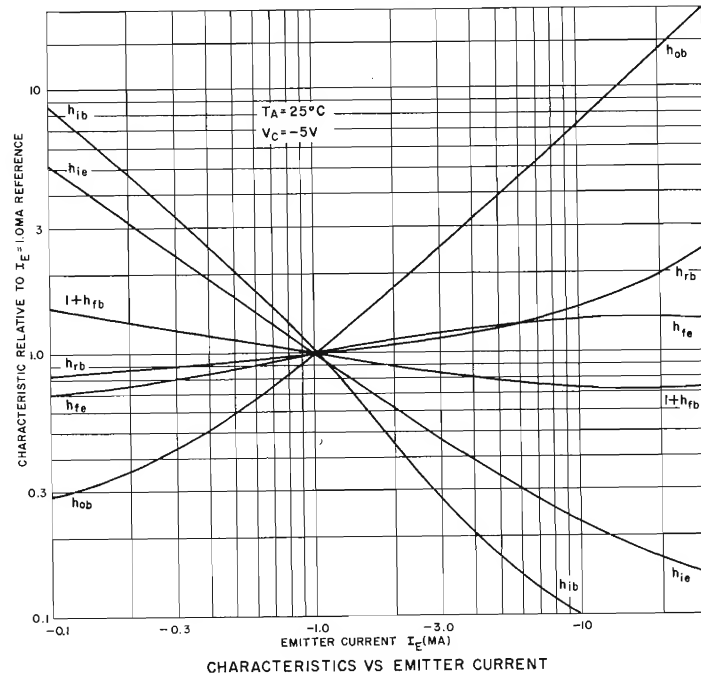
CHARACTERISTICS VS COLLECTOR VOLTAGE

VARIATION OF h-PARAMETERS WITH BIAS CONDITIONS

Figure 2.19

Once the h-parameters are known for the particular bias conditions and configuration being used, the performance of the transistor in an amplifier circuit can be found for any value of source or load impedance.

Figure 2.20 gives the equations for determining the input and output impedances, current, voltage, and power gains of any black-box, including the transistor, when any set of its four-pole parameters (z, y, a, h, or g) are known or have been calculated.

	z	y	h	g	a
Z_i	$\frac{\Delta^z + z_{11} z_l}{z_{22} + z_l}$	$\frac{y_{22} + y_l}{\Delta^y + y_{11} y_l}$	$\frac{\Delta^h + h_{11} y_l}{h_{22} + y_l}$	$\frac{g_{22} + z_l}{\Delta^g + g_{11} z_l}$	$\frac{a_{11} z_l + a_{12}}{a_{21} z_l + a_{22}}$
Z_o	$\frac{\Delta^z + z_{22} z_g}{z_{11} + z_g}$	$\frac{y_{11} + y_g}{\Delta^y + y_{22} y_g}$	$\frac{h_{11} + z_g}{\Delta^h + h_{22} z_g}$	$\frac{\Delta^g + g_{22} y_g}{g_{11} + y_g}$	$\frac{a_{22} z_g + a_{12}}{a_{21} z_g + a_{11}}$
A_v	$\frac{z_{21} z_l}{\Delta^z + z_{11} z_l}$	$\frac{-y_{21}}{y_{22} + y_l}$	$\frac{-h_{21} z_l}{h_{11} + \Delta^h z_l}$	$\frac{g_{21} z_l}{g_{22} + z_l}$	$\frac{z_l}{a_{12} + a_{11} z_l}$
A_i	$\frac{z_{21}}{z_{22} + z_l}$	$\frac{-y_{21} y_l}{\Delta^y + y_{11} y_l}$	$\frac{-h_{21} y_l}{h_{22} + y_l}$	$\frac{g_{21}}{\Delta^g + g_{11} z_l}$	$\frac{1}{a_{22} + a_{21} z_l}$

PROPERTIES OF THE TERMINATED FOUR-TERMINAL NETWORK

Figure 2.20

Part 2 — High Frequency Considerations

ADDITION OF PARASITIC ELEMENTS TO THE LOW-FREQUENCY EQUIVALENT CIRCUITS

JUNCTION CAPACITANCES

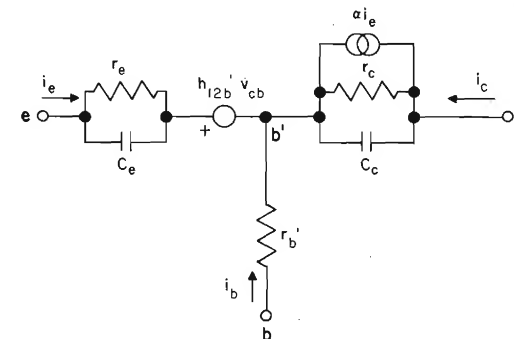
As soon as the transistor is operated outside its low-frequency range (generally above audio frequencies), the presence of reactive components within the transistor becomes apparent. The barrier layers separating the emitter and collector from the base are regions containing strong electric fields. This implies that there are capaci-

TRANSISTOR T-EQUIVALENT CIRCUIT VALID FROM LOW-THROUGH-MEDIUM FREQUENCIES

Figure 2.21

tances associated with these regions. These are identified as barrier capacitances, also sometimes referred to as junction, depletion layer, or transition capacitances (see Chapter 1).

Figure 2.21 illustrates the addition of these capacitances to the low-frequency T-equivalent circuit. The differences between this equivalent circuit and that in Figure 2.3 is that besides adding the junction capacitances C_e and C_c, the base resistance r_b' (from b-b') and the emitter resistance r_e, are the generic values, with Early's feedback term accounted for by the addition of the internal generator h_{22b}' v_{cb}. This manipulation allows us to work with the feedback term independently and know that the emitter diffusion resistance $r_e \cong KT/q I_E$ and $r_b = r_b'$ (the physical value of the base spreading resistance).

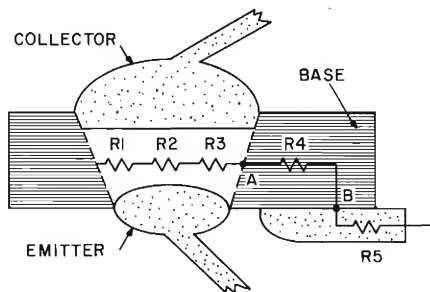
There are actually two types of capacitances associated with any semiconductor junction: *transition capacitance* (C_T) and *diffusion capacitance* (C_D).

Transition capacitance is due to the high electric field in the depletion region caused by the voltage across the barrier. Hence the transition capacitance is voltage dependant. The diffusion capacitance is due to the current flowing through the depletion region. Hence C_D is current dependant. The total junction capacitances (C_e and C_c) are the sum of the transition (C_T) and diffusion (C_D) capacitances.

The collector capacitance C_c is primarily made up of the transition capacitance C_{TC} as the diffusion capacitance is small in a reverse biased junction. The emitter junction, being forward biased, will, on the other hand, primarily consist of the diffusion component.

PARASITIC RESISTANCES

Base Spreading Resistance. r_b'

The active portion of the base region of a transistor is not equipotential, but exhibits an ohmic resistance to the flow of base current. This parasitic resistance is called the *base-spreading resistance*, r_b'. (The term base-spreading resistance is due to the shape of the base of an alloy junction transistor which "spreads out" as one progresses from the center of the junction to the periphery of the transistor).[8] The

NOTE: Although the sheet resistivity is uniform in the base, the width of the base is modulated (Early effect) causing resistance R1, R2, and R3 to become **effectively** non-equal. Resistors R1 and R3 which are on the periphery will be smaller than R2. The sum of R1, R2, and R3 make up actual base spreading resistance r_b'. Resistors R4 (material bulk or sheet resistance) and R5 (base contact resistance) are in series with r_b'. Even though these are extrinsic resistances and are not collector modulated, they are generally considered an integral part of r_b'. It is then convenient to call this term r_{bb}' (total resistance from b to b'). The non-shaded portion of this figure is the active base region.

PHYSICAL DIAGRAM OF ALLOY-JUNCTION TRANSISTOR BASE RESISTANCE

Figure 2.22

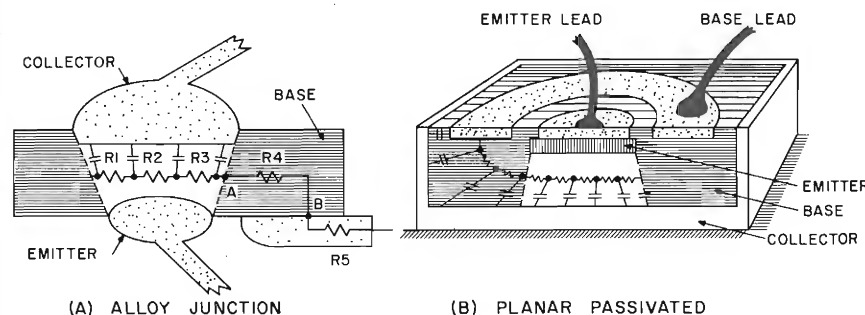
prime in the nomenclature is due to the fact that r_b' is defined as the resistance between the external base contact and point b' (see Figure 2.21) which is a point in the active region of the transistor which cannot be reached. (Sometimes this spreading resistance is also designated as r_{bb}' — or resistance from point b to b'.)

CROSS SECTION VIEWS SHOWING DISTRIBUTED NATURE OF r_b' AND C_c

Figure 2.23

This base resistance is not purely resistive but takes on a distributed form (transmission line) in many transistor structures. (See Figures 2.23 and 2.24.) In general, however, in order not to excessively complicate the analysis, it will be assumed that r_{bb}' is resistive. As will be seen later, r_{bb}' is a most objectionable parameter, since it contributes to the deterioration of transistor performance in many ways.

Leakage Conductance

In all transistors, there exists a certain amount of leakage current from collector to base. This effect can be represented by a corresponding leakage conductance g_{c1} connected in parallel with the collector capacitance. However, this leakage conductance is extremely small for a reliable modern transistor and is therefore generally ignored. At one time this leakage component was actually thought to be the collector conductance g_c. Early [3] suggested, however, that another phenomenon, presently called the *Early-effect, base-width-modulation*, or *space-charge-layer-widening* was the cause of the predominant portion of this collector conductance.

The Early-effect takes place in all transistors because the collector depletion region extends into the base. The depth of this penetration, and hence the base width, depends on the collector voltage. As a matter of fact, if the collector voltage is increased sufficiently the depletion region can penetrate so deeply into the base region as to reach all the way to the emitter causing *punch-through*, a condition describing the fact that there is an effective emitter-collector short-circuit. For small-signal voltages, the effect will not be as drastic, but does cause added complexity in the equivalent circuit. This added complexity was previously illustrated by the differences between the "generic" and "effective" terms of r_e and r_b, or if one wants to avoid confusion, the use of the feedback generator term h_{12}' v_{cb}.

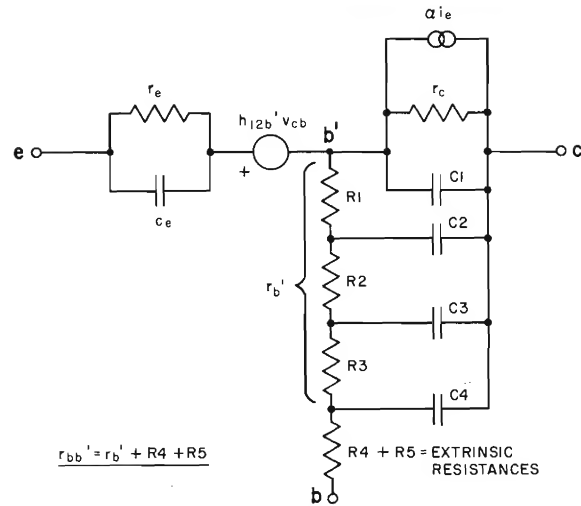
There is also an effect on the collector resistance r_c since the magnitudes of α and β are functions of base width. This base width is effectively modulated by the signal at the collector causing a modulation in the current amplification. Hence the output port of the transistor feeds energy back to the input port and vice-versa, giving us both a capacitive term C_{TC} as well as a resistive term r_c in the collector junction.

EQUIVALENT CIRCUIT WITH DISTRIBUTED r_b'
(ALLOY JUNCTION MODEL)

Figure 2.24

Extrinsic Resistances (r_e', r_b' and r_c')

As can be seen in Figures 2.23 and 2.24 there is some series resistance associated with bringing the active base region out to the transistor's external terminals (leads). In the case of the base resistance in Figure 2.22 it is the sum of R4 and R5; specifically, the sum of the resistances of the semiconductor base bulk-material, the contact resistance at point B, and finally the resistance of the lead itself. The lead resistance will generally be extremely small but both the bulk resistance and the contact resistance can be appreciable. In high frequency transistors, having extremely small junctions, such resistances can be as high as several hundred ohms. Generally such high values are only found in series with the collector junction (*collector saturation resistance*), since the collector region consists of high resistivity material in order to provide reduced capacitance and increased voltage breakdown ratings. In the base and emitter regions this *extrinsic* resistance is minimized by the use of relatively low-resistivity material; hence, here a fraction of one ohm up to a few ohms is more typical.

In general, then, one might be tempted to neglect the *extrinsic* base and emitter resistances. This can lead to serious errors in some transistor structures, however. In some diffused-base transistors the base region is so small that it becomes difficult to make a good, solid electrical contact to it, resulting in an increased r_{bb}'.

In transistors with extremely small geometry, like some UHF transistors, the same problem exists in the emitter contact, hence an increased r_e' occurs. When operated in the common-emitter connection this r_e' acts like an unbypassed (internal) emitter resistance and results in decreased gain and increased noise figure. Figure 2.25 shows these extrinsic resistances in the total equivalent circuit of the transistor. This model consists of the intrinsic* transistor and all extrinsic* elements such as the depletion layer (or transition) capacitances C_{TE} (C_e) and C_{TC} (C_c) as well as contact and bulk resistances such as r_e', r_b' and r_c'.

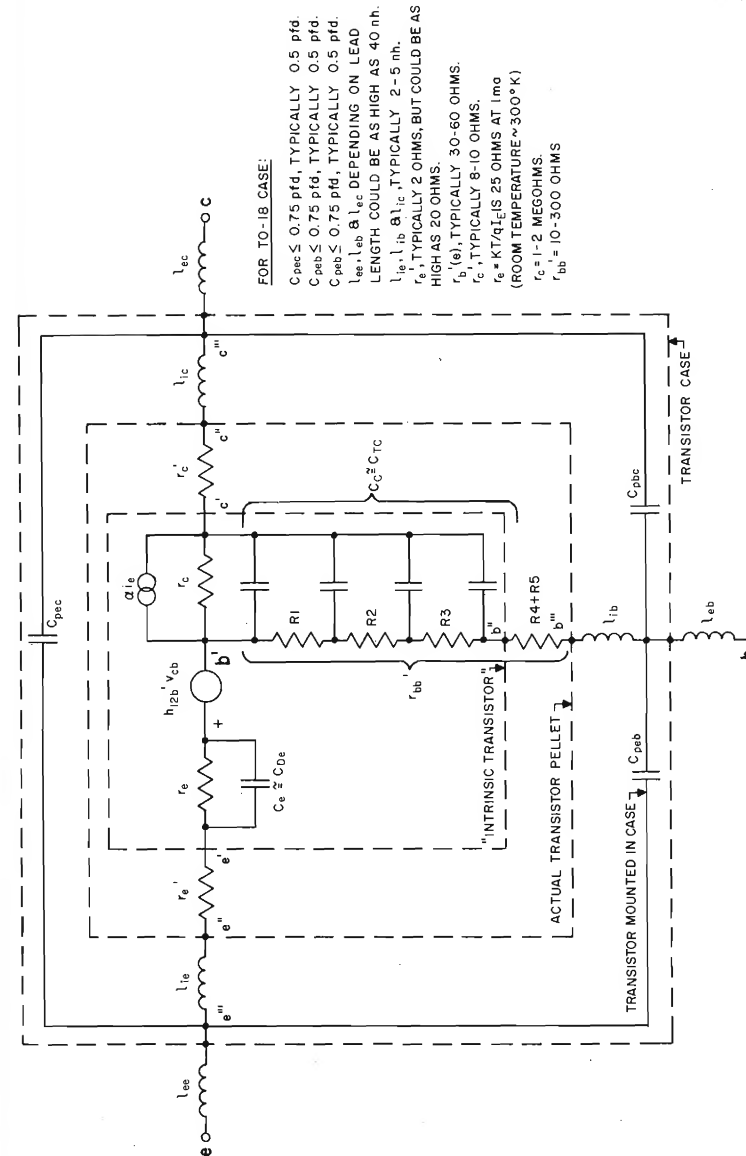
Intrinsic and *extrinsic* are used here in their general meanings as "belonging to" or "not belonging to" the essence of the device.

MODEL OF REASONABLY COMPLETE HIGH FREQUENCY TRANSISTOR WITH TYPICAL VALUES
(IN HF T-EQUIVALENT CIRCUIT)

Figure 2.25

Lead Inductances

Up to this point, one only has the model of the transistor proper before it is placed into a package. Leads must now be used to connect the transistor structure to the header, hence the inclusion of inductances l_{ie}, l_{ib} and l_{ic}. The header itself is generally made of metal with tiny glass-passages for the leads, giving us lead-to-case and lead-to-lead capacitances C_{peb}, C_{pbc} and C_{pec}. Emerging from the transistor case are three leads, which can of course be cut very short to reduce the external lead inductances l_{ec}, l_{eb} and l_{ec}.

As can be imagined, the lead inductances are very small, in the order of a few nanohenries and therefore they only become important for operation in and beyond the VHF band. At and above VHF these inductances act as rf chokes, having appreciable impedance in some cases. For instance, the inductive reactance of 20 nh at 500 mc is in excess of 62 ohms. If this inductance were situated in the emitter lead connection, the effective increase in input impedance, and hence drop in gain, could be appreciable. Let us assume that we operate below 50 mc, however, and that we minimize the external lead inductance of the transistor (while we hope the manufacturer has reduced the internal lead inductances) then all transistor inductances can be neglected in the calculations. Before we attempt to eliminate all stray reactances, however, let us say a word about the stray package capacitances.[7]

Header Capacitances

The TO-18 transistor package, presently extensively used for high frequency transistors, typically exhibits about 0.5 pfd for C_{peb}, C_{pbc} and C_{pec}. If one works with high capacitance transistors, having C_{TE} and C_{TC} in excess of 5 pfd, this does not represent an appreciable amount of added parasitic capacitance. For good high frequency units (VHF and UHF transistors) having only 0.5 — 2 pfd of C_{TE} and C_{TC}, these parasitic capacitances may become excessive. In a common-emitter VHF amplifier, for instance, the collector-to-base package capacitance can add directly to the transition capacitance. This adds feedback to the transistor since it returns a portion of the output (collector) signal to the input (base) connection thereby making the transistor more bilateral. External neutralization can generally eliminate this added package capacitance since one has reasonably close access to points e‴, b‴, c‴ assuming the external leads are cut short. This is unfortunately not quite the case with the internal transition capacitances C_{TE} and C_{TC}. The latter are isolated from points e″, b″ and c″ by r_e', r_b' and r_c' making perfect unilateralization (signal flowing only in the forward direction) very difficult to achieve.

In general, one can summarize the case for (or maybe we should really say — against . . .) the parasitic reactances in the following manner: as the operating frequency increases, all parasitic elements must be minimized, be they resistive as r_e', r_b' and r_c' or reactive as C_{TE} and C_{TC}; be they an integral part of the transistor or of the package as all C_p's and l's shown in Figure 2.25.

Part of this reduction can only be accomplished by the device manufacturer, as only he can design both the device and its package for minimum parasitics. Part of this reduction must be assumed by the user by making an educated choice of the optimum device to be used for a given application at a given frequency, and how to best connect it into the circuit.

Therefore our first simplifying assumption is to neglect all device inductances, which should not create appreciable inaccuracies below 200 mc if we cut external lead lengths to a bare minimum. The second simplification is to lump the existing extrinsic resistances in with their intrinsic relatives, hence r_{bb}', r_e and r_c are the lumped sum of the various resistances in each branch of the structure. The third simplification will be to lump the package and device capacitances. Such approximations will not

give us the epitome of exactness but will allow us to predict the performance of our circuit in the mid-frequency range (from above audio to the low VHF frequencies) with reasonable accuracy.

CONSIDERATIONS OF THE EQUIVALENT CIRCUIT

The variety of equivalent circuits used at medium and high frequencies, range from the simple but not very accurate, to the accurate but very complex representation. Neither extreme is very useful and one should therefore use a reasonably accurate but analytically manageable equivalent circuit.

One of the most popular high-frequency equivalent circuits is the *hybrid-π* common-emitter circuit of Giacolletto[8] Figure 2.26 illustrates this circuit which has the advantage of closely tying the electrical parameters to the physical structure of the device. Figure 2.26(A) shows the general form of this equivalent circuit, Figure 2.26(B) shows the high-frequency simplification of this equivalent circuit. Since the bulk of small signal amplifier circuits use the transistor in the common-emitter configuration, this equivalent circuit sees frequent use.

(A) MEDIUM FREQUENCIES

(B) SIMPLIFICATION AT HIGH FREQUENCIES

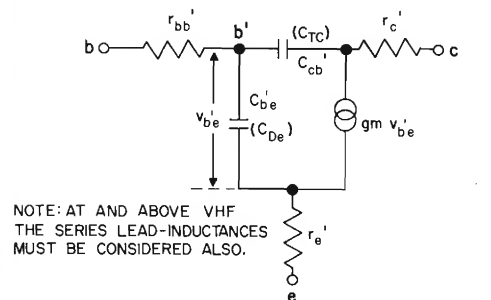
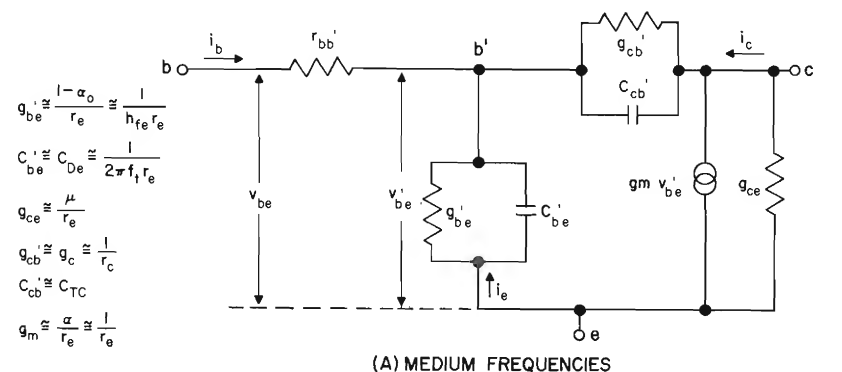
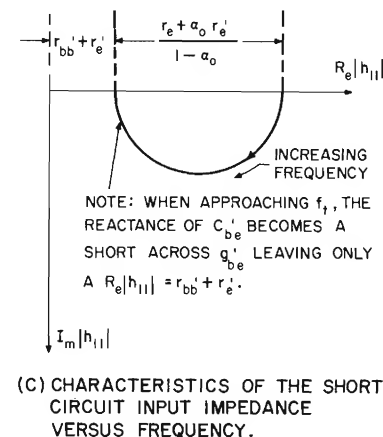
(C) CHARACTERISTICS OF THE SHORT CIRCUIT INPUT IMPEDANCE VERSUS FREQUENCY.

HYBRID-π EQUIVALENT CIRCUIT

Figure 2.26

The base spreading resistance r_{bb}' in this hybrid-π equivalent circuit, is the actual base resistance appearing between the active region (point b') and the external base

contact (point b). The emitter conductance $g_{b'e}$ is not merely the reciprocal of the emitter diffusion resistance (r_e) here, but since the base current appears amplified by h_{fe} in the emitter $g_{b'e}$ becomes $1/h_{fe}\ r_e$. The emitter capacitance, however, is not affected by this mechanism, thus $C_{b'e}$ is approximately equal to the emitter diffusion capacitance

$$C_e = \frac{1}{2\pi f_t r_e}$$

The hybrid-π collector conductance ($g_{cb'}$) and capacitance ($C_{cb'}$) are the aforementioned Early-conductance (g_c) and transition capacitance (C_{TC}) of the collector junction. There remain two elements to consider in this equivalent circuit: *collector to emitter conductance*, g_{ce}; and the *current generator*, $g_m\ v_{be}$.

Collector to Emitter Conductance (g_{ce})

As previously explained, it is generally more convenient to deal with an equivalent circuit composed of mostly generic parameters and then account for Early's base-width modulation by a feedback generator ($\mu\ v_c$) added in the emitter branch. In the hybrid-π, we can take account of this feedback term, by inserting a conductance (g_{ce}) between the collector and emitter. This conductance will have a value of

$$g_{ce} \cong \frac{i_c}{v_c} = \frac{\mu}{r_e}$$

since

$$i_c = \frac{v_c \mu}{r_e}$$

for constant $v_{b'e}$.

Current Generator ($g_m\ v_{b'e}$)

The value of this current generator depends on the internal base voltage $v_{b'e}$. Thus, g_m is determined by $\alpha\ i_e = g_m\ v_{b'e}$ which yields the transconductance

$$g_m = \frac{\alpha i_e}{v_{b'e}}$$

since

$$\frac{i_e}{v_{b'e}} = \frac{1}{r_e}$$

$$g_m = \frac{\alpha}{r_e} \cong \frac{1}{r_e} \cong \frac{h_{fe}}{r_{IN} - r_{bb'}}$$

where gm is the *intrinsic* transconductance. Any internal series resistance or reactance such as the extrinsic emitter resistance r_e' (or even an external unbypassed emitter resistor), or the series-lead inductance in the emitter[9] will reduce the *effective* value of transconductance which we shall define as gm', where

$$g_m' = \frac{g_m}{1 + g_m (R + j X_L)} \qquad (2h)$$

The intrinsic transconductance is constant over an appreciable frequency range. At high frequencies, the emitter-to-base capacitance $C_{b'e}$ effectively shunts $g_{b'e}$, thus reducing g_m and giving us a *transconductance cut-off frequency* (where gm is reduced to .707 of its low frequency value). This frequency is

$$fgm = \frac{r_{b'e} + r_{bb'}}{2\pi\ r_{b'e}\ C_{b'e}\ r_{bb'}} \qquad (2i)$$

In this equation $r_{b'e} = \frac{1}{g_{b'e}} = r_{IN} - r_{bb'}$

and $C_{b'e} \cong \frac{1}{2\pi\ r_{b'e}\ fh_{fe}}$

At high frequencies, the emitter lead inductance also starts reducing g_m' as the following example shows. If $g_m \cong 1/r_e$, $g_m \cong .04$ mhos at 1 ma. Assuming a series inductance of 10 nh and r_e' of 5 ohms, $g_m' = .04/\ 1 + .04\ (5 + j\ 6.28) \cong .03$ mho. The parasitic elements have reduced g_m by 25% at 100 mc. Furthermore, if the transistor is operated at several milliamperes (I_E) the effect will be much more drastic since g_m is higher as current is increased. To summarize what has been illustrated so far on the subject of transconductance

g_m is relatively constant from low through medium-frequencies.

g_m has a cut-off frequency given by equation (2i) whose only reactive element is $C_{b'e}$.

Total measured transconductance is the intrinsic transconductance ($g_m \cong 1/r_e$) modified by the extrinsic terms in series with the active device as illustrated by equation (2h). Therefore the extrinsic emitter resistance, and any external unbypassed emitter resistance as well as both internal and external emitter inductances must be minimized for good high-frequency operation.

Transconductance enters into both the voltage and power gain equations in the following manner:

Voltage Gain

$$A_v \cong \frac{g_m' R_L}{2}$$

Power Gain

$$P_G \cong \frac{(g_m')^2 r_{IN} R_L}{4}$$

Now let us reflect for a moment on the hybrid-π equivalent circuit and decide what values its elements should have for good high-frequency operation.

Base spreading resistance $r_{bb'}$ forms a low-pass filter with $C_{b'e}$, hence both $r_{bb'}$ and $C_{b'e}$ must be reduced as much as possible.

Emitter capacitance $C_{b'e}$ also shunts $g_{b'e}$ (see graph of h_{11} versus frequency in Figure 2.26(B)) thus reducing gm at high frequencies, hence once again $C_{b'e}$ should be minimized.

Transconductance is essentially equal to $h_{fe}/r_{IN} \cong 1/r_e$. The effective transconductance is reduced by extrinsic device and unbypassed external emitter resistance and inductance. These latter must therefore be minimum, both in the device and the external circuit.

Collector capacitance, C_{TC}, provides a feedback path between collector and base (b'). A large collector capacitance increases the feedback with resulting lack of stability (determined by the ratio of forward to reversed gain, the so called *loop gain*).

At low-to-medium frequencies it suffices to know gm, r_{IN} and r_{OUT} to equate voltage gain and power gain. As the transconductance cut-off frequency can be determined from equation (2i), one can see when an appreciable error would result by using the low-frequency gm value. The input and output impedance at low-to-medium frequencies can be calculated (or measured) and from these one can calculate the power gain, voltage gain, and stability factor. The input and output impedances will soon start to be affected by their reactive components, however, and at medium frequencies (in relation to the capabilities of the transistor) they will become complex and difficult to determine analytically.

As a matter of fact, the use of equivalent circuits is more useful to the device designer than to the circuit designer. The former must optimize the structure for its applications. The latter finds to his disappointment that the manufacturer does not specify all the elements of the equivalent circuit. The reason for this, as the circuit designer soon finds out, is that the elements of the various equivalent circuits are difficult to measure accurately. In desperation both device and circuit designer generally turn to the black-box parameters (as these can be measured accurately). Plugging the measured values into well established two-part analysis gives all the necessary information for circuit design. Before we fully abandon the equivalent circuit techniques, however, it should be noted that a full grasp of the equivalent circuit is useful, if not necessary, to evaluate device limitations as well as to compare one device to another. For example, two devices with equal input impedance may have appreciably different values of h_{fe}, r_{bb}' and r_e', thereby yielding radically different performances.

CONSIDERATIONS OF THE TRANSISTOR'S FREQUENCY LIMITATIONS

GAIN-BANDWITH PRODUCT

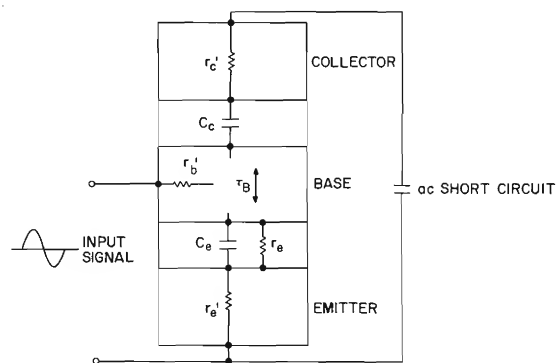
When operated at low frequencies in the common emitter configuration the transistor exhibits a short-circuit current gain ($R_L << r_{OUT}$) of h_{feo}. This value may vary in modern transistors from a low of 20 to a high of several hundred. As the signal frequency is increased, the magnitude of h_{fe} decreases and its phase shift increases. This is due to the fact that when carriers are injected into the base-emitter junction

VARIOUS TIME-CONSTANTS LIMITING THE GAIN-BANDWITH PRODUCT OF THE TRANSISTOR

Figure 2.27

they will take a certain time to cross into the collector region. As a matter of fact, if we look at a physical picture we see (Figure 2.27) that there are three* time constants limiting the speed of the injected carriers[10]: emitter time-constant r_e C_e, collector time-constant r_e C_{TC} (since the collector is shorted to the emitter), and base transit-time τ_B.

Lindmayer et al[10] defines the sum of these three constants as the *gain-bandwidth product* f_t, since it is the frequency at which $|h_{fe}|$ falls to unity, thus

$$f_t = \frac{1}{2\pi\,[\tau_B + r_e\,(C_e + C_c)]}$$

*If the collector bulk resistance is appreciable a fourth time constant $r_c' \times C_{TC}$ must be added.

It can be said that even if C_e ($C_{b'e}$) and C_c (C_{TC}) were made very small, the base transit-time would still limit the frequency response of the transistor. Therefore one must design high gain-bandwidth (f_t) transistors with extremely thin base regions and/or add an accelerating field into the base region. A good modern high-frequency transistor might have

$r_e\,C_{b'e}$ of $25 \times 1 \times 10^{-12}$	$= 0.025$ nanoseconds
$r_e\,C_{TC}$ of $25 \times 0.4 \times 10^{-12}$	$= 0.010$ nanoseconds
τ_B of 125×10^{-12}	$= 0.125$ nanoseconds
Total time for carriers to reach collector	$= 0.160$ nanoseconds

$$\text{Hence } f_t = \frac{1}{2\pi\,TC_{total}} = \frac{1}{6.28 \times 160 \times 10^{-12}} \cong 1.0 \text{ kmc}$$

A large collector bulk resistance will add a fourth time-constant of r_c' C_{TC}, which if $r_c' = 100$ ohms and $C_{TC} = 0.5$ pfd gives the carriers another delay of $100 \times 0.5 \times 10^{-12} = 0.05$ nanosecond, reducing f_t to 760 mc. Thus a good high frequency transistor should also exhibit low extrinsic collector series resistance (r_c'). In epitaxial transistors, r_c' is small and this fourth time-constant can be made negligibly small.

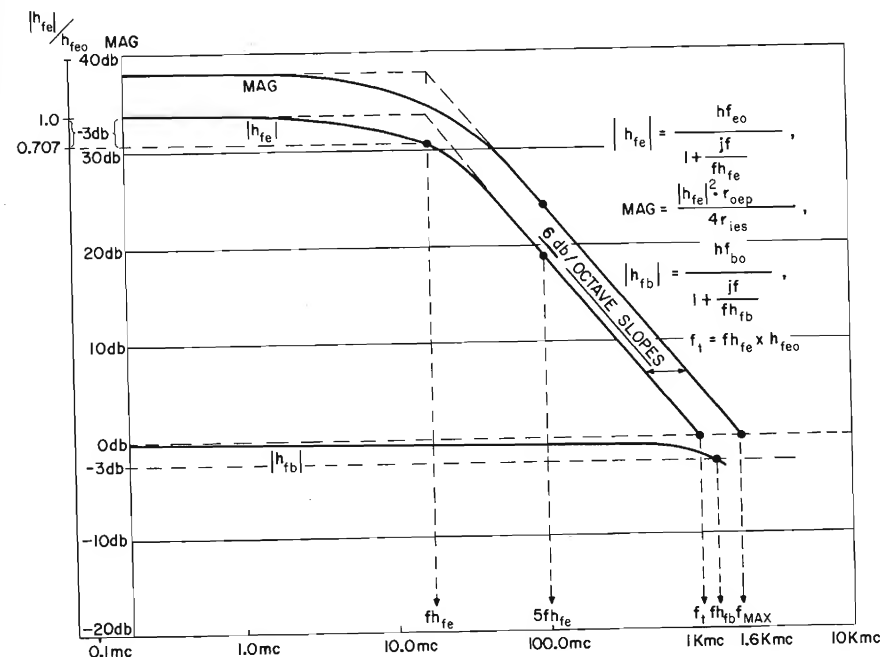
Let us plot h_{fe}, h_{fb}, and maximum available power gain (MAG) versus frequency for a typical 2N918 UHF transistor.

MAG, $|h_{fe}|$, $|h_{fb}|$ VS. FREQUENCY OF TYPICAL UHF TRANSISTOR

Figure 2.28

The first deduction we can make is that there is an exact relationship between f_t and h_{feo} ($h_{feo} \times fh_{fe} = f_t$), both values generally supplied by the transistor manu-

facturer. Secondly at a frequency 5 times this beta cutoff frequency (fh_{fe}), a 6 db/octave slope has been reached. Along this 6 db/octave slope the product of $|h_{fe}|$ and its corresponding frequency is a constant, defined as the so-called *gain-bandwidth product*. The constant has the dimension of a frequency, is called f_t, and is attained when $|h_{fe}| = 1$.

ALPHA AND BETA CUTOFF FREQUENCIES

We have seen in the gain-bandwidth discussion that the beta-cutoff frequency (fh_{fe}) can be used as an aid to locate the proximity of the 6 db/octave slope. Actually, modern transistor circuit analysis has done away with the formerly much used "alpha cutoff frequency" (fh_{fb}) and "beta cutoff frequency" (fh_{fe}).[11] As Pritchard pointed out in an earlier editorial,[12] the modern transistor is primarily frequency-limited by its emitter, base, and collector time-constants, and may not be usable at fh_{fb} (as a matter of fact, due to feedback, there may not even be an fh_{fb}). We shall therefore satisfy ourselves to only define these two frequencies, and use fh_{fe} only as an aid to locate the end of the 6 db/octave slope.

Alpha cutoff frequency is the frequency at which the common-base current gain α, falls to 0.707 of its low frequency value (h_{fbo}). In modern transistors fh_{fb} is usually somewhat above f_t.

Beta cutoff frequency is the frequency at which the common-emitter current gain β, more recently identified as h_{fe}, falls to 0.707 of its low frequency value (h_{feo}).

Transconductance cutoff frequency f_{gm} is the frequency at which g_m falls to 0.707 of its low-frequency value, as previously seen in our discussion of the hybrid-π equivalent circuit.

Maximum frequency of oscillation f_{max} is the frequency at which the maximum available unilateralized power gain (MAG) falls to unity. Looking at the equation for MAG in Figure 2.28, it can be seen that as $|h_{fe}|$ drops to unity there still is a power gain given by $r_{oep}/4r_{ies}$ (impedance ratio of output to input impedance). Hence f_{max} will be generally higher than f_t. f_{max} is sometimes also referred to as the *(power gain)*$^{1/2}$ (bandwidth) product[13]; stated as $\sqrt{PG} \times BW$ which gives us a 6 db PG/octave slope, but should not be confused with f_t. As a matter of fact, we can draw some other interesting conclusions from the MAG equation. The series input-impedance r_{ies} is the real part of h_{ie}, which as we approach f_t (on the 6 db/octave slope) is approximately equal to $r_{bb'}$, see Figure 2.26(B). The parallel output-impedance r_{oep}, is really the reciprocal of g_{oep} (the real part of the output admittance y_{oep}) and is approximately equal to

$$r_{oep} \cong \frac{1}{2\pi f_t C_{TC}} \qquad (2j)$$

since

$$r_{ies} \cong r_{bb'} \qquad (2k)$$

and $|h_{fe}|^2 = \left(\frac{f_t}{f_o}\right)^2$ (along the 6 db/octave slope)

$$MAG = 1 \cong \frac{\left(\frac{f_t}{f_o}\right)^2 \frac{1}{2\pi f_t C_c}}{4r_{bb'}} \quad \text{(to determine } f_{max}, f_o = f_{max}\text{)}$$

$$\text{or } MAG \cong \frac{f_t}{8\pi f_o^2 (r_{bb'} C_{TC})} \qquad (2l)$$

therefore

$$f_{max} = \sqrt{\frac{f_t}{8\, r_{bb'} C_{TC}}} \qquad (2m)$$

Several conclusions can be drawn from the above equations. Providing one operates the transistor in the 6 db/octave slope, which extends from f_t back to about $5fh_{fe}$, a knowledge of

f_t
h_{feo}
$r_{bb'}$, C_{TC} } or at least the $r_{bb'} C_{TC}$ product

gives us a reasonable figure of merit of the transistor, as we can easily derive approximations for

r_{ies} (see equation (2k))
r_{oep} (see equation (2j))
MAG (see equation (2l))
f_{max} (see equation (2m))

The manufacturer of high-frequency transistors will usually give the four required parameters, as they can be measured (relatively) easily. It can be said that the high-frequency performance of a transistor is primarily determined by the four parameters: f_t', $r_{bb'}$, C_{TC} ($C_{b'c}$) and C_{TE} ($C_{b'e}$). C_{TC} imposes an upper limit on output impedance (r_{oep}), $r_{bb'}$ a low limit on input impedance (r_{ies}), C_{TE} limits f_t while f_t in turn limits $|h_{fe}|$ at the operating frequency.

Figure 2.29 is a nomagram which relates the various parameters to make possible a rapid determination of the maximum available unilateralized power gain (MAG) at frequencies above $5fh_{fe}$ (with reduced accuracy down to fh_{fe}).

Step 1 consists of placing a straight edge to join the values (generally specified by the manufacturer) of f_t and $r_{bb'} C_{TC}$ and thereby locating f_{max}. In the example on the nomogram an f_t of 1 kmc and an $r_{bb'} C_{TC}$ time-constant of 15 psec gives an f_{MAX} of approximately 1.6 kmc.

Step 2 then consists of placing the straight edge on the operating frequency (f_o = 100 mc in the example) and joining f_o with the f_{max} determined in step 1 (1600 mc). The maximum available (unilateralized) power gain is then read off the MAG scale. In our 100 mc example, the MAG is approximately 24.5 db.

THE USE OF BLACK-BOX PARAMETERS (h or y)

One other method of high frequency characterization is to use two-port parameters, considering the transistor simply as a *black-box* having one input and one output port. This analysis is much more exact, since it uses the terminal properties of the transistor, rather than the internal parameters of an approximate equivalent circuit. This method applies to any linear two-port active device and is amenable to matrix analysis. The main disadvantage is the lack of direct relationship to the physical equivalent circuit, although this is generally of little concern to the circuit designer. He finds the use of black-box parameters attractive because the manufacturer gives them on his high-frequency transistor specification sheets. Furthermore, both the manufacturer and user can measure the black-box parameters more easily than the elements of the equivalent circuits. The two-port parameters of the linear active network completely describes its performance. It is thus possible to derive complete and accurate gain and stability expressions at any frequency, "plug-in" the measured values of the parameters and "crank-out" the results.

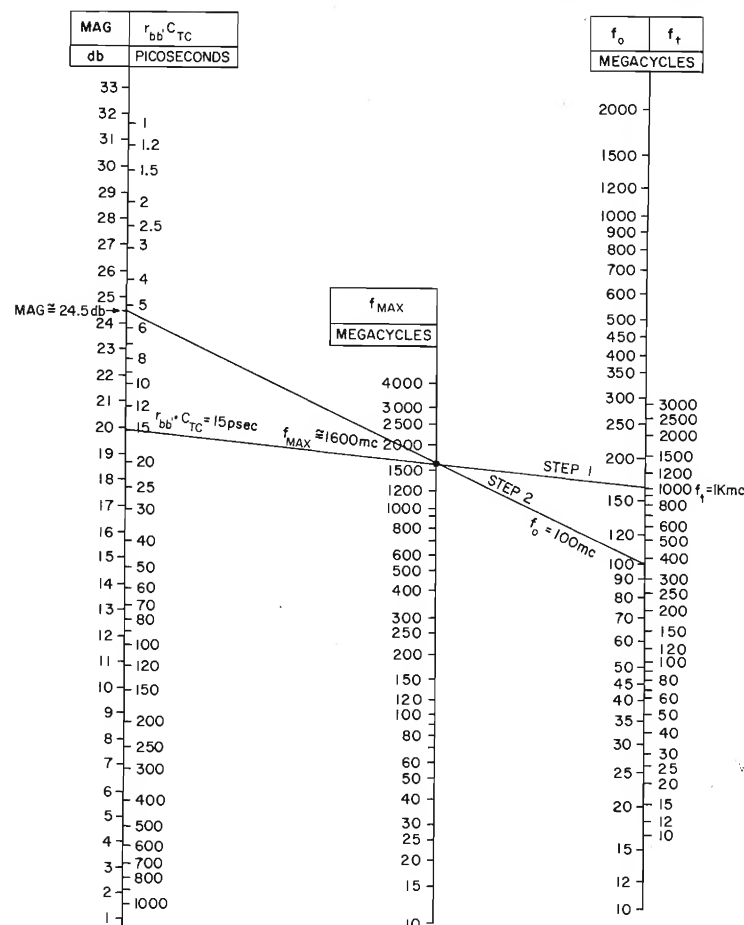
In general, any of the many sets of two-port parameters (z, g, h, y, a and b) could be used. Because at high frequencies it is more convenient to measure the y-parameters, the latter seem to be used predominately on manufacturer's specification sheets. Refer-

NOMOGRAM TO DETERMINE MAG AS A FUNCTION OF $r_{bb'}$, C_{TC} AND f_t

Figure 2.29

ring back to equations (2b) and (2c), the four y-parameters are short-circuit parameters and are given as

$$y_{11} = \frac{i_1}{v_1} = \text{input admittance}$$

$$y_{21} = \frac{i_2}{v_1} = \text{forward transfer admittance}$$

$$y_{12} = \frac{i_1}{v_2} = \text{reverse transfer admittance}$$

$$y_{22} = \frac{i_2}{v_2} = \text{output admittance}$$

Any admittance y can be resolved into its components of conductance g, and sus-

ceptance b, in the following format:

$$y = g + jb$$

hence the input admittance (common-emitter) is

$$\left.\begin{aligned} y_{11e} &= y_{ie} = g_{ie} + jb_{ie} \\ y_{21e} &= y_{fe} = g_{fe} + jb_{fe} \end{aligned}\right\} \text{output ac short-circuited}$$

$$\left.\begin{aligned} y_{12e} &= y_{re} = g_{re} + jb_{re} \\ y_{22e} &= y_{oe} = g_{oe} + jb_{oe} \end{aligned}\right\} \text{input ac short-circuited}$$

The manufacturer's specification sheet will generally show both the real and imaginary components of the y-parameters at a given frequency and operating point (bias). Sometimes there may be graphs of these parameters covering the frequency range for which the transistor has been designed. The next step consists of determining from these measured values the actual dynamic parameters of the transistor.

CALCULATION OF INPUT ADMITTANCE (COMMON-EMITTER)

$$y_{INe} = y_{ie} - \frac{y_{fe}\,y_{re}}{y_{oe} + y_L}$$

where y_L is the load admittance. Since the highest power gain is attained in the *conjugate match** condition, we will make

$$b_{oe} = -b_L$$

hence

$$y_{INe} = y_{ie} - \frac{y_{fe}\,y_{re}}{g_{oe} + g_L}$$

CALCULATION OF OUTPUT ADMITTANCE (COMMON-EMITTER)

$$y_{OUTe} = y_{oe} - \frac{y_{fe}\,y_{re}}{y_{ie} + y_s}$$

where

$$y_s = \text{source admittance, if } (g_{ie} + g_s) >> (b_{ie} + b_s),$$

then

$$y_{OUTe} = y_{oe} - \frac{y_{fe}\,y_{re}}{g_{ie} + g_s}$$

CALCULATION OF GAIN

$$\text{Current gain} = \frac{y_{fe}\,y_L}{y_{ie}\,(y_{oe} + y_L) - y_{fe}\,y_{re}}$$

$$\text{Voltage gain} = \frac{-y_{fe}}{y_L + y_{oe}}$$

$$\text{Power gain} = \left|\frac{y_{fe}}{y_{oe} + y_L}\right|^2 \frac{g_L}{g_{IN}}$$

To determine stability, the loop gain is calculated. This loop gain is essentially the ratio of forward to reverse gain and hence should be as large as possible.

$$\text{Loop gain} = \frac{y_{fe}\,y_{re}}{(y_L + y_{oe})\,(y_L + y_s)}$$

if

$$(g_{ie} + g_s) > (b_{ie} + b_s) \text{ and } (g_{oe} + g_L) > (b_{oe} + b_L);$$

*A linear four-terminal network is conjugate matched if the generator is the complex conjugate (equal magnitude – opposite sign or phase) of its input impedance and the load is the complex conjugate of its output impedance.

then the

$$\text{loop gain} = \frac{y_{fe}\, y_{re}}{(g_{ie} + g_s)\,(g_{oe} + g_L)}$$

$$\text{MAG} = \frac{|y_{fe}|^2}{4 g_{ie}\, g_{oe}}$$

Assume a 2N918 transistor has the following specified parameters at 200 mc:

$$|y_{fe}| = g_{fe} + b_{fe} = R_e\,|y_{fe}| + I_m\,|y_{fe}| = (20 + j50)\ 10^{-3}$$

$$g_{ie} = R_e\,|y_{ie}| \quad = 8 \times 10^{-3}\ \text{mho}$$

$$g_{oe} = R_e\,|y_{oe}| \quad = 0.4 \times 10^{-3}\ \text{mho}$$

$$\text{then its MAG} \cong \frac{2900 \times 10^{-6}}{4 \times 8 \times 10^{-3} \times 0.4 \times 10^{-3}} \cong \frac{2900}{12.8} \cong 227 \cong \underline{23.6\ \text{db}}$$

The loop gain would be very high, since y_{re} is minimized (perfect neutralization is not feasible) in this neutralized condition. Naturally losses in tuned circuits, poorly bypassed resistors, etc., would subtract from the MAG so that the actual circuit power gain will be somewhat smaller than this "maximum" amount of power gain.

MEASUREMENT OF y-PARAMETERS

Short-circuit y-parameter measurements can be made by using simple bridge techniques. Readily available commercial equipment such as the *Boonton RX Meter** (range 1-250 mc), the *Wayne Kerr B801 VHF Admittance Bridge* (range 1-100 mc), and the *General Radio Immittance Bridge B-1601* (range 30-1500 mc) will do the job.

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NOTES

* For details see Boonton "The Note Book" No. 19, 1958.

LARGE SIGNAL CHARACTERISTICS AND TRANSISTOR CHOPPERS

CHAPTER 3

The large signal or d-c characteristics of junction transistors can be described in many cases by the equations derived by Ebers and Moll.[1] These equations are useful for predicting the behavior of transistors in bias circuits, switching circuits, choppers, d-c amplifiers, etc. Some of the more useful equations are listed below for reference. They apply with a high degree of accuracy to germanium and silicon junction transistors operated at low current and voltage levels.

PARAMETERS

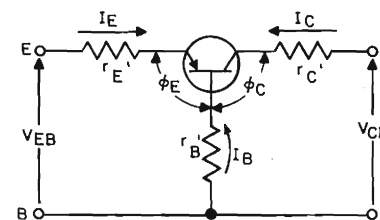
The parameters used in the following large signal equations are listed below and indicated in Figure 3.1.

PARAMETERS USED IN LARGE SIGNAL EQUATIONS

Figure 3.1

I_{CO} I_{CBO} — Collector leakage current with reverse voltage applied to the collector, and the emitter open circuited (I_{CO} has a positive sign for NPN transistors and a negative sign for PNP transistors).

I_{EO} I_{EBO} — Emitter leakage current with reverse voltage applied to the emitter, and the collector open circuited (I_{EO} has a positive sign for NPN transistors and a negative sign for PNP transistors).

α_N — Normal alpha, the d-c common base forward current transfer ratio from emitter to collector with output short circuited (α has a positive sign for NPN transistors and PNP transistors). In practice, best results are obtained if the collector junction has a few tenths of a volt reverse bias. Since α is a function of emitter current, the value at that particular value of emitter or collector current should be used in the large signal equations.

α_I — Inverted alpha, same as α_N but with emitter and collector interchanged.

r_B', r_E', r_C' — Ohmic resistance internal to the transistor and in series with the base, emitter, and collector leads respectively.

I_B, I_E, I_C — D-C currents in the base, emitter, and collector leads respectively; positive sense of current corresponds to current flow into the terminals.

ϕ_C — Bias voltage across collector junction, i.e., collector to base voltage exclusive of ohmic drops (across r_B', r_C'); forward bias is considered a positive polarity.

ϕ_E — Bias voltage across emitter junction, i.e., emitter to base voltage exclusive of ohmic drops (across r_B', r_E'); forward bias is considered a positive polarity.

V_{EB}, V_{CB}, V_{CE} — Terminal voltages: emitter to base, collector to base, and collector to emitter respectively.

$\Lambda = \frac{q}{\eta KT}$ — $1/\Lambda = 26$ millivolts at 25°C for $\eta = 1$.

q — Electronic charge $= 1.60 \times 10^{-19}$ coulomb.

K — Boltzmann's constant $= 1.38 \times 10^{-23}$ watt sec/°K.

T — Absolute temperature, degrees Kelvin = °C + 273.

η — A constant of value between 1 and 2 (η tends to be nearly 1 for germanium transistors and varies between 1 and 2 for silicon transistors).[2]

Λ can be determined from a semi-log plot of the junction forward characteristic (the semi-log scale is used for the current, while the linear scale is used for the voltage). A portion of the plot will be linear, from which Λ can be determined

$$\Lambda = \ln\left(\frac{\Delta I}{\Delta V}\right) \qquad (3a)$$

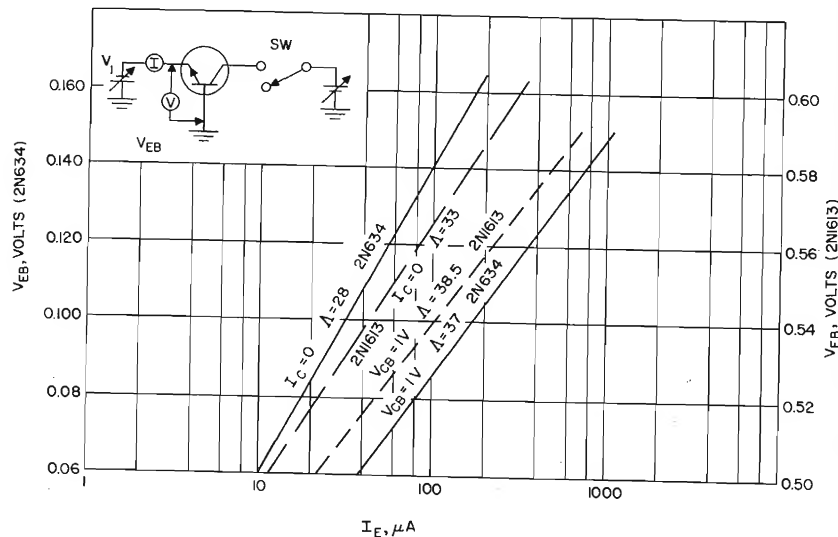
where ΔV is the corresponding change in voltage for a ΔI change in current on the linear portion of the plot. This is shown in Figure 3.2 for the emitter-base junction of a germanium alloy and a silicon planar transistor. Curves are shown for the case of an open collector and for the case of a one volt reverse bias of the collector-base junction. Notice that the slope is different for these two cases. The best correlation between theory and practice results when the Λ obtained with the reverse bias is used.[3]

V_{EB} VS. I_E FOR A GERMANIUM ALLOY AND A SILICON PLANAR TRANSISTOR AS A FUNCTION OF AN OPEN CIRCUITED OR REVERSE BIASED COLLECTOR JUNCTION

Figure 3.2

BASIC EQUATIONS

The basic equations which govern the operation of transistors under all conditions of junction bias are

$$\alpha_N I_{EO} = \alpha_I I_{CO} \qquad (3b)$$

$$I_E = -\frac{I_{EO}}{1-\alpha_N\alpha_I}(e^{\Lambda\phi_E}-1) + \frac{\alpha_I I_{CO}}{1-\alpha_N\alpha_I}(e^{\Lambda\phi_C}-1) \qquad (3c)$$

$$I_C = +\frac{\alpha_N I_{EO}}{1-\alpha_N\alpha_I}(e^{\Lambda\phi_E}-1) - \frac{I_{CO}}{1-\alpha_N\alpha_I}(e^{\Lambda\phi_C}-1) \qquad (3d)$$

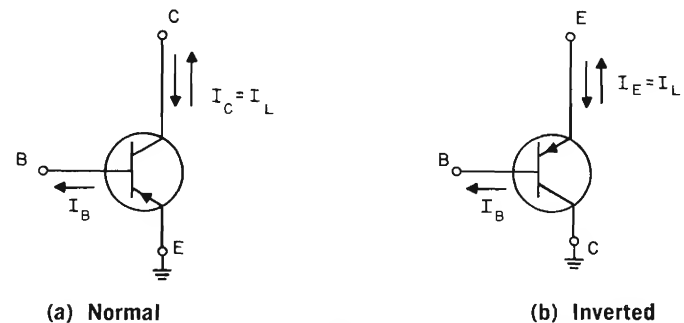
$$I_E + I_B + I_C = 0 \qquad (3e)$$

The above equations are written for the direction of current flow shown in Figure 3.1 and the sign of I_{EO} and I_{CO} as given above under Parameters. The three possible areas of transistor operations are: 1) one junction forward biased and one junction reverse biased (active), 2) both junctions forward biased (saturated), 3) both junctions reverse biased (cutoff).

ACTIVE OPERATION

The transistor behaves as an active device if one junction is forward biased and the other is reverse biased. Under normal operation, the collector is reverse biased so ϕ_C in equations (3c) and (3d) is negative. If this bias exceeds a few tenths of a volt, $e^{\Lambda\phi_C} << 1$, and it can be eliminated from the equations. The collector current can then be solved in terms of the leakage currents, current gains, and emitter-base potential, thus giving the large signal behavior of the device.

SATURATED OPERATION

The transistor can be operated in the normal (grounded emitter) or the inverted (grounded collector) connection as seen in Figure 3.3. The equations which are developed for each respective configuration will be labeled "normal" and "inverted." The directions of base, collector, and emitter current respectively are taken as *into* the transistor. Where a current flows *out* of the transistor, it is to be given a minus sign. When a (±) sign proceeds the equation, the plus applies to a PNP transistor while the minus applies to an NPN transistor.

(a) Normal (b) Inverted

THE NORMAL AND INVERTED CONNECTIONS

Figure 3.3

The transistor in saturation can be represented by an equivalent circuit as shown in Figure 3.4. r_C' and r_E' are the collector and emitter bulk or body resistances from

the junction to the terminals. The collector to emitter voltage due to transistor action, ϕ, is determined by the connection:

$$\text{(Normal)} \qquad V_{CE} = (\pm)\frac{1}{\Lambda} \ln \frac{\alpha_I \left[1 - \frac{I_C}{I_B}\frac{(1-\alpha_N)}{\alpha_N}\right]}{\left[1 + \frac{I_C}{I_B}(1-\alpha_I)\right]} \qquad (3f)$$

$$\text{(Inverted)} \qquad \phi_{EC} = (\pm)\frac{1}{\Lambda} \ln \frac{\alpha_N \left[1 - \frac{I_E}{I_B}\frac{(1-\alpha_I)}{\alpha_I}\right]}{\left[1 + \frac{I_E}{I_B}(1-\alpha_N)\right]} \qquad (3g)$$

Notice that equation (3g) can be obtained from (3f) by replacing I_C by I_E, α_N by α_I in the numerator, and α_I by α_N in the denominator. If the ratio of load current to base drive, $\frac{I_B}{I_C}$ or $\frac{I_E}{I_B}$ is very small or zero, equations (3f) and (3g) respectively reduce to

$$\text{(Normal)} \qquad \phi_{CE} \approx (\pm)\frac{1}{\Lambda} \ln \alpha_I \qquad (3h)$$

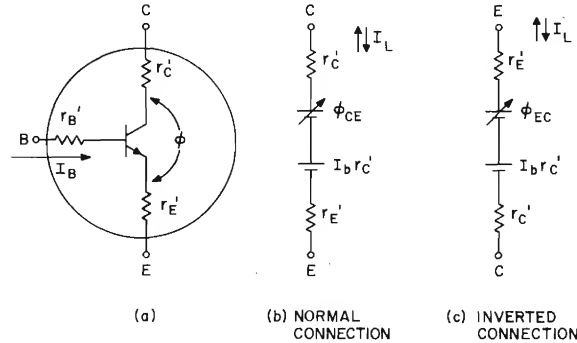
$$\text{(Inverted)} \qquad \phi_{EC} \approx (\pm)\frac{1}{\Lambda} \ln \alpha_N \qquad (3i)$$

EQUIVALENT COLLECTOR-EMITTER CIRCUIT OF A SATURATED TRANSISTOR

Figure 3.4

Thus the collector to emitter voltage or "offset voltage" becomes (for an npn transistor)

$$\text{(Normal)} \qquad V_{CE} = -\frac{1}{\Lambda}\ln \alpha_I + I_b\, r_E' \qquad (3j)$$

$$\text{(Inverted)} \qquad V_{EC} = -\frac{1}{\Lambda}\ln \alpha_N + I_B\, r_C' \qquad (3k)$$

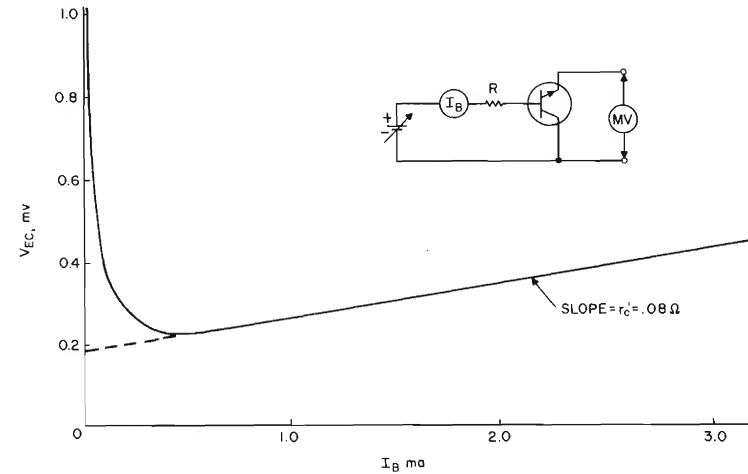
Since α_N and α_I are functions of base drive, the offset voltage will change as I_B is varied. This is shown in Figure 3.5 which shows the inverted connection offset voltage of a planar epitaxial transistor as a function of base current. From zero, the offset voltage decreases with increasing base drive because α_N is increasing. At some base drive, the offset voltage becomes a minimum. Above this, the offset voltage becomes a linear function of I_B since the $I_B r_C'$ drop predominates. The slope of V_{EC} vs. I_B curve in this region (with $I_E = 0$) gives r_C'. Likewise, by operating the transistor in the normal connection (with $I_C = 0$) the slope of V_{CE} vs. I_B curve at the higher values of base current ($I_B > 1$ ma) gives r_E'.

V_{EC} VS. I_B FOR 2N2192

Figure 3.5

Since $\alpha_I < \alpha_N$ for most transistors, the offset voltage of the inverted connection will be less than that of the normal connection. Thus in low level chopper circuits, the inverted connection is always used. Examination of equations (3f) and (3g) shows that the sign of ϕ_{CE} and ϕ_{EC} can be made to reverse by forcing a load current from collector to emitter for a PNP transistor and from emitter to collector for a NPN transistor. Thus, the emitter to collector terminal voltages V_{EC} or V_{CE} can be made zero.

The transistor in either mode of operation will remain saturated as long as the bracketed terms in the numerator or denominator of equations (3f) and (3g) remain larger than one. *Thus, the transistor behaves as a "closed switch," and the load current can flow through the transistor from collector to emitter or emitter to collector, depending upon the polarity of the load supply.* If either the numerator or denominator term which is bracketed becomes zero, the log becomes infinite and the transistor comes out of saturation. Since $\alpha_I < \alpha_N$, it can be seen from equations (3f) and (3g), that both the normal and inverted configurations will become unsaturated respectively at lower ratios of $\frac{I_C}{I_B}$ & $\frac{I_E}{I_B}$ if the load current passes from collector to emitter in a PNP transistor, and from emitter to collector in an NPN transistor.

By differentiating equation (3f) and (3g) respectively with respect to I_C and I_E, and adding the bulk resistances, the dynamic impedance of the saturated transistor can be found. If $\left(\frac{1-\alpha_N}{\alpha_N}\frac{I_C}{I_B}\right)$ and $\left(\frac{1-\alpha_I}{\alpha_I}\right)\frac{I_E}{I_B}$ are much less than 1, then

$$\text{(Normal)} \qquad r_{dN} \approx \frac{1}{\Lambda}\left(\frac{1-\alpha_I\,\alpha_N}{I_B\,\alpha_I}\right) + r_E' + r_C' \qquad (3l)$$

$$\text{(Inverted)} \qquad r_{dI} \approx \frac{1}{\Lambda}\left(\frac{1-\alpha_I\,\alpha_N}{I_B\,\alpha_N}\right) + r_E' + r_C' \qquad (3m)$$

$$\text{and} \qquad \frac{r_{dI}}{r_{dN}} = \frac{\alpha_N}{\alpha_I} \qquad (3n)$$

if $r_E' + r_C' << \frac{1}{\Lambda}\left(\frac{1-\alpha_I\,\alpha_N}{I_B\,\alpha_N}\right)$.

For base currents where the above inequality holds, the dynamic impedance is inversely proportional to the base current as shown in Figure 3.6. Also, the dynamic impedance of the inverted connection is larger than that of the normal connection since $\alpha_N < \alpha_I$. (This is in contrast to the offset voltage where it is smaller for the inverted mode than for the normal connection.)

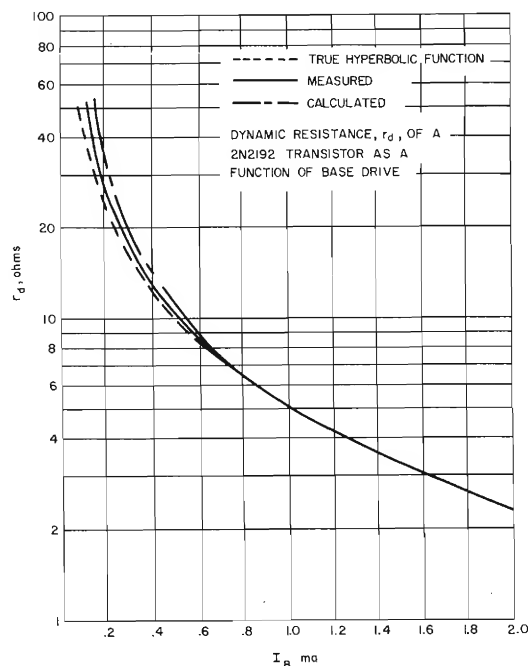



Figure 3.6

CUTOFF OPERATION

By reverse biasing both emitter and collector, equations (3b), (c), and (d) can be solved for the emitter and collector currents

(Normal) $$I_C = \frac{I_{CO}(1 - \alpha_I)}{1 - \alpha_N\alpha_I} \quad (3o)$$

(Inverted) $$I_E = \frac{I_{EO}(1 - \alpha_N)}{1 - \alpha_N\alpha_I} \quad (3p)$$

Equations (3o) and (3p) indicate that with both junctions reverse biased, the collector current will be less than I_{CO}, and the emitter current will be less than I_{EO}. Also, the inverted connected will result in the lowest leakage current in the load. While this is true for germanium transistors, it is not true for most silicon transistors. The reason for this is that the alphas of the silicon transistor are almost zero at collector or emitter currents given by the leakage currents. Leakage currents for well made signal planar transistors at low voltages are below a nanoampere.

USEFUL LARGE SIGNAL RELATIONSHIPS

The relationships given with an asterisk * (opposite page) apply only to germanium transistors and not to signal silicon transistors because of the reasons given in the preceding section of this chapter.

COLLECTOR LEAKAGE CURRENT (I_{CEO})*

For the direction of current flow shown

$I_B = 0$; I_{CEO}; $-V_{CE} > -0.1$ VOLT

$$I_{CEO} = \frac{I_{CO}}{1 - \alpha_N} \quad (3q)$$

I_{CEO} is the collector leakage current with the base open-circuited and is generally much larger than I_{CO}.

COLLECTOR LEAKAGE CURRENT (I_{CES})*

For the direction of current flow shown

$$I_{CES} = \frac{I_{CO}}{1 - \alpha_N\alpha_I} \quad (3r)$$

I_{CES} is the collector leakage current with the base shorted to the emitter and equals the leakage current the collector diode would have if the emitter junction was not present. Accurate values of α_N and α_I for use in the equations in this section are best obtained by measurement of I_{CO}, I_{CEO} and I_{CES} and calculation of α_N and α_I from equations (3q) and (3r). The value of I_{EO} may be calculated from equation (3b).

COLLECTOR LEAKAGE CURRENT (I_{CER})*

For direction of current flow shown

$V_{CE} > -0.1$ VOLT; I_{CER}; R

$$I_{CER} = \frac{(1 + \Lambda I_{EO}R)\, I_{CO}}{1 - \alpha_N\alpha_I + \Lambda R I_{EO}(1 - \alpha_N)} \quad (3s)$$

I_{CER} is the collector leakage current measured with the emitter grounded and a resistor R between base and ground. The size of the resistor is generally about 10 K. From equation (3s), it is seen that as R becomes very large, I_{CER} approaches I_{CEO}—equation (3q). Similarly, as R approaches zero, I_{CER} approaches I_{CES}—equation (3r).

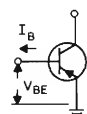
COLLECTOR LEAKAGE CURRENT — SILICON DIODE IN SERIES WITH EMITTER*

For direction of current flow shown

$V_C > -0.8$ VOLT; I_C; R; V_D

$$I_C = \frac{(1 + \Lambda I_{EO}R - \alpha_I\Lambda V_D)\, I_{CO}}{1 - \alpha_N\alpha_I + \Lambda R I_{EO}(1 - \alpha_N)} \quad (3t)$$

This circuit is useful in some switching applications where a low collector leakage current is required and a positive supply voltage is not available for reverse biasing the base of the transistor. The diode voltage V_D used in the equation is measured at a forward current equal to the I_{CO} of the transistor. This equation holds for values of I_C larger than I_{CO}.

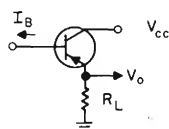
BASE INPUT CHARACTERISTICS

for $I_C = 0$

$$V_{BE} = I_B (R_E + R_B) + \frac{1}{\Lambda} \ln \left(\frac{I_B}{I_{EO}} + 1 \right) \qquad (3u)$$

for $V_{CE} > -.1$ volt

$$V_{BE} = I_B \left(R_B + \frac{R_E}{1 - \alpha_N} \right) + \frac{1}{\Lambda} \ln \left[\frac{I_B (1-\alpha_N \alpha_I)}{I_{EO} (1-\alpha_N)} + 1 + \frac{\alpha_N (1-\alpha_I)}{\alpha_I (1-\alpha_N)} \right] \qquad (3v)$$

A comparison of equations (3u) and (3v) indicates that they are approximately equal if R_E is small and α_N is smaller than α_I. For this condition, the base input characteristic will be the same whether the collector is reverse biased or open-circuited.

VOLTAGE COMPARATOR CIRCUIT

for $V_O = V_{CC}$

$$I_B = \frac{V_{CC}}{R_L} \left[1 + \left(\frac{\alpha_N}{\alpha_I} \right) \left(\frac{1 - \alpha_I}{1 - \alpha_N} \right) \right] \qquad (3w)$$

If an emitter follower is overdriven such that the base current exceeds the emitter current, the emitter voltage can be made exactly equal to the collector voltage. For example, if a square wave with an amplitude greater than V_{CC} is applied to the base of the transistor, the output voltage V_O will be a square wave exactly equal to V_{CC}. Equation (3w) gives the base current required for this condition and indicates that the transistor should be used in the inverted connection if the required base current is to be minimized. This circuit is useful in voltage comparators and similar circuits where a precise setting of voltage is necessary.

JUNCTION TRANSISTOR CHOPPERS

Transistor choppers are used in the amplification of low level d.c. signals, as well as in the conversion of d.c. signals to a synchronous a.c. voltage for driving the control phase of two phase servo motors. The chopper converts the d.c. signal to a synchronous a.c. voltage whose magnitude is proportional to that of the d.c. signal, and whose phase relationship to the reference a.c. voltage is either zero or 180°, depending upon the polarity of the d.c. voltage. This can best be seen by referring to Figure 3.7(A). The chopper contacts close during the positive half cycle of the a.c. reference and open during the negative half cycle. With the switch in position 1, the positive voltage E_S is tied to the resistor R as shown in Figure 3.7(B) during the positive half cycle of the reference. During the negative half cycle of the reference, the chopper contacts are open and the voltage across R is zero. The capacitor removes the d.c. level such that e_o is now an a.c. square wave which in phase with the reference a.c. If the switch is in position 2, the negative voltage E_S is applied to R during the positive half cycle of the reference voltage, and as can be seen in Figure 3.7(C), the output is 180° out of phase with the reference a.c.

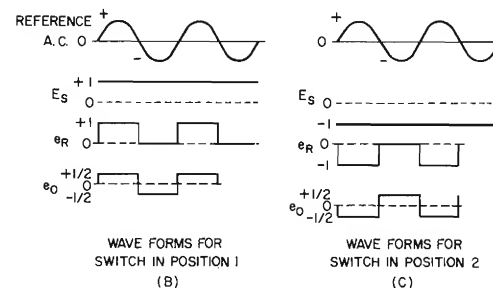
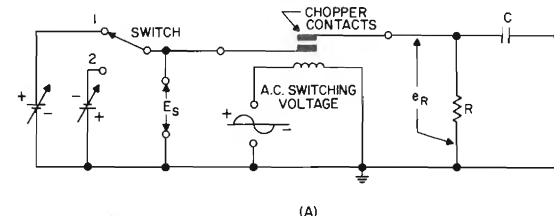
Figure 3.8 shows a single transistor replacing the mechanical chopper. When the base voltage is made positive with respect to the collector (NPN transistor), the transistor behaves as a closed switch, and the d.c. input voltage is connected to R. During the half cycle of the reference voltage when the base is made negative with the supply,

HALF-WAVE CHOPPER

Figure 3.7

the transistor behaves as an open switch, and the voltage across R is zero. However, the transistor is not a perfect switch, and an error voltage and current are respectively superimposed on the d.c. source. During the half cycle that the switch is closed, the error voltage introduced by the transistor is

$$V_{EC} = .026 \ln \alpha_N + I_B r_C' \qquad (3x)$$

where α_N is the normal alpha as defined at the beginning of this chapter and r_C' is the collector bulk or body resistance. The error current which is introduced when the transistor is an open switch is

$$I_{PI} = \frac{I_{CBO}\, \alpha_I (1 - \alpha_N)}{\alpha_N (1 - \alpha_N \alpha_I)} \qquad (3y)$$

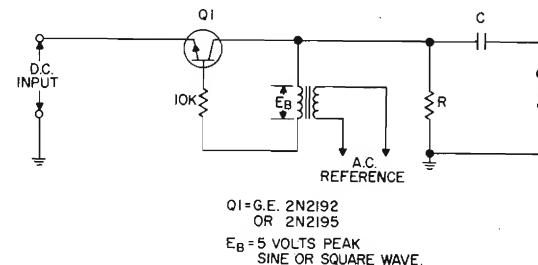
where α_I is the inverse alpha and I_{CBO} is the leakage current as defined earlier in this chapter.

SIMPLE SERIES TRANSISTOR CHOPPER

Figure 3.8

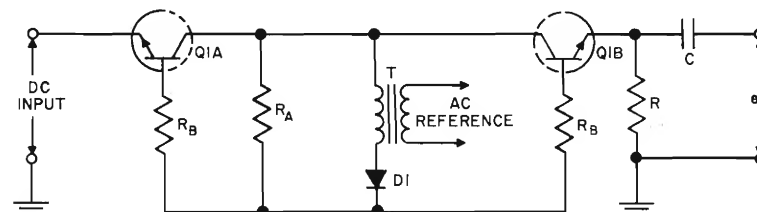
The error voltage introduced by the transistor during the "on" half cycle can be minimized by using two transistors whose offset voltages cancel one another as shown in Figure 3.9. The transistors must not only be matched at room temperature but must track over the required ambient temperature extremes. This is no problem with transistors such as the 2N2356 and the 2N3082 where two transistor pellets are mounted in one header. The initial offset voltages are matched to 50 and 75 miciovolts respectively. Drifts of less than ±100 microvolts over an ambient temperature of −55 to 125°C are easily obtainable. The low drift results primarily from the low initial offsets of each transistor (due to the very high α_N and low r_c') and to the negligible temperature difference between the transistor pellets. Some of the important parameters of these chopper transistors is given in Table 3.1.

TYPE NUMBER	G.E. 2N2356	G.E. 2N2356A	G.E. 2N3082	G.E. 2N3083	UNITS
BV_{CBO}	25	25	25	25	volts, min
BV_{CEO}	—	—	20	20	volts, min
BV_{EBO}	7	7	10	10	volts, min
Differential Offset Voltage, 25°C	50	—	75	—	μ volts, max
Differential Offset Voltage change with temperature −55 to 25°C 25 to 50°C	 100 100	 — —	 100 100	 — —	 μ volts, max μ volts, max
Differential Offset Voltage, −55 to 125°C	—	50	—	75	μ volts, max
Differential Offset Current, 25°C	2	2	5	2	n amp, max
"On" Dynamic Resistance, $I_{B1} = I_{B2} = 1$ ma	40	40	40	40	ohm, max
Collector Capacitance ($V_{CB} = 0$ V)	—	—	8	8	pf, max
Emitter Capacitance ($V_{EB} = 0$ V)	—	—	8	8	pf, max

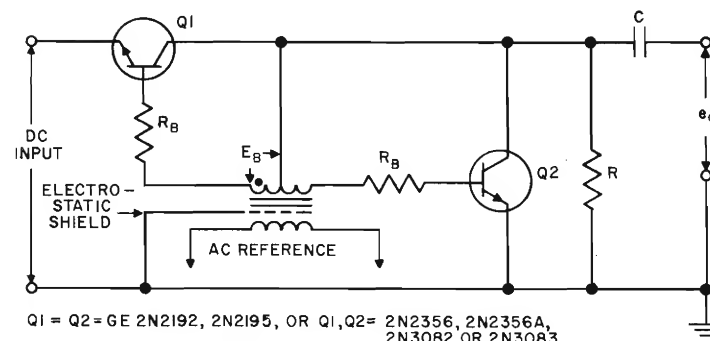
PARAMETERS OF CHOPPER TRANSISTORS

Table 3.1

A chopper configuration[4, 5] which can be used to advantage for a low source impedance input is shown in Figure 3.10. During the half cycle when Q_1 is "on," Q_2 is turned "off" because its collector-base junction is reverse biased, and R is tied to the d.c. input. On the next half cycle when Q_1 is turned "off," Q_2 is turned "on," shorting R, The leakage current due to Q_1 does not flow through R during this half cycle since Q_2 essentially short circuits R. During the alternate half cycle when Q_2 is turned "off," its leakage current will flow primarily through Q_1 (its turned "on") and the input circuit

if R is made much larger than the source impedance. Thus, the drift due to leakage current is minimized. In addition, the offset voltages of the two transistors effectively cancel, even though they occur on separate half cycles. The reason for this is that they form a d.c. voltage which is not chopped and which is not passed by the capacitor, C. An advantage this circuit has over the chopper circuits discussed above is that it is less sensitive to noise pickup because the load always looks back into a low impedance.

NOTE:
1. QIA QIB – GE 2N2356, 2N2356A, 2N3082 OR 2N3083 (TWO MATCHED TRANSISTORS IN ONE PACKAGE)
2. ELECTROSTATIC SHIELDING BETWEEN PRIMARY AND SECONDARY WINDINGS OF TRANSFORMER T MAY BE REQUIRED.
3. R_B = 10K, E_B = 10 VOLT PEAK (SINE OR SQUARE WAVE).
4. DI = IN3604

AN IMPROVED SERIES TRANSISTOR CHOPPER

Figure 3.9

QI = Q2 = GE 2N2192, 2N2195, OR QI, Q2 = 2N2356, 2N2356A, 2N3082 OR 2N3083

NOTES:
1. R_B = 10K, E_B = 7.5V SINE OR SQUARE WAVE FOR 2N2195, 2N2192, 2N2356, 2N2356A
2. R_B = 50K, E_B = 5V SQUARE WAVE FOR 2N3082, 2N3083

SERIES-SHUNT CHOPPER

Figure 3.10

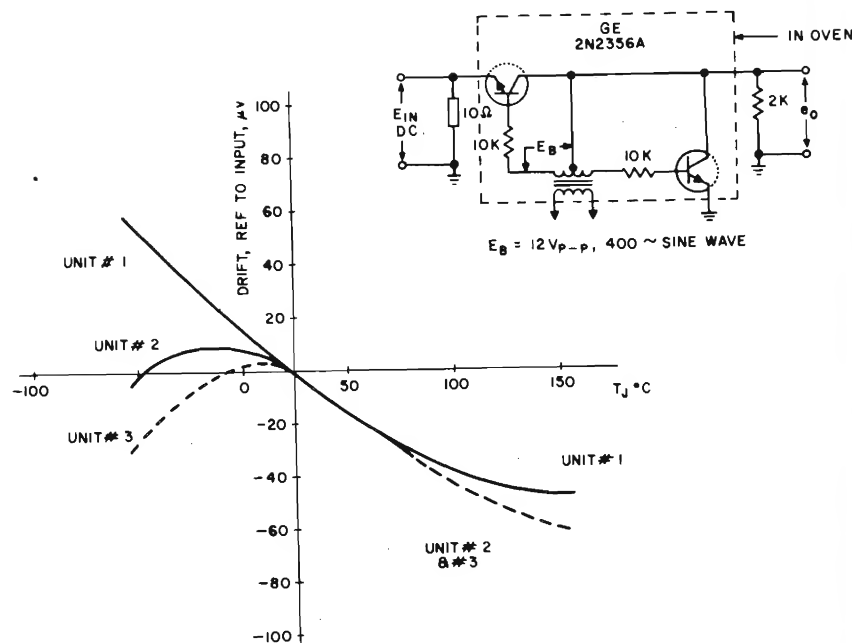
Figure 3.11 shows actual drift performance obtained with this circuit using the 2N2356A as the chopper transistor[6]. The chopper drift was less than ±60 μv from −55 to 150°C.

TYPICAL TEMPERATURE DRIFT OF SERIES — SHUNT CHOPPER USING GE 2N2356A

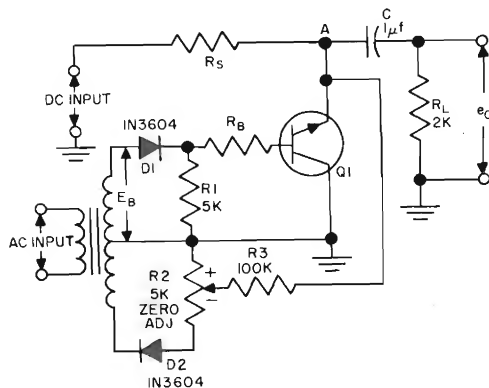
Figure 3.11

SHUNT CHOPPER FOR HIGH IMPEDANCE SOURCES

Figure 3.12

Figure 3.12 shows a transistor chopper used for high source impedance applications or those where the d.c. input cannot be loaded. Although R_S is shown as part of the chopper circuit, it can be the d.c. source impedance.

Operation of this chopper is basically one of shorting node A to ground each half cycle when the base of the transistor is made positive with respect to ground (the collector). A zeroing adjustment for removing the transistor's offset voltage is provided by D_1, R_2, and R_3 which causes a current to flow during the half cycle from collector to emitter [see equation (3g)]. In some applications where the 12X1111 and 2N2192 are used, the offset voltage is small enough (less than a millivolt) so that the balance network can be eliminated.

On the half cycle of the supply which would normally reverse bias the collector-base junction of Q, the diode D_1 prevents this from occurring. The collector-base potential is then zero; however, Chaplin and Owens[7] have shown that the emitter-collector impedance is given by

$$r_{EC} = \frac{0.026}{I_{CBO}}(1 + \alpha_N/\alpha_I - 2\,\alpha_N) \qquad (3z)$$

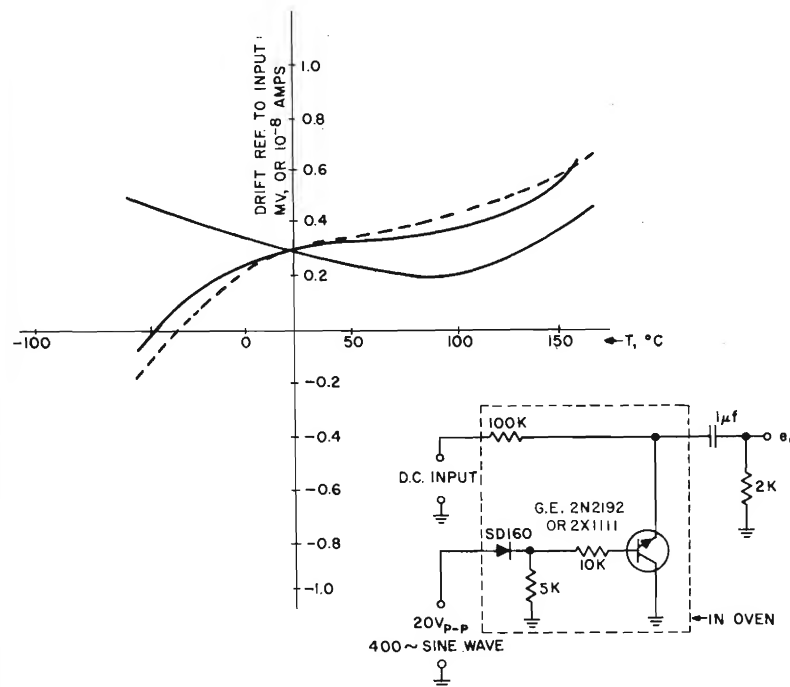
Thus the dynamic impedance is approximately 26 mv. divided by the I_{CBO}. For silicon transistors (even at high temperatures) this impedance can be made larger than the load impedance so that the current at node A due to the input d.c. voltage flows into the load during this half cycle. The maximum value of the load is then determined by the minimum value of r_{EC} obtained from equation (3z). Also, any drifts which normally

CHOPPER DRIFT WITH 2N2192

Figure 3.13

would have been caused by the transistor leakage currents have been eliminated.

For the condition that $r_{EC} >> R_L$, the peak to peak load current is given by

$$I_{P\text{-}P} = \frac{2\,E_{D.C.}}{R_S + 2\,R_L} \qquad (3aa)$$

The equivalent input current drift due to drift in transistor offset voltage (ΔV) is shown to be

$$I_O = \frac{\Delta V}{R_S} \text{ for } R_S >> R_L \qquad (3bb)$$

A second component of the chopper drift is due to transient current spikes which occur when the transistor switches "on" and "off." The net area (charge) of the transients develops a potential on the capacitor C which, to the circuit, appears as an input signal. In order to zero the output, a d.c. input current (integrated over one-half cycle) must be provided. The 12X1111 is ideal for this application because of its low junction capacitances (< 8 pf at 0 volts) and low initial offset ($< 250\ \mu V$ at $I_B = .1$ ma).

Temperature drift tests made using 2N2192's show that with the entire chopper of Figure 3.12 exposed to temperature, the required d.c. input necessary to zero the output is less than 10^{-8} amperes from -55 to $125°C$. This is equivalent to 1 mv of drift referred to the input for $R_S = 100$ K.

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(1) Ebers, J. J., "Large – Signal Behavior of Junction Transistors," *Proceedings of the IRE*, Vol. 42, December 1954.

(2) Pritchard, R. C., "Advances in the Understanding of the P-N Junction Triode," *Proceedings of the IRE*, Vol. 46, June 1958.

(3) Giorgis, J., "Some Large Signal Properties of Planar and Planar Epitaxial Transistors," G. E. Application Note 90.13.

(4) Kruper, A., "Switching Transistors used as a Substitute for Mechanical Low Level Choppers," *AIEE Transactions*, Vol. 74, part I, March 1955.

(5) Giorgis, J., and Thompson, C. C., "Silicon Transistor Performance in a Chopper Application," *Applications and Industry*, #37, July 1958.

(6) Giorgis, J., "Silicon Transistor Choppers for Low Impedance Sources," *Solid State Design*, Vol. 4, No. 5, May 1963.

(7) Chaplin, G. B., and Owens, A. R., "Some Transistor Input Stages for High-Gain D.C. Amplifiers," *The Proceedings of the IEE*, Vol. 105, part B, No. 21, May 1958.

(8) Giorgis, J., "A Transistor Chopper for High Impedance Sources," *Electronic Equipment Engineering*, Vol. 11, No. 1, January 1963.

NOTES

BIASING AND DC AMPLIFIERS

CHAPTER 4

BIASING

INTRODUCTION

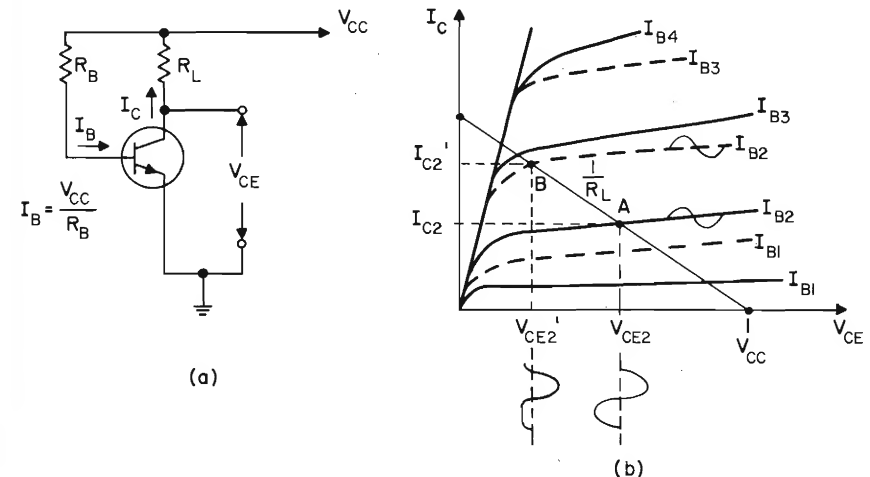
One of the basic problems encountered in the design of transistor amplifiers is that of establishing and maintaining the proper dc emitter current and collector to emitter voltage (called the *bias conditions of the circuit*). The biasing problem is due primarily to the change of transistor parameters (h_{FE}, I_{CO}, V_{BE}) with temperature and the variation of these parameters between transistors of the same type. This can readily be seen by referring to Figure 4.1(a) where the transistor is operated in the common emitter mode and is biased by a constant base current, I_B. Figure 4.1(b) shows the common emitter collector characteristics of two different transistors with the same collector load line superimposed on them. For the transistor characteristic shown with solid lines and a base current I_{B2}, the operating point is at A. On the other hand, if a higher gain transistor is used, or the original transistor's gain and leakage current are increased due to an increase in temperature, the transistor characteristic shown with dashed lines could result. For the same base current, I_{B2}, the bias point is at B and distortion would result since the transistor begins to saturate during the positive half cycle of the signal base current.

SIMPLE BIAS CIRCUIT

Figure 4.1

The factors which must be considered in the design of transistor bias circuits, whether operating class A or class B, and single or multi stage include

1. *The specified maximum and minimum values of current gain (h_{FE}) at the operating point* for the type of transistor used.

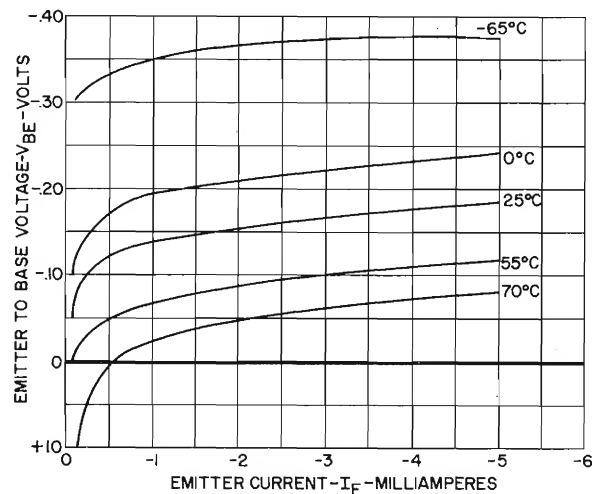
2. *The variation of h_{FE} with temperature.* This will determine the maximum and minimum values of h_{FE} over the desired temperature range of operation. The variation of h_{FE} with temperature is shown in Figure 1.26 for the 2N525 transistor.
3. *The variation of collector leakage current (I_{CO}) with temperature.* For most transistors, I_{CO} increases at approximately 6.5-8%/°C and doubles with a temperature change of 9-11°C. In the design of bias circuits, the minimum value of I_{CO} is assumed to be zero and the maximum value of I_{CO} is obtained from the specifications and from a curve such as Figure 1.25. In low level stages and when silicon transistors are used, I_{CO} can usually be neglected if the junction temperature is below about 100°C. This is not true, however, if the emitter bias current is in the microampere region.
4. *The variation of base to emitter voltage drop (V_{BE}) with temperature.* Under normal bias conditions, V_{BE} is about 0.2 volts for germanium transistors and 0.7 volts for silicon transistors and has a temperature coefficient of about —2.5 millivolts per °C. Figure 4.2 shows the variation of V_{BE} with collector current at several different temperatures for the 2N525. Note that for some conditions of high temperature it is necessary to reverse bias the base to get a low value of collector current.
5. *The tolerance of the resistors used in the bias networks; tolerance of the supply voltages.*

INPUT CHARACTERISTICS OF 2N525 (V_{CE} = 1V)

Figure 4.2

SINGLE STAGE BIASING

Several bias circuits are shown in Figure 4.3(a) through 4.3(d) which have been used to stabilize the emitter current and collector to emitter voltage. There are a number of methods by which each circuit can be analyzed and synthesized, and the methods chosen depend upon the requirements of the application and the aptitude and preference of the designer. For example, the circuit of Figure 4.3(c) roughly can

be biased for low level applications which operate near room temperature. The V_{CE}, V_{CC} and I_E are selected by the designer – generally it is advisable to choose V_{CE} and I_E at the values given on the specification sheet for the measurement of the small signal parameters. I_B is then $I_E/h_{FE} + I_{CO}$; and V_A, the voltage at point A of Figure 4.3(c), is then $I_E R_3 + V_{BE}$. (V_{BE} is approximately .2 volts for germanium and 0.7 volts for silicon.) $I_E R_3$ is chosen to be at least five times larger than V_{BE}, and the current through R_2 is chosen to be at least five times I_B. R_2 is then V_A/I_2, and R_1 is

$$\frac{V_{CC} - V_A}{I_{R2} + I_B}$$

The load resistance is then

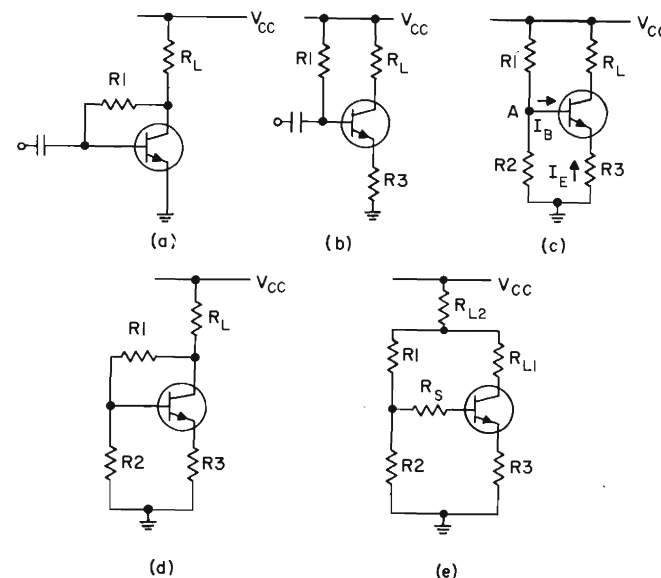
$$\frac{V_{CC} - I_E R_3 - V_{CE}}{I_E} \text{ or } \frac{V_{CC} - V_{CE}}{I_E} - R_3$$

VARIOUS CLASS A BIAS CIRCUITS

Figure 4.3

Most applications require operation in an ambient other than room temperature so that a more thorough analysis must be done. Rather than analyzing each circuit individually, a general one battery circuit as shown in Figure 4.3(e) can be analyzed. Each of the other circuits in Figure 4.3 can be obtained by setting the appropriate resistor in 4.3(e) to zero or infinity. For example, the circuit of Figure 4.3(b) is obtained by setting R_{L2} and R_S equal to zero and R_2 equal to infinity.

By means of Thévenin's theorem, any of the circuits in Figure 4.3 can be converted into another general circuit which consists of a three resistor and two battery circuit as shown in Figure 4.4.[1] This allows the designer to use the simple circuit of Figure 4.4 to analyze the bias circuit and determine the values of R_E, R_C, R_B, V_B and V_C.

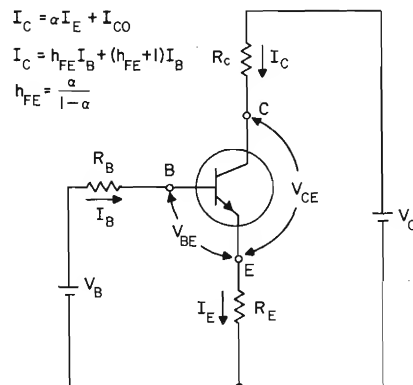
Once these are obtained, then the resistance values and the supply voltage of any of the bias circuits of Figure 4.3 can be determined.

GENERAL TRANSISTOR BIAS CIRCUIT

Figure 4.4

Thus, for the circuit of Figure 4.4, the following equations apply

$$I_E = (h_{FE} + 1)\,(I_B + I_{CO}) \tag{4a}$$

$$V_B = \left[\frac{R_B}{(h_{FE}+1)} + R_E\right] I_E + V_{BE} - I_{CO} R_B \tag{4b}$$

$$V_C = I_E\,(R_E + \alpha R_C) + V_{CE} \tag{4c}$$

(The currents in the above equation and as shown in Figure 4.4 are those which would be measured if an ammeter were inserted in that circuit.)

Considering bias conditions at the temperature extremes: at the minimum temperature, I_E will have its minimum value, and the worst conditions would occur for $h_{FE} = h_{FE}^{min}$, $V_{BE} = V_{BE}^{max}$, $I_{CO} = 0$, or, at the lowest temperature

$$V_B = \left[\frac{R_B}{h_{FE}^{min}+1} + R_E\right] I_E^{min} + V_{BE}^{max} \tag{4d}$$

At the highest temperature of operation I_E will have its maximum value and the worst conditions would occur for $h_{FE} = h_{FE}^{max}$, $V_{BE} = V_{BE}^{min}$, $I_{CO} = I_{CO}^{max}$. At the highest temperature

$$V_B = \left[\frac{R_B}{h_{FE}^{max}+1} + R_E\right] I_E^{max} + V_{BE}^{min} - I_{CO}^{max} R_B. \tag{4e}$$

From these two equations the value of R_B can be calculated by equating the two expressions, thus

$$R_B = \frac{(I_E^{max} - I_E^{min})\,R_E + V_{BE}^{min} - V_{BE}^{max}}{I_{CO}^{max} - \frac{I_E^{max}}{h_{FE}^{max}+1} + \frac{I_E^{min}}{h_{FE}^{min}+1}} \tag{4f}$$

From equation (4c) the minimum collector to emitter voltage with no signal is

$$V_{CE}^{min} = V_C^{min} - I_{E\,max}\,(R_E + R_C) - i_{e\,max}\left(\frac{R_E\, r_E}{R_E + r_E} + \frac{R_E\, r_C}{R_C + r_C}\right) \tag{4g}$$

where i_e is the peak emitter current due to the signal, and r_E and r_C are the a.c. impedances respectively between the emitter and ground and the collector and ground.

The bias conditions (I_E, V_{CE}) may be determined by the application. For example, the transistor may be biased to obtain the lowest noise figure, optimize the gain, or the lowest possible supply drain. Because of the variations of small signal parameters and noise with operating point, the range or tolerance of the bias conditions may be determined by the amount the noise performance or gain are allowed to degrade. If the application does not determine the bias conditions, and if wide ambient temperatures are encountered, it is desirable to bias the transistor near the operating conditions given for the measurement of the small signal parameters.

Regardless of how the bias current is determined, the extremes of operating point are ultimately limited by the requirement that the transistor does not cut-off ($I_E = 0$) or saturate ($V_{CE} = 0$) under conditions of maximum input signal. The a.c. impedances seen by the collector and emitter are used in calculating the additional voltage drop due to the signal.

The procedure for determining the resistors and voltages of Figure 4.4 can best be described by a sample bias design.

1. Select the transistor type to be used (2N525).
2. Determine the required range of temperature.

   0°C to + 55°C

3. Determine I_{CO}^{max}.

   From the electrical specifications the upper limit of I_{CO} is 10 μa at 25°C and from Figure 1.25(A), I_{CO} will increase by a factor of 10 at 55°C, thus $I_{CO}^{max} = 10 \times 10 = 100\ \mu$a.

4. Determine the values of h_{FE}^{min} and h_{FE}^{max}

   From the electrical specifications, the range of h_{FE} at 25°C is 34 to 65. From Figure 1.26 h_{FE} can change by a factor of 0.83 at 0°C and by a factor of 1.45 at +55°C.

   Thus $h_{FE}^{min} = 0.83 \times 34 = 28$, and $h_{FE}^{max} = 1.45 \times 65 = 94$.

5. Determination of I_E and the range of I_E.

   The nominal bias condition is selected as 1 ma and 5 volts because the small signal parameters are specified here and the temperature range involved. The range of I_E is selected to be 0.6 ma to 1.4 ma since the change in small signal parameters is small over this current range. If we assume that the maximum input signal is 8 microamperes peak to peak, the maximum emitter current swing due to the signal occurs at 55°C and is $(h_{fe}^{max} + 1)\,I_b = 65 \times 1.3 \times 1.1 \times 8 = .75$ ma peak to peak or .375 ma peak. Thus the minimum value of bias current that has been selected is sufficient to keep the transistor from cutting off.

   The allowable range of emitter current must be narrowed to take into account the tolerance of the bias resistors. If the bias network has three resistors with a 5% tolerance, then

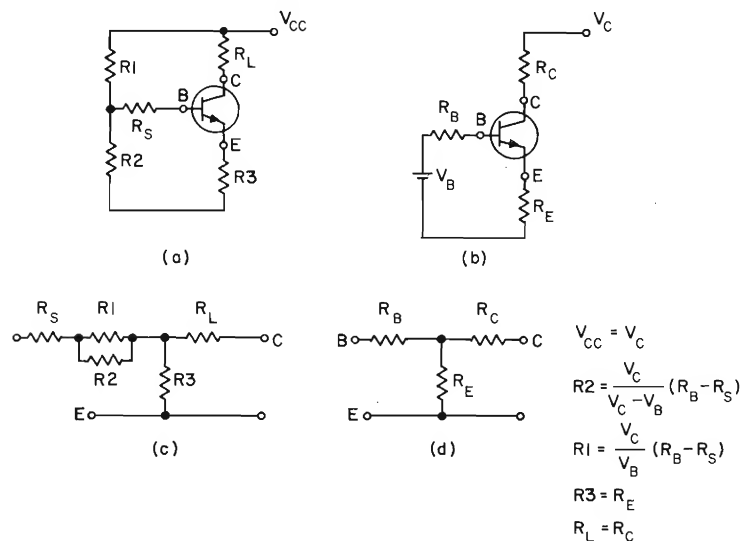
   $I_E^{min} = (1 + 3 \times .05)\,(.6) = .69$ ma and

   $I_E^{max} = (1 - 3 \times .05)\,(1.4) = 1.2$ ma.

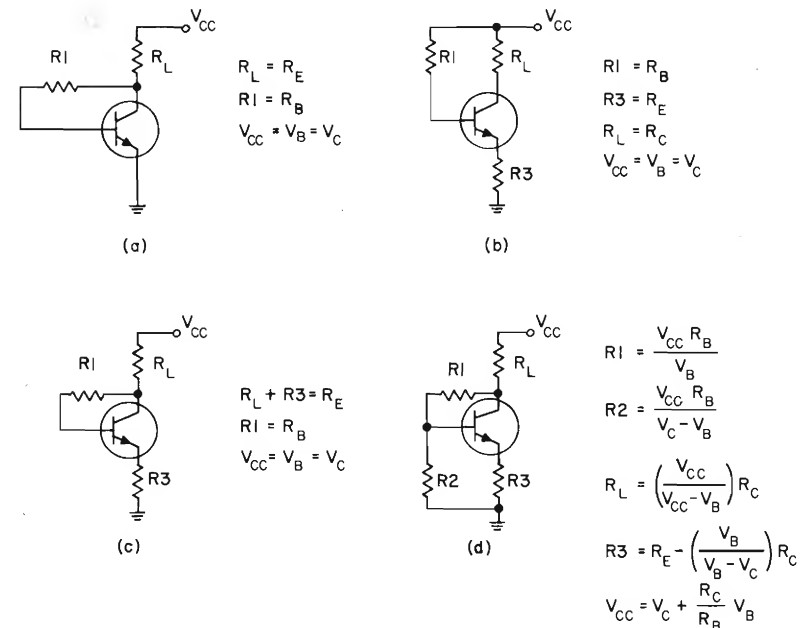
6. Since the V_{BE} temperature coefficient is about 2.5 mv/°C, $V_{BE\,max} - V_{BE\,min}$ can be estimated to be $2.5 \times 10^{-3} \times 55 = .135$ volt.
7. Calculate the value of R_B from equation (4f),
   $R_B = 4.6\,R_E - 1.2K.$
8. Using the equation from step 7, choose a suitable value of R_B and R_E. This involves a compromise since low values of R_E require a low value of R_B which shunts the input of the stage and reduces the gain. A high value of R_E reduces the collector to emitter bias voltage which limits the peak signal voltage across R_L, or for the same collector-emitter voltage, requires a higher V_C.
   Choose $R_E = 2.7K$ for which $R_B = 11.2K$.
9. Calculate V_B using equation (4d)
   $V_B = 2.32$ volts
10. Determine V_C and R_C.
   R_L and V_C must be chosen so that with the maximum bias current and peak signal the transistor does not saturate. However, an upper limit is set on V_C by the BV_{CER} rating of the transistor and the allowable power dissipation at the highest operating temperatures. The load resistor, R_C, is chosen to be as large as possible with the constraints given above.
   In our example the emitter is assumed to be bypassed so that the emitter to ground a.c. impedance is negligible. In addition, the collector is assumed to be a.c. coupled to a 500 ohm load. To effect a maximum transfer of signal to the load, $R_C >> 500$ ohms. R_C is thus selected to be 5K. Since the peak signal current is .375 ma and using equation (4g)

   $V_{C\,min} > (1.05)\,(5K + 2.7K)\,(1.4\text{ ma}) + .375\text{ ma} \times 453\,\Omega\,(1.05)$
   or
   $V_{C\,min} > 11.4 + .18 \approx 11.6$ volts

CONVERTING GENERAL BIAS CIRCUIT TO VOLTAGE DIVIDER TYPE

Figure 4.5

V_C is selected to be 15 volts. Once R_B, R_E, R_C, V_C and V_B of the general bias circuit are determined, the resistor and supply voltage of a particular bias circuit can be calculated. This is accomplished by equating between the bias circuits: 1) the transistor open circuit terminal voltages, and 2) the equivalent terminal resistances with the supply voltages shorted. For example, Figure 4.5 shows how the voltage divider bias network of Figure 4.3(c) is determined in terms of the general bias circuit. The open circuit collector-emitter voltages are V_{CC} and V_C, respectively, while the open circuit base-emitter voltages are $(R_2/R_1 + R_2)\,V_{CC}$ and V_B, respectively. The equivalent resistance network of the circuits with the power supplies shorted are shown in Figure 4.5(c) and (d). From inspection $R_C = R_L$, $R_3 = R_E$, and $R_S + R_1\,R_2/R_1 + R_2 = R_B$. Using these relationships and the voltage relationship given above, the values of the bias resistors and voltages are calculated as shown in Figure 4.5(d). The same relationship for other types of bias circuits are given in Figure 4.6.

BIAS CIRCUIT VALUES IN TERMS OF GENERAL BIAS PARAMETERS

Figure 4.6

Thus far, it has been assumed that the supply voltage V_{CC} is relatively constant. There are many applications, where batteries are used and where the circuit is expected to operate with a 50% drop in supply voltage. In addition, the battery drain must be kept small and a minimum of components must be used (for example, a portable radio).

In this case, the voltage divider circuit of Figure 4.5 with R_3 small or zero is usually used with germanium transistors. However, it has been found[2] that the constant base drive of Figure 4.6(b) is required when silicon transistors are used. The reason for

this is that the V_{BE} characteristic of silicon transistors has a steeper slope than it does for germanium transistors. The disadvantage of this circuit, however, is that the stage gain and bias point are more susceptible to h_{FE} variations. Another approach to biasing silicon transistors for this type of application is to use a separate battery for the bias supply. Since the drain is greatly reduced, the life of the bias battery will be several times larger than that of the collector supply battery.

BIASING OF MULTISTAGE AMPLIFIERS

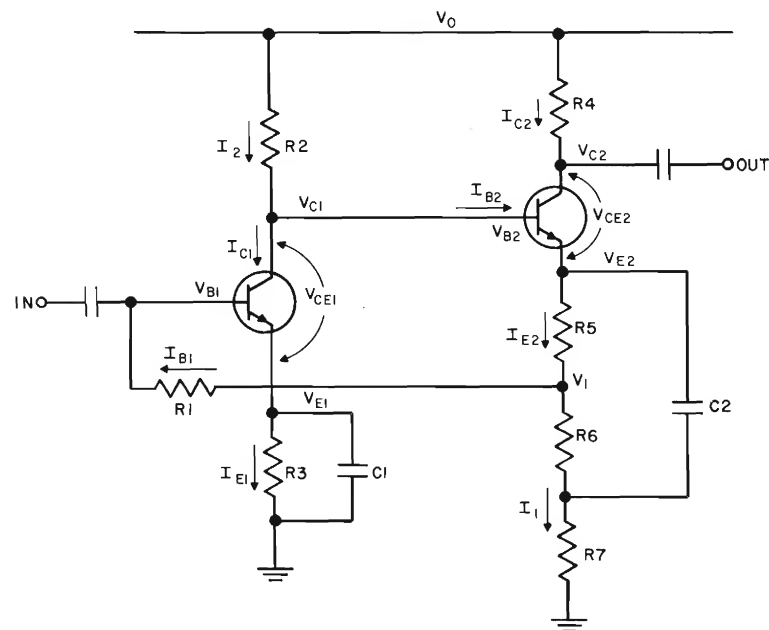
Frequently, in biasing an amplifier, it becomes necessary to use techniques by which higher input impedance or better stability are obtained than afforded by the circuits already shown. Many different schemes have been used to accomplish these purposes and the degree of complexity of any one method depends largely upon the factors listed earlier in this chapter. In any design, however, considerations similar to those in the example shown above must govern the circuit values chosen. Some of the bias methods for two and three stage direct coupled amplifiers are shown in Figures 4.7, 4.8, and 4.9.

DIRECT COUPLED AMPLIFIER

Figure 4.7

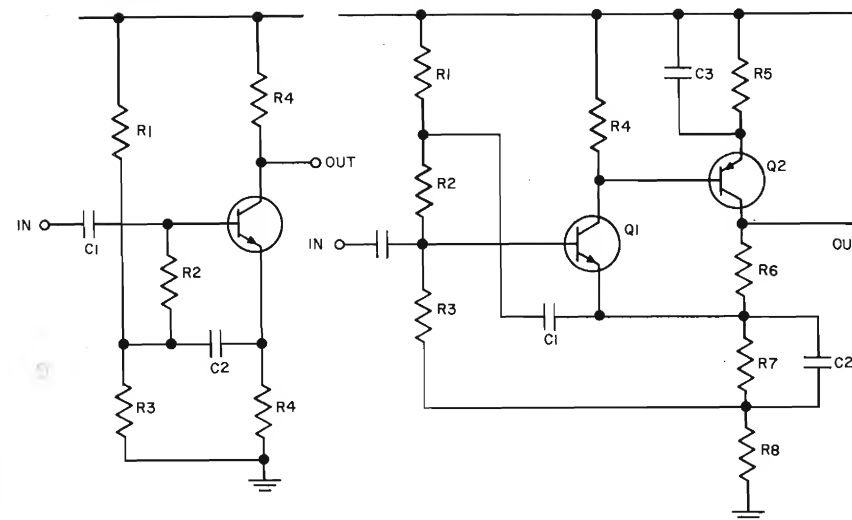
In Figures 4.7 and 4.8, biasing techniques are used which will improve the input impedance of the amplifier being designed. In Figure 4.7, the ac feedback through R_1 is essentially eliminated by the existence of C_2. R_1 can therefore be quite small in order to obtain good temperature stability for the amplifier. In Figure 4.8 bootstrapping techniques are used. Here the ac and dc feedback are quite large. Temperature stability and input impedance can be optimized but the gain of the circuit is sacrificed for increased input impedance.

BOOTSTRAPPED AMPLIFIERS

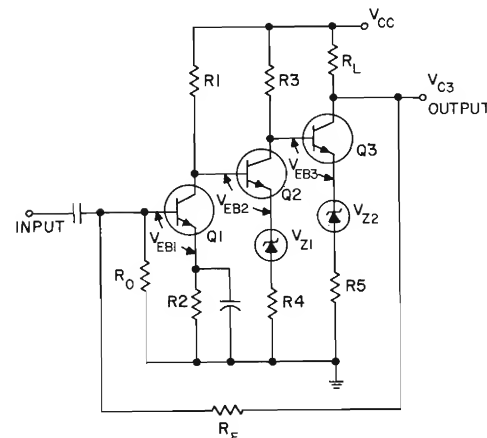
Figure 4.8

3-STAGE COMMON EMITTER DIRECT COUPLED AMPLIFIER

Figure 4.9

Two-stage Biasing Analysis

As an example of biasing considerations for a direct coupled amplifier, the circuit of Figure 4.7 is considered. As with single stage circuits, the bias can be established

using a "rule of thumb" procedure (as shown in Chapter 9) or it can be done analytically. *In the analytical derivation for Figure 4.7 which follows, R_6 and R_7 are combined and called R_6' since only the dc conditions are of interest.* Nodal equations can be written for this bias scheme:

$$I_2 = I_{C1} + I_{B2} \tag{4h}$$

$$I_{B1} + I_{C1} = I_{E1} \tag{4i}$$

$$I_{B2} + I_{C2} = I_{E2} \tag{4j}$$

$$I_{E2} = I_{B1} + I_1 \tag{4k}$$

Again, these currents are those which one would measure in the lines in which they flow. In addition to these equations, two more equations can be written which depend upon the transistor's action.

$$I_{C1} = h_{FE1} I_{B1} + (h_{FE1} + 1) I_{CO1} \tag{4l}$$

$$I_{C2} = h_{FE2} I_{B2} + (h_{FE2} + 1) I_{CO2} \tag{4m}$$

The relationships between the voltages, resistors, and currents in the circuit are

$$I_2 = \frac{V_0 - V_{C1}}{R_2} \tag{4n}$$

$$I_{B1} = \frac{V_1 - V_{B1}}{R_1} \tag{4o}$$

$$I_{E1} = \frac{V_{E1}}{R_3} \tag{4p}$$

$$I_{C2} = \frac{V_0 - V_{C2}}{R_4} \tag{4q}$$

$$I_{E2} = \frac{V_{E2} - V_1}{R_5} \tag{4r}$$

$$I_1 = \frac{V_1}{R_6} \tag{4s}$$

Substituting these voltage and resistor values into the node equations, and eliminating I_{C1} and I_{B2} by use of the transistor equations (4l) and (4m), the following results

$$\frac{V_0 - V_{C1}}{R_2} = h_{FE1}\left(\frac{V_1 - V_{B1}}{R_1}\right) + (h_{FE1} + 1) I_{CO1} + \frac{V_0 - V_{C2}}{h_{FE2} R_4} - \left(\frac{h_{FE2} + 1}{h_{FE2}}\right) I_{CO2} \tag{4t}$$

$$(1 + h_{FE1})\left(\frac{V_1 - V_{B1}}{R_1} + I_{CO1}\right) = \frac{V_{E1}}{R_3} \tag{4u}$$

$$\left(\frac{V_0 - V_{C2}}{R_4} - I_{CO2}\right)\left(1 + h_{FE2}\right) = h_{FE2}\left(\frac{V_{E2} - V_1}{R_5}\right) \tag{4v}$$

$$\frac{V_{E2} - V_1}{R_5} = \frac{V_1 - V_{B1}}{R_1} + \frac{V_1}{R_6'} \tag{4w}$$

To these equations, other transistor voltage relationships can be written

$$V_{E1} + V_{CE1} = V_{C1} \tag{4x}$$

$$V_{E2} + V_{CE2} = V_{C2} \tag{4y}$$

$$V_{E1} + V_{BE1} = V_{B1} \tag{4z}$$

$$V_{E2} + V_{BE2} = V_{B2} = V_{C1} \tag{4aa}$$

There are now eight independent equations (4t) through (4aa) relating the voltage and resistance values of the circuit. The circuit requirements of the particular design now govern the remainder of the design procedure. All of the above equations are true at all temperature extremes. The stability problem arises since the values of I_{CO} and h_{FE} change as a function of temperature. As these values change, the voltage and

current relationships within the circuit must also change so that equations (4l) through (4aa) are satisfied. In practical design, for example, the specifications for the amplifier normally demand that the output be capable of a specific voltage excursion. This peak to peak allowable swing at the collector of the output transistor can theoretically equal the supply voltage, if the bias voltage, V_{C2}, is exactly $V_0/2$. Maintaining V_{C2} exactly over the range of h_{FE} and I_{CO} is essentially impossible, and thus the output voltage excursion must be somewhat less than the supply voltage so that limiting does not occur on the output waveform as the bias level changes. At the lowest temeperature of interest, the emitter currents will be a minimum and the worst conditions would occur for $h_{FE} = h_{FE}^{min}$, V_{BE}^{max}, and $I_{CO} = 0$. At high temperature, the emitter currents will have a maximum value, and the worst case is encountered for $h_{FE} = h_{FE}^{max}$, $V_{BE} = V_{BE}^{min}$, and $I_{CO} = I_{CO}^{max}$.

The choosing of resistor values throughout the circuit is normally accomplished by considering circuit requirements in conjunction with transistor operating conditions. Equations (4h) through (4s) may also be of value in selecting resistors. A perfectly general biasing scheme is difficult to describe since individual circuit requirements play an important role in every amplifier. A general method of checking the values of resistance chosen could be worked out by solving equations (4t) through (4aa) for V_{C2} by eliminating all voltages except V_0, V_{BE1}, and V_{BE2}. The resulting equation will be of the form

$$V_{C2} = \frac{K_1 V_0 + K_2 V_{BE1} + K_3 V_{BE2} + K_4 I_{CO1} + K_5 I_{CO2}}{K_6} \tag{4bb}$$

If no approximations are made, these constants can be quite lengthy. For the case of Figure 4.7 the constants are

$$K_1 = \frac{(1 + h_{FE2}) R_6'}{R_4}\left[R_5\left(1 + \frac{R_A}{R_6'}\right) + R_A + h_{FE1} R_2\right] - R_A\left(h_{FE2} - \frac{R_2}{R_4}\right) \tag{4cc}$$

$$K_2 = -h_{FE2}(h_{FE1} R_2 - R_6') \tag{4dd}$$

$$K_3 = h_{FE2} R_A \tag{4ee}$$

$$K_4 = h_{FE2}(1 + h_{FE1})(R_B + R_1 R_2) \tag{4ff}$$

$$K_5 = -(1 + h_{FE2})\left[(1 + h_{FE1})(R_3 R_5 + R_B) + (R_1 R_2 + R_C)\right] \tag{4gg}$$

$$K_6 = \frac{(1 + h_{FE2}) R_6'}{R_4}\left[R_5\left(1 + \frac{R_A}{R_6'}\right) + R_A + h_{FE1} R_2\right] + \frac{(R_A + R_6') R_2}{R_4} \tag{4hh}$$

where,

$$R_A = R_1 + (1 + h_{FE1}) R_3 \tag{4ii}$$

$$R_B = R_2 R_3 + R_2 R_6' + R_3 R_6' \tag{4jj}$$

$$R_C = R_1 R_5 + R_1 R_6' + R_5 R_6' \tag{4kk}$$

By calculating the value of V_{C2} using the worst case values for h_{FE}, V_{BE}, and I_{CO} at the temperature extremes the variation in V_{C2} with temperature can be checked. Though this procedure is tedious, one is able to determine the stability of any given amplifier using steps similar to those outlined for the circuit of Figure 4.7.

Because of the circuit configuration used in this example, other types of bias schemes can also be analyzed by setting some of the resistor values at zero. Two different bias schemes would call for the following resistor changes: $R_5 = 0$; or $R_6 = 0$, and R_1 represents resistance seen at the base by the first transistor.

Three-stage Biasing Analysis

A general purpose 3-stage direct coupled amplifier is shown in Figure 4.9. The purpose of the zener diodes V_{Z1} and V_{Z2} is to provide sufficient collector to emitter voltage

for the preceding stage. In some cases they could be eliminated, or replaced by a forward biased diode. Using the method of analysis given for the two stage amplifier, the collector voltage of Q_3 is

$$V_{C3} = \frac{1}{K_O}\left[K_1 V_{CC} + K_2 V_{EB1} + K_3 V_1 + K_4 V_2 + K_5 I_{CO1} + K_6 I_{CO2} + K_7 I_{CO3}\right] \quad (4ll)$$

where $V_1 = V_{EB2} + V_{Z1}$ and $V_2 = V_{EB3} + V_{Z2}$

The coefficients K_O ...... K_7 are given in Table 4.1. For the case where $R_1 >> h_{FE2} R_4$, $R_3 >> h_{FE3} R_5$, and $h_{FE1} R_2 >> R_O$, the expression becomes

$$V_{C3} = \frac{R_2 (R_F + R_O)}{R_O R_1}\left(V_{CC} + \frac{R_1}{R_2} V_{EB1} - V_1 + \frac{R_O R_1 V_2}{h_{FE3} R_2 R_3}\right) - \frac{R_F (R_O + R_2) I_{CO1}}{R_O}$$
$$+ \frac{R_2 (R_F + R_O)}{R_O}\left(I_{CO2} - \frac{I_{CO3}}{h_{FE3}}\right) \quad (4mm)$$

The ac gain and frequency stability considerations are given in Chapter 9.

$$K_0 = 1 + \frac{R_L (\beta_1 R_2 + R_O)}{(\beta_1 R_2 + R_O) R_F + \beta_1 R_O R_2} + Z R_L$$

$$K_1 = 1 + \frac{[\beta_2 (R_3 - R_4) - R_1] \beta_3 R_L}{(R_1 + \beta_2 R_4)(R_3 + \beta_3 R_5)}$$

$$K_2 = \frac{R_L (R_O + R_F) Z}{R_O} + \frac{R_L R_O}{(\beta_1 R_2 + R_O) R_F + \beta_1 R_2 R_O}$$

$$K_3 = - \frac{\beta_2 \beta_3 R_L R_3}{(R_1 + \beta_2 R_4 \times R_3 + \beta_3 R_5)}$$

$$K_4 = \frac{R_L \beta_3}{R_3 + \beta_3 R_5}$$

$$K_5 = - \frac{R_L R_F (R_O + R_2) Z}{R_O}$$

$$K_6 = \frac{(R_4 + R_1)(R_L R_3 \beta_2 \beta_3)}{(R_1 + \beta_2 R_4)(R_3 + \beta_3 R_5)}$$

$$K_7 = - \frac{\beta_3 R_3 R_L}{R_3 + \beta_3 R_5}$$

where $$Z = \frac{R_O R_1 R_3 \beta_1 \beta_2 \beta_3}{[R_2 R_O \beta_1 + R_F (R_2 \beta_1 + R_O)](R_1 + \beta_2 R_4)(R_3 + \beta_3 R_5)}$$

and

$\beta_1 = h_{FE1}$

$\beta_2 = h_{FE2}$

$\beta_3 = h_{FE3}$

Table 4.1

NONLINEAR COMPENSATION

In the previous section, the bias point was maintained by employing feedback. It is possible to stabilize the bias point for temperature variations by using nonlinear components or another transistor (as shown under DC AMPLIFIERS). The nonlinear components to be discussed in this chapter compensate only for temperature changes and are not effective for the variation of transistor parameters between units or with life.

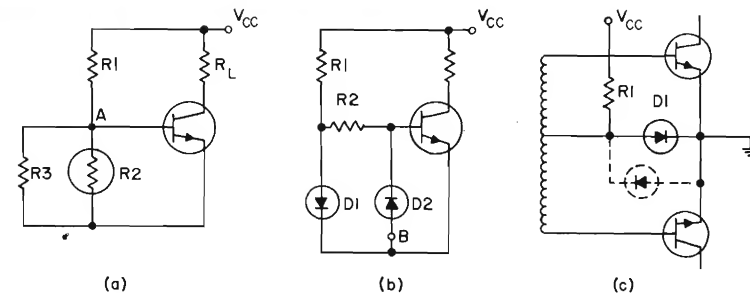
Figure 4.10(a) shows a circuit where a thermistor, R_2, in parallel with a fixed resistor R_3 is used to compensate for the transistor leakage current, V_{BE}, and gain variation with temperature. Since the thermistor has a negative temperature coefficient, it will reduce the base-emitter voltage with increasing temperature. The temperature coefficient and values of resistors are usually determined experimentally.

NONLINEAR TEMPERATURE COMPENSATION

Figure 4.10

A similar compensation technique which can be used with germanium transistors is shown in Figure 4.10(b). Diode D_1 (a silicon diode) is forward biased and compensates for the transistor V_{BE} variations. D_2 is a germanium diode (it could be the collector-base junction of a transistor of the same kind that is being used) which compensates for I_{CO} variations. Because I_{CO} is voltage sensitive, more perfect compensation is obtained if point B of D_2 were returned to a minus voltage equal to the collector voltage of the transistor. If silicon transistors are used, diode D_2 could be eliminated. Because of the low impedance presented by D_1, the signal would have to be inserted in series with the base – this can be accomplished with transformer coupling.

Diodes can also be used to compensate for V_{BE} variations of push-pull amplifiers as shown in Figure 4.10(d). The stages are generally biased Class AB in order to eliminate crossover distortion. If the stages were biased Class B (no quiescent current) the input signal would have to exceed the transistor V_{BE} before any appreciable collector current would flow. The d.c. current through the diode must be larger than the maximum peak signal current if the diode is not to cut off during the negative half cycle of the signal. By placing another diode as shown by the dotted line, the diode bias current can be reduced since the second diode will conduct for the negative half cycle of the signal.

THERMAL RUNAWAY

When a transistor is used at high junction temperatures (high ambient temperatures and/or high power dissipation) it is possible for regenerative heating to occur which will result in thermal run-away and possible destruction of the transistor. In any circuit the junction temperature (T_J) is determined by the total power dissipation in the transistor (P), the ambient temperature (T_A), and the thermal resistance (K).

$$T_J = T_A + KP \quad (4nn)$$

If the ambient temperature is increased, the junction temperature would increase an equal amount provided that the power dissipation was constant. However, since both h_{FE} and I_{CO} increase with temperature, the collector current can increase with increasing temperature which in turn can result in increased power dissipation. Thermal runaway will occur when the rate of increase of junction temperature with respect to the power dissipation is greater than the thermal resistance ($\Delta T_J/\Delta P > K$).

Thermal run-away is generally to be avoided since it can result in failure of the circuit and possibly in destruction of the transistor. By suitable circuit design it is possible to ensure either that the transistor can not run away under any conditions or that the transistor can not run away below some specified ambient temperature. A dif-

ferent circuit analysis is required depending on whether the transistor is used in a linear amplifier or in a switching circuit.

In switching circuits such as those described in Chapter 6, it is common to operate the transistor either in saturation (low collector to emitter voltage) or in cutoff (base to emitter reverse biased). The dissipation of a transistor in saturation does not change appreciably with temperature and therefore run-away conditions are not possible. On the other hand, the dissipation of a transistor in cutoff depends on I_{CO} and therefore can increase rapidly at higher temperatures. If the circuit is designed to ensure that the emitter to base junction is reverse biased at all temperatures (as for the circuit of Figure 4.11) the following analysis can be used

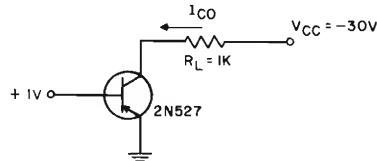



Figure 4.11

The transistor power dissipation will be

$$P = I_{CO}V_{CE} = I_{CO}(V_{CC} - I_{CO}R_L) = I_{CO}\,V_{CC} - I_{CO}^2\,R_L \qquad (4oo)$$

The rate of change of power dissipation with temperature will be

$$\frac{dP}{dT} = \frac{dP}{dI_{CO}} \cdot \frac{dI_{CO}}{dT} = (V_{CC} - 2I_{CO}R_L)\,\delta I_{CO} \qquad (4pp)$$

where $\delta \cong 0.08$ is the fractional increase in I_{CO} with temperature. The condition for run-away occurs when $dP/dT = 1/K$ or,

$$(V_{CC} - 2I_{COM}R_L)\,\delta I_{COM} = 1/K \qquad (4qq)$$

where I_{COM} is the value of I_{CO} at the run-away point. Solving for I_{COM} gives

$$I_{COM} = \frac{V_{CC} \pm \sqrt{(V_{CC})^2 - (8R_L)/(\delta K)}}{4R_L} \qquad (4rr)$$

In this equation the solution using the negative sign gives the value of I_{COM}, while the solution using the positive sign gives the value of I_{CO} after run-away has occurred. It is seen from the equation that the value of I_{CO} after run-away can never be greater than $V_{CC}/2R_L$ so that the collector voltage after run-away can never be less than one half of the supply voltage V_{CC}. If the term under the square root sign in the above equation is zero or negative, thermal run-away cannot occur under any conditions. Also, if thermal run-away does occur it must occur when the collector voltage is greater than $0.75V_{CC}$, since, when the term under the square root sign is zero, $I_{COM}\,R_L$ equals $0.25\,V_{CC}$. As R_L goes to 0, the solution for I_{COM} using the negative sign is indeterminant, i.e., equal to 0/0. In this case Equation (7mm) is used and

$$I_{COM} = \frac{1}{\delta\,K\,V_{CC}} \qquad (4ss)$$

Since no R_L exists, the current after thermal runaway is theoretically infinite, and the transistor will be destroyed unless some other current limiting is provided. Once the value of I_{COM} is determined from Equation (4rr) or (4ss) the corresponding junction temperature can be determined from a graph such as Figure 1.25. The heating due to I_{COM} is found by substituting I_{COM} for I_{CO} in equation (4oo). Finally, the ambient tem-

perature at which run-away occurs can be calculated from Equation (4nn).

In circuits which have appreciable resistance in the base circuit such as the circuit of Figure 4.12 the base to emitter junction will be reverse biased only over a limited temperature range. When the temperature is increased to the point where the base to emitter junction ceases to be reverse biased emitter current will flow and the dissipation will increase rapidly. The solution for this case is given by

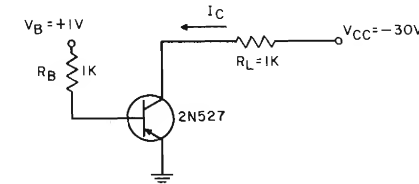



Figure 4.12

$$I_{COM} = \frac{(V_{CC} - 2R_Lh_{fe}I_x) \pm \sqrt{(V_{CC} - 2R_Lh_{fe}I_x)^2 - (8R_L)/(\delta K)}}{4R_Lh_{fe}} \qquad (4tt)$$

where $I_x = V_B/R_B$. When R_L approaches 0.

$$I_{COM} = \frac{1}{h_{FE}\,\delta\,K\,V_{CC}} \qquad (4uu)$$

In the analysis of run-away in linear amplifiers it is convenient to classify linear amplifiers into preamplifiers and power amplifiers. Preamplifiers are operated at low signal levels and consequently the bias voltage and current are very low particularly in stages where good noise performance is important. In capacitor coupled stages a large collector resistance is used to increase gain and a large emitter resistance is used to improve bias stability. Accordingly, thermal run-away conditions are seldom met in preamplifier circuits.

In contrast, power amplifiers invariably require transistors to operate at power levels which are near the run-away condition. The conditions are aggravated by the use of biasing networks of marginal stability which are required for power efficiency and by the use of transformer coupling to the load which reduces the effective collector series resistance. Since thermal run-away in power stages is likely to result in destruction of the transistors, it is wise to use worst case design principles to ensure that thermal run-away cannot occur. The worst case conditions are with $h_{fe} \rightarrow \infty$, $V_{BE} = 0$, $R_L = 0$, and $I_{CO} = I_{CO}^{max}$. If these conditions are applied to a transistor in the general bias circuit shown in Figure 4.13 the total transistor dissipation is given by:

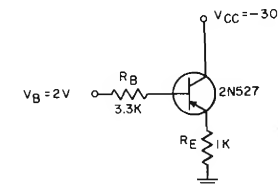



Figure 4.13

$$P = V_{CE}I_C = (V_{CC} - V_B - I_{CO}R_B)\left(I_{CO} + \frac{V_B + I_{CO}R_B}{R_E}\right) \qquad (4vv)$$

Equating dP/dT with 1/K and solving for I_{COM} as before,

$$I_{COM} = \frac{(V_{CC} - R_1V_B) \pm \sqrt{(V_{CC} - R_1V_B)^2 - (R_2)/(\delta K)}}{4R_B} \qquad (4ww)$$

where

$$R_1 = \frac{R_E + 2R_B}{R_E + R_B} \qquad R_2 = \frac{8R_ER_B}{R_E + R_B}$$

As before, the solution of equation (4ww) using the negative sign gives the value of I_{COM}, while the solution using the positive sign gives the final value of I_C after run-away has occurred. If the quantity under the square root sign is zero or negative, run-away cannot occur under any conditions.

In class B power amplifiers the maximum transistor power dissipation occurs when the power output is at 40% of its maximum value at which point the power dissipation in each transistor is 20% of the maximum power output. In class A power amplifiers on the other hand, the maximum transistor dissipation occurs when there is no applied signal. The maximum power dissipation is obtained by substituting I_{COM} in equation (4vv) and the maximum junction temperature is obtained from equation (4nn).

In the design of power amplifiers the usual procedure is to design the circuit to meet the requirements for gain, power output, distortion, and bias stability as described in the other sections of this manual. The circuit is then analyzed to determine the conditions under which run-away can occur to determine if these conditions meet the operating requirements. As a practical example, consider the analysis of the class-A output stage of the Three Transistor Reflex Receiver shown in Chapter 15. The transistor is the 2N241A for which K = 250°C/watt and I_{CO}^{max} = 16μa at 25°C and 25 volts. Calculating the circuit values corresponding to Figure 4.13 and equation (4ww)

$$V_{CC} = 9 \text{ v}, \quad R_E = 100\ \Omega$$

$$V_B = \frac{(1000)(9)}{1000 + 4700} = 1.58 \text{ v} \qquad R_B = \frac{(1000)(4700)}{1000 + 4700} = 825\ \Omega$$

$$R_1 = \frac{100 + 2(825)}{100 + 825} = 1.89 \qquad R_2 = \frac{8(100)(825)}{100 + 825} = 713\ \Omega$$

Calculating I_{COM} from equation (7ss)

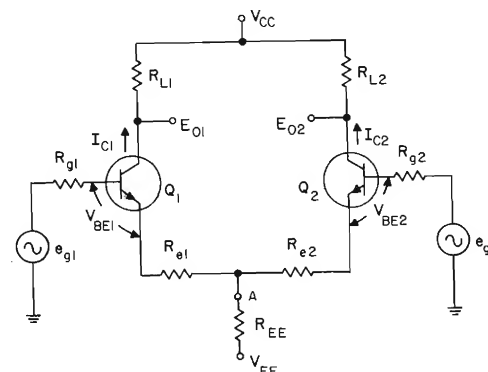
$$I_{COM} = \frac{6 \pm \sqrt{0.47}}{3300} = 1.61 \text{ ma or } 2.02 \text{ ma}$$

Since the quantity under the square root is positive, thermal run-away can occur. The two solutions give the value of I_{COM} (1.61 ma) and the value of I_{CO} after run-away has occurred (2.02 ma). The fact that these two currents are very nearly equal indicates that the change in power dissipation when run-away occurs will not be very large. Using the value I_{COM}/I_{CO}^{max} = 100 the junction temperature at run-away from Figure 1.25 is about 92°C. The dissipation at run-away, calculated from equation (4vv), is about 187 milliwatts. The rise in junction temperature due to this power dissipation is (0.25) (187) = 46.7°C. The ambient temperature at run-away is then calculated to be 92 − 46.7 = 45.3°C. The above value of maximum transistor power dissipation is calculated under the assumption that the series collector resistance is zero. In the circuit under consideration the transformer primary will have a small dc resistance (R_T) which will reduce the transistor power dissipation by approximately $(I_C)^2R_T$ where I_C is given by the second term in equation (4vv). Assuming that the dc resistance of the transformer is 20 ohms the reduction in power dissipation for the case just considered will be 18.8 milliwatts and the ambient temperature at run-away will be increased to 50.0°C.

DC AMPLIFIERS

TRANSISTOR REQUIREMENTS

In the previous section of this chapter it was shown that the variation of transistor dc parameters with temperature and life produced a corresponding change in the transistor bias conditions. Thus the transistor base current and/or voltage must be changed to return the collector voltage and current to their original value. It is this drift (the input necessary to return the output to its original value) that usually limits the minimum detectable dc signal. Feedback does not reduce the drift in a dc amplifier since the gain is also reduced proportionally.

Drift is reduced by compensation; and the most effective method found to date is the use of a second transistor in the emitter coupled circuit of Figure 4.14. The circuit will amplify single ended inputs (by setting $e_{g2} = 0$) or it will amplify the difference of isolated inputs ($e_{g1} - e_{g2}$). One feature of the circuit is that it tends to amplify only the difference of the two input signals and reject the signal common to both inputs. This property has been given the name of *common mode rejection*; it is defined as the amplifier gain with a differential input divided by the amplifier gain with both inputs tied together. It is usually given in db.

EMITTER COUPLED DIFFERENTIAL AMPLIFIER
Figure 4.14

Inspection of Figure 4.14 shows that both single and differential outputs are available. The single ended output presents more of a drift problem; however, the drift can be minimized by using multistage amplifiers with common mode feedback and a constant current emitter supply.

The transistor parameters which contribute to the drift are:

1. *Leakage current.* For silicon planar transistors, the leakage current can be as low as 1 na at 100°C (V_{CB} = 10V). Leakage current becomes a secondary drift factor unless the source resistance is very large.
2. *DC current gain.* Since $I_B = I_C/h_{FE} + 1$, a change in current gain results in a change in base current, which, multiplied by the source impedance, produces an equivalent voltage drift. The drift contribution of the h_{FE} variations can be reduced by the matching of the transistor current gains, by operating at low bias currents, and by using low source impedances. Planar transistors are available which have a current gain of 100 or more at collector currents of 10 and 100 μA. The current gains of two transistors can be matched to better than 10%.

3. *Base emitter voltage.* The base emitter voltages tend to cancel one another in the differential amplifier. However, the difference of the base emitter voltages is in series with the signal and cannot be distinguished from it. It is important not only to match the base emitter voltages, but to keep the transistors at the same temperature since the V_{BE} temperature coefficient is 2.5 mv/°C.

A method of maintaining the transistors of the differential amplifier at the same temperature is by mounting the transistor pellets on isolated islands of a header as shown in Figure 4.15. The degree of V_{BE} matching and the calculated temperature coefficient of one such transistor is shown in Figure 4.16. Notice that an initial V_{BE} match of 2.5 mv and a temperature coefficient of 3 μv/°C for the match are typical. Figure 4.17 shows how well the base emitter voltages and the current gains track with life. The percentile curves are shown for the severe life tests of 500 mw operating life and 300°C storage.

TO-5 PACKAGE
(a)

FLAT PACKAGE
(b)

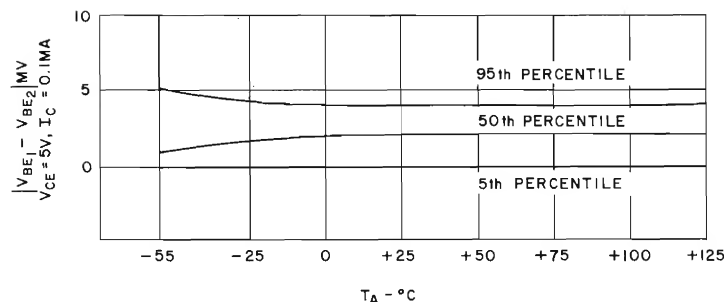
DIFFERENTIAL AMPLIFIER PACKAGE
Figure 4.15

(a) V_{BE} MATCH VS. TEMPERATURE FOR 2N2480 DIFFERENTIAL AMPLIFIER

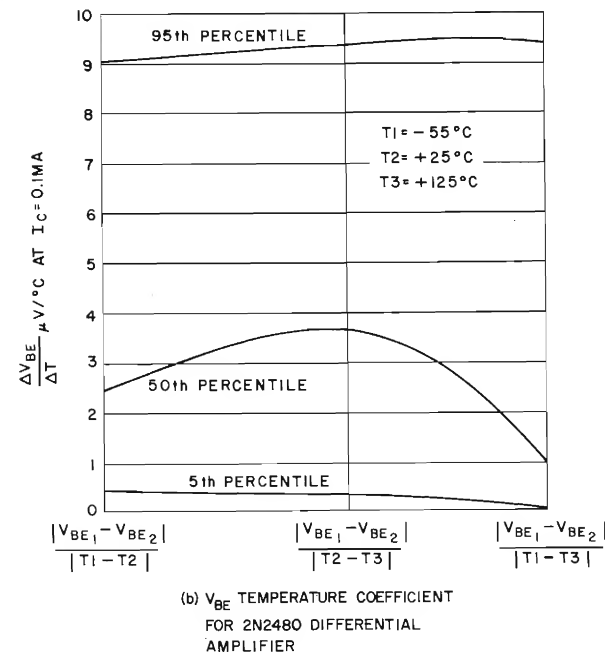
Figure 4.16 (a)

(b) V_{BE} TEMPERATURE COEFFICIENT FOR 2N2480 DIFFERENTIAL AMPLIFIER

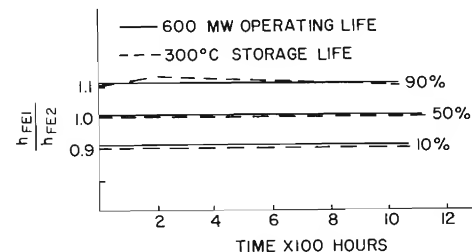
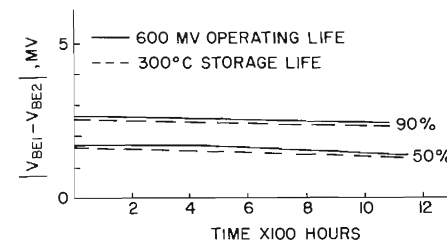
Figure 4.16 (b)

TYPICAL V_{BE} AND h_{FE} MATCH LIFE TEST DATA
Figure 4.17

Table 4.2 shows some of the important parameters and the degree of matching for three typical differential amplifier transistors which are commercially available.

Thus, with the excellent initial matching and tracking of silicon planar transistors with temperature and life, it is possible for most applications to design high performance dc amplifiers without resorting to chopped stabilization techniques.

TYPE NUMBER	G.E. 2N2480	G.E. 2N2652A	G.E. 2N2920
$V_{CEO\,min}$ (volts)	40	60	60
$I_{CBO\,max\,(na)}$ at 25°C ($V_{CB} > 30V$)	50	2	2
$h_{FE\,min}$			
at $I_C = 10\ \mu a$	—	—	150
at $I_C = 100\ \mu a$	20	35	225
at $I_C = 1$ ma	30	50	300
h_{FE} match, max			
at $I_C = 10\ \mu a$	—	—	—
at $I_C = 100\ \mu a$	20%	10%	10%
at $I_C = 1$ ma	20%	10%	—
V_{BE} match, max			
at $I_C = 10\ \mu a$	—	—	5 mv
at $I_C = 100\ \mu a$	10 mv	3 mv	3 mv
at $I_C = 1$ ma	10 mv	3 mv	5 mv
ΔV_{BE} Temp Coefficient, max	15 μv/°C	10 μv°/C	10 μv°/C

TYPICAL DIFFERENTIAL AMPLIFIER CHARACTERISTICS
Table 4.2

SINGLE STAGE DIFFERENTIAL AMPLIFIER

The circuit of Figure 4.14 has been analyzed in detail in the literature.[3,4] The single ended output voltage, E_{02}, for a differential input is given by[3]

$$\left[\frac{(e_{g2}-e_{g1})+(V_{BE1}-V_{BE2})+R_{g2}I_{CO2}-R_{g1}I_{CO1}-\left(\frac{R_{g1}}{h_{FE1}}+R_{E1}\right)\frac{V_{EE}}{R_{EE}}}{R_{e1}+R_{e2}+\frac{R_{g2}}{h_{FE2}}+\frac{R_{g1}}{h_{FE1}}+\frac{R_{g1}R_{g2}}{h_{FE1}h_{FE2}R_{EE}}}\right]-I_{CO2}R_{L2} \tag{4xx}$$

The differential output voltage[3]

$$E_{02}-E_{01}=K\left[(e_{g1}-e_{g2})+(V_{BE2}-V_{BE1})+(R_{g1}I_{CO1}-R_{g2}-I_{CO2})+\left(\frac{R_{g1}}{h_{FE1}}-\frac{R_{g2}}{h_{FE2}}+R_{e1}-R_{e2}\right)\frac{V_{EE}}{R_{EE}}\right]+I_{CO1}R_{L1}-I_{CO2}R_{L2} \tag{4yy}$$

where

$$K=\frac{R_{L1}+R_{L2}}{R_{e1}+R_{e2}+\frac{R_{g2}}{h_{FE2}}+\frac{R_{g1}}{h_{FE1}}+\frac{R_{g1}R_{g2}}{h_{FE1}h_{FE2}R_{EE}}}$$

If the transistors and external resistors are equal, the differential gain

$$A_{ddo}=\frac{E_{02}-E_{01}}{e_{g1}-e_{g2}}=\frac{2R_L}{R_E+\frac{R_g}{h_{FE}}\frac{1}{R_{EE}}\left(\frac{R_g}{h_{FE}}\right)^2} \tag{4zz}$$

where $R_E = R_E + r_E$, and r_E is the base-emitter junction dynamic impedance $\eta KT/qI_E$. For the case where $R_g/h_{FE} << R_E$, the gain becomes for a differential output

$$A_{ddo}=\frac{2R_L}{R_E} \tag{4aaa}$$

If $R_{EE} >> R_E$, the input resistance for a differential input is

$$R_{in}\approx(h_{FE}+1)R_E \tag{4bbb}$$

For a differential input and single ended output, or a single ended input and differential output, the gain is one half of that given by equations (4zz) and (4aaa). For a single ended input ($e_{g2} = 0$) the input resistance

$$R_{in}=(h_{FE1}+1)\,2R_{E1}+\frac{R_g}{(h_{FE2}+1)} \tag{4ccc}$$

The common mode gain for a differential output is given by ($e_{g1} = e_{g2} = e_g$)

$$A_{cdo}=\frac{E_{02}-E_{01}}{e_g}=\frac{K}{(R_{L1}+R_{L2})R_{EE}}\left[\frac{R_{L1}R_{g2}}{h_{FE2}}-\frac{R_{L2}R_{g1}}{h_{FE1}}\right] \tag{4ddd}$$

In the derivation of equation (4aaa) it was *not* assumed that the $R_g << h_{FE} R_E$.

If the circuit is perfectly balanced and the transistors are exactly alike, then the common mode gain is zero. If the source impedance and external resistances are equal, but the current gains are different, equation (4ddd) becomes

$$A_{cdo}=\frac{E_{02}-E_{01}}{e_g}=\frac{K}{2R_{EE}}\left(\frac{1}{h_{FE2}}-\frac{1}{h_{FE1}}\right) \tag{4eee}$$

and the common mode rejection then becomes

$$CMR=\frac{\text{Differential Gain}}{\text{Common Mode Gain}}=\frac{2R_{EE}h_{FE1}h_{FE2}}{R_g(h_{FE1}-h_{FE2})} \tag{4fff}$$

For a single ended output the common mode gain is

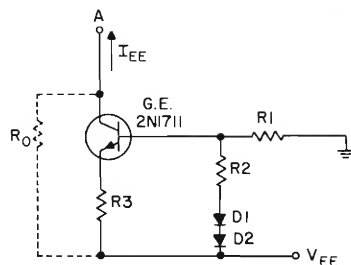
$$A_{cso}=\frac{R_{L1}}{R_{E1}+2R_{EE}} \tag{4hhh}$$

if $2 R_{EE} h_{fe1} >> R_g$.

The common mode rejection becomes for $R_{EE} >> R_{E1}$

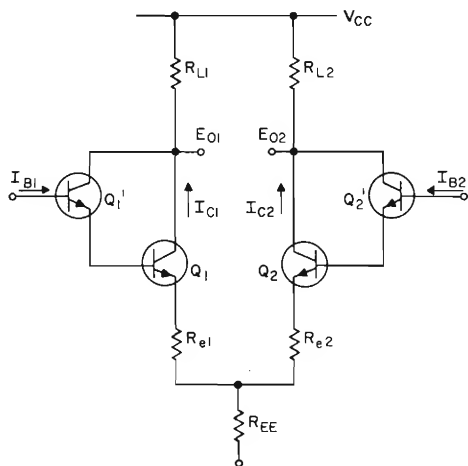
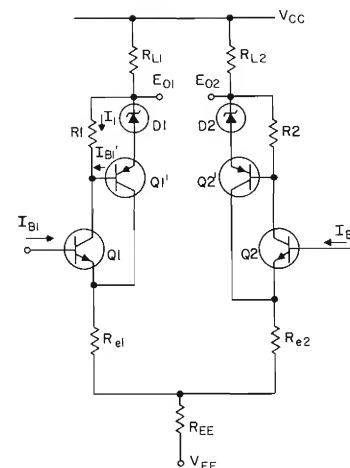
$$CMR=\frac{2R_{EE}}{R_{E1}+R_{E2}} \tag{4iii}$$

Thus to reduce the common mode gain and improve the common mode rejection, for both the single ended and differential output, R_{EE} should be as large as possible. As R_{EE} is increased, the operating currents must be decreased or V_{EE} must be increased. Another solution is to replace R_{EE} and V_{EE} by a constant current source as shown in Figure 4.18. For $R_1 = R_2$, $I_{EE} = V_{EE}/2\,R_3$, and the diodes D_1 and D_2 compensate for the V_{BE} variation of the transistor with temperature.

Because the temperature coefficient of a forward biased junction is a strong function of dc current for silicon (see Chapter 17), it is important that some care be exerted in selecting the transistors, the diodes, and current levels if an optimum compensation is desired. If the transistor is diffused and non-gold doped, the diodes should be the same and the current through the diodes should be selected to be equal to I_{EE}.

CONSTANT CURRENT SOURCE
Figure 4.18

The resistance shown in dashed lines is the output impedance of the circuit and is approximately the h_{ob} of the transistor. At low collector currents it is at least several megohms.

The common mode rejection as given in equations (4fff) and (4iii) assumed that only the current gains were not equal. The mis-matching of resistors also contribute to the common mode rejection; however, such a discussion is beyond the scope of this manual. For such a discussion the reader is referred to reference 4.

Examination of equation (4aaa) shows that the differential gain is proportional to R_L/R_E if $R_g/h_{FE} << R_E$. Thus an upper limit on gain and an upper limit on source impedance are set by the inequality. The gain or source impedance can be increased by increasing the current gain of the transistor. Figures 4.19 and 4.20 show circuits where the gain is increased by using additional npn and pnp transistors respectively. In the Darlington configuration of Figure 4.19, it is important that Q_1' and Q_2' have good current gain hold up at very low currents, have low collector capacitance, and low leakage. R_E of equations (4yy) and (4zz) becomes $2\, r_{E1} + R_{E1}$ where $r_{E1} = \eta KT/q\, I_{E1}$.

DARLINGTON SINGLE STAGE DIFFERENTIAL AMPLIFIER
Figure 4.19

NPN-PNP SINGLE STAGE DIFFERENTIAL AMPLIFIER
Figure 4.20

The current gain becomes $h_{FE1}\, h_{FE1}'$, where the current gains are measured at the respective bias currents of the two transistors. Since the base currents I_{B1} and I_{B2} have been reduced by the gain of Q_1' and Q_2' respectively, the drift due to current gain variation is considered reduced.

A complimentary circuit arrangement is used in Figure 4.20 to increase the gain.[5] The breakdown diodes D_1 and D_2 are chosen to have a positive temperature coefficient which cancels the base-emitter coefficients of Q_1' and Q_2'. The current gain of the transistor pair Q_1 and Q_1' is

$$h_{FE} = h_{FE1}\left(1 + h_{FE1}'\frac{I_{B1}'}{I_1}\right) \qquad (4jjj)$$

Thus to increase the gain, R_1 should be made large to reduce I_1. In the limit, it becomes infinite so that the base current of the pnp transistor becomes the collector current of the npn transistor, and the need for high current gain at low collector currents for the npn is also required. The input impedance of this circuit is also high since the collector current of the pnp transistors flows through the external emitter resistors.

TWO STAGE DIFFERENTIAL AMPLIFIER

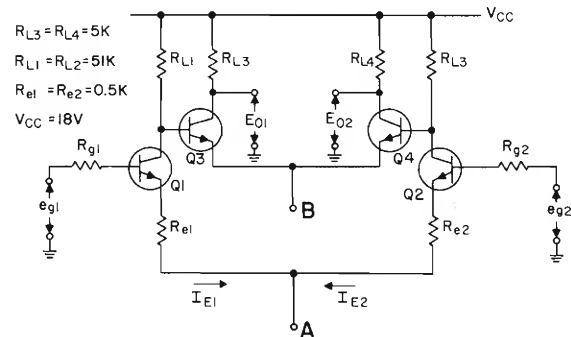
A basic two stage npn differential amplifier is shown in Figure 4.21. The emitters of the first and second stages have been returned respectively to terminals A and B since there are quite a number of possible terminations as shown in Figure 4.22. Some of the possible terminations when no common mode feedback is desired are shown in Figure 4.22(a) while some of the common mode feedback circuits are shown in Figure 4.22(b). Which of the terminations in Figure 4.22(a) are used depends upon the circuit applications, i.e., whether or not common mode signals exist, the magnitude of the input, etc.

The differential gain of the two stage amplifier is

$$A_{ddo} = \frac{V_{01} - V_{02}}{eg_1 - e_{g2}} = \frac{2\, h_{fe3}\, R_{L3}}{R_{E1}} \qquad (4kkk)$$

where $R_{E1} = R_{e1} + r_e$ and it is assumed that current gains and resistors on either side are equal, i.e., $h_{fe3} = h_{fe4}$, $R_{e1} = R_{e2}$ etc. Another assumption is that the input im-

pedance seen at the base of Q_1 and Q_2 is larger than the source impedance, R_g. Voltage gains of several thousand are possible since transistors with current gains of 100-400 at currents of 10-100μA are commercially available.

For most applications which require a single ended output, the circuit provides sufficient gain — one half of that given by (4kkk) — so that succeeding stages can be

(SEE FIGURE 4.22 FOR CIRCUIT CONNECTIONS TO POINTS A AND B)

BASIC NPN TWO STAGE DIFFERENTIAL AMPLIFIER

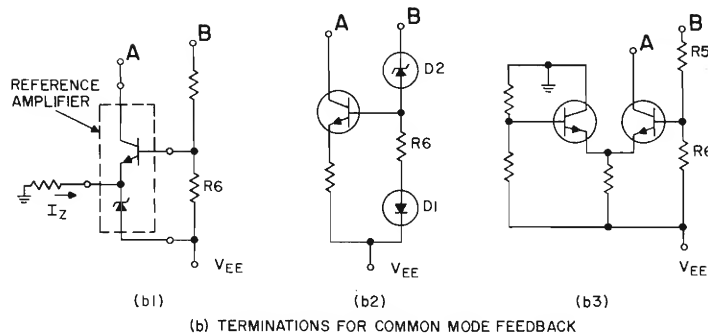
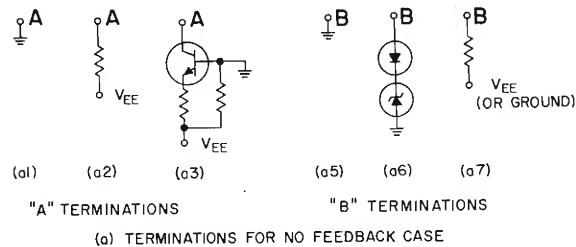
Figure 4.21

EMITTER TERMINATIONS FOR POINTS A AND B OF TWO STAGE DIFFERENTIAL AMPLIFIERS (FIG. 4.21)

Figure 4.22

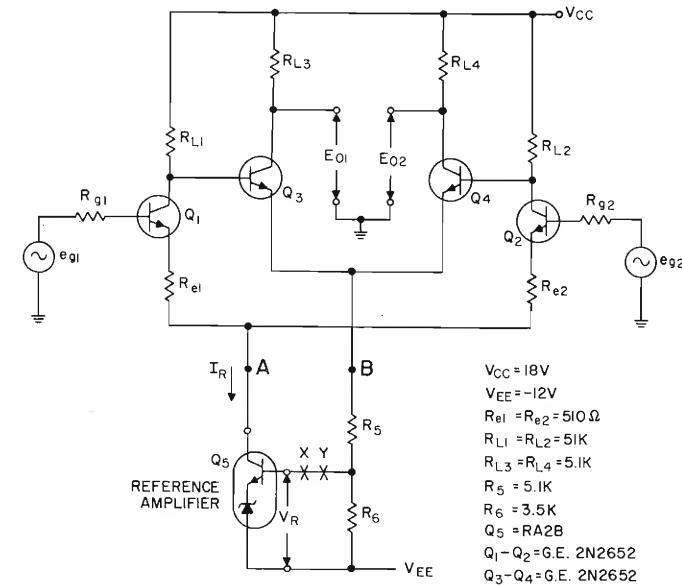
single ended. For example, the emitter-base junction of a single ended third stage reflects back to the input a drift of only 1-2 μv/°C. With a single ended output, the causes of drift are the power supply variations (especially the minus supply) and the variation of the emitter bias currents with temperature. The temperature drift of the bias circuits can be reduced significantly by the common mode feedback circuit of Figure 4.22(b1). This can best be explained by referring to the complete circuit diagram given by Figure 4.23.

TWO STAGE DIFFERENTIAL AMPLIFIER WITH COMMON MODE FEEDBACK

Figure 4.23

The voltage drop across R_6 due to the emitter currents of Q_3 and Q_4 is compared to the reference diode plus emitter-base voltage of the reference amplifier, Q_5. This latter voltage, V_R, is extremely stable with temperature and with life (a detailed explanation of the reference amplifier is given in Chapter 10). The error between V_R and the voltage drop across R_6 is converted into a current I_R by Q_5. This current is essentially the collector currents of the first stage of the differential amplifier, which in turn determines the emitter current of Q_3 and Q_4. If the RA2 series of reference amplifiers is used, the external zener current, I_Z, is not required, and the bias currents of Q_1 and Q_2 must be 250 μA. If the RA3 series is used, then a 5 ma external zener current must be supplied and Q_1 and Q_2 must be biased at 50 μA for optimum performance.

If the temperature coefficient of the reference amplifier is τ%/°C and the reference voltage is V_R, then the single ended output voltage temperature gradient is

$$\frac{\Delta V_{01}}{\Delta T} = \frac{\Delta V_{02}}{\Delta T} = \frac{V_R \tau}{100}\left(\frac{R_{L1}}{2\,R_6}\right) \qquad (4lll)$$

Thus for an RA2B and with the values of resistances given in Figure 4.23, the drift contribution due to the reference amplifier is only .25 m V/°C at the single ended

output or 0.25 μv/°C at the input if the amplifier gain is a thousand.

Because the voltage at point B in Figure 4.21 or 4.23 is proportional only to a common mode input voltage but does not change for a differential input, it can be amplified and fed back to the input so that the common mode gain is reduced but the differential gain is not affected. The feedback occurs via R_5, R_6, the reference amplifier, Q_1 and Q_2, and the base-emitter circuit of Q_3 and Q_4. The reference amplifier provides the circuit gain since Q_1 and Q_2 operate in the grounded base mode in this loop. The common mode loop gain is calculated by opening the circuit at some point, such as X-Y in Figure 4.23, with point Y terminated in an impedance equal to the input impedance of the reference amplifier. The loop gain is then the ratio of the current which flows in this terminating impedance to a current injected into point X. The common mode loop gain is

$$G_C \approx \frac{h_{fe5} R_{L1} R_6}{2 [R_5 R_6 + R_{in} (R_5 + R_6)]} \qquad (4mmm)$$

or

$$G_C \approx \frac{g_m R_{L1} R_6 R_{in}}{2 [R_5 R_6 + R_{in} (R_5 + R_6)]} \qquad (4nnn)$$

where g_m, h_{fe5}, and R_{in} are respectively the transconductance, ac current gain, and input resistance of the reference amplifier.

Without the common mode feedback (point X in Figure 4.23 returned to a dc voltage which biases the circuit properly) the common mode gain for a single ended output is approximately

$$A_{cso} = \frac{R_{L1} R_{L2} h_{or}}{4 R_5'} \qquad (4ooo)$$

where

$$R_5' = R_5 + \frac{R_6 R_{in}}{R_6 + R_{in}},$$

and h_{or} is the output admittance of the reference amplifier.

With common mode feedback, the common mode gain for a single ended output becomes

$$A_{cso}' = \frac{A_{cso}}{1 + G_C}. \qquad (4ppp)$$

In practice, the common mode gain obtained may not be as low as that given by equation (4ppp) because of a mis-match in h_{re} of Q_1 and Q_2. Even so, common mode gains as low as 3×10^{-3} and common mode rejections in excess of 100 db are easily obtained for the single ended output case.

REFERENCES

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(2) Snyder, G. E., "A High Performance Silicon Transistor for the Entertainment Industry," *IEE Transactions on Broadcast and Television Receivers*, Vol. BTR-9, No. 2, July 1963.

(3) Okada, R. H., "Stable Transistor Wide-Band D-C Amplifier," *Communications and Electronics*, March 1960.

(4) Middlebrook, R. D., *"Differential Amplifiers,"* John Wiley & Sons, New York, New York (1963).

(5) Hilbiber, D. F., "A New DC Differential Amplifier," *1961 International Solid State Circuits Conference*, pp. 44-45.

NOTES

LOGIC

CHAPTER 5

An understanding of the manner in which each circuit in a radio receiver operates is almost all that is required to achieve an understanding of how a receiver operates. The remaining residue of information needed to complete understanding is the order in which the circuits are connected. For the example chosen, the order is so obvious and simple that it could conceivably be deduced from an understanding of the circuits alone. Naturally other examples, such as radio transmitters, various test equipment, etc., could have been used.

More elaborate systems cannot be understood solely in terms of circuit operation. In general, as systems become more complex, understanding must be based more and more on the way in which circuits are interconnected and less attention need be given to the fine details of circuit operation. The particular circuit is only important to understanding as far as the function (amplify, oscillate, shape, etc.) it performs and not on how it performs that function.

The classical approach to electronic equipment has been to teach circuit theory and operation as fundamental and, if time permits, to use a simple block diagram to show how the circuits are interconnected. As a result, most of us are oriented in such a manner that we allot a disproportionate importance to circuitry and tend to consider organization as being of nominal importance.

Digital systems are representative of a class of systems where an understanding of the organization of circuitry is of far greater importance than an understanding of the circuit details. That is, a complete and thorough study of each individual circuit in a digital system will give virtually no clue to the operation of the system. A typical diagram of a portion of the system will contain "black" boxes labelled AND, OR, FLIP-FLOP, etc. It is totally immaterial to an *understanding* of the system whether the functions are synthesized with relays, vacuum tubes, magnetic cores, cryotrons, hydraulic valves, transistors, etc. Which of these devices will be used is determined by such things as size, cost, weight, power, and speed. Furthermore, quite different digital equipments can be built using identical circuits.

The purpose of this section is to discuss some of the concepts and techniques utilized in digital work in order to aid the circuit designer in visualizing some of the constraints and conditions placed upon switching circuits by the intended usage.

SWITCHING ALGEBRA

Consider the switch arrangement in Figure 5.1(a). If either switch A, *or* switch B, *or* both are operated, then the output will be the input voltage E. More than one switch may be operated to cause an output equal to the input as the only requirement is that at least one of the switches be thrown to obtain an output at F. This type of switch arrangement is called an OR gate. Figure 5.1(b) is one way of symbolizing any circuit which performs an OR function. Such a box need not be made up of mechanical switches only, but may be synthesized in many ways.

If a table is made of the possible combinations of switches A and B and the value of the output F for each of these combinations it would appear as shown in Figure 5.2(a). Since a switch has only two possible conditions or states, either closed or open, and the network can either have a closed or open path between input and output, it is common to use the symbol "0" to represent an open condition and a "1" to repre-

(a) MECHANICAL SWITCH ARRANGEMENT FOR OBTAINING THE OR FUNCTION.

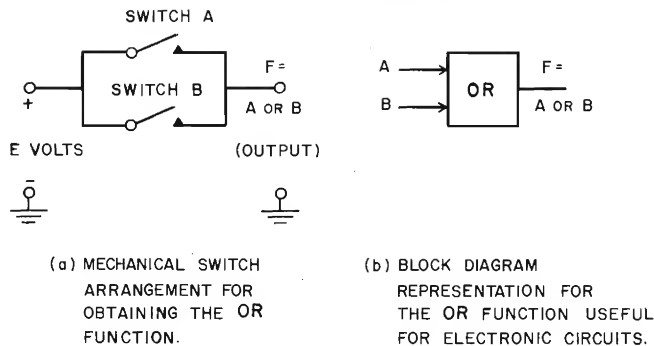
(b) BLOCK DIAGRAM REPRESENTATION FOR THE OR FUNCTION USEFUL FOR ELECTRONIC CIRCUITS.

THE OR FUNCTION

Figure 5.1

sent the closed condition. This use of "0" and "1" is different from that normally encountered in that these symbols *do not represent* numbers. They are simply used as a short hand for indicating the presence or absence of a conducting path. In a similar manner, the symbol "+" is used to indicate OR rather than the usual "plus" of ordinary arithmetic. The table of Figure 5.2(b), using these conventions, is sometimes called a truth table as well as a table of combinations. This is borrowed from abstract logic where "0" and "1" represent "false" and "true" respectively and $F = A + B$ would be interpreted as "statement F is true if *either* statement A *or* statement B (*or both*) is true."

A	B	F
OPEN	OPEN	0 VOLTS
CLOSED	OPEN	E VOLTS
OPEN	CLOSED	E VOLTS
CLOSED	CLOSED	E VOLTS

(a)

A	B	F=A+B
0	0	0
1	0	1
0	1	1
1	1	1

(b)

TABLE OF COMBINATIONS FOR THE SIMPLE OR GATE

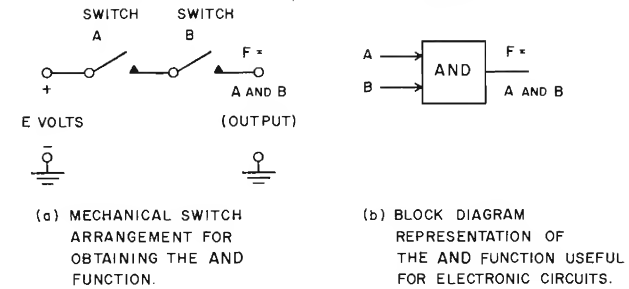
Figure 5.2

Consider now the case of series switches as shown in Figure 5.3(a). There will be a conducting path between input and output if, and only if, *both* A *and* B are closed. The symbol "•" is used to indicate the AND and again care should be used to prevent confusing this symbol with ordinary algebraic multiplication.

With the above concepts in mind, it is quite possible to set up an "algebra" to describe various switching arrangements. Keeping in mind that "0" represents an open path and "1" represents a conducting path we may write the first six results of Table 5.1 from the truth tables of Figures 5.2(b) and 5.3(c).

Notice, in Table 5.1, that $1 + 1 = 1$ does not appear at all like ordinary algebra. If we read "a conducting path or a conducting path is a conducting path," however, and visualize short circuits in place of the two switches in Figure 5.1(a), it is a meaningful and logical statement.

(a) MECHANICAL SWITCH ARRANGEMENT FOR OBTAINING THE AND FUNCTION.

(b) BLOCK DIAGRAM REPRESENTATION OF THE AND FUNCTION USEFUL FOR ELECTRONIC CIRCUITS.

A	B	F=A·B
0	0	0
1	0	0
0	1	0
1	1	1

(c) TABLE OF COMBINATIONS FOR THE AND FUNCTION.

SIMPLE AND FUNCTION

Figure 5.3

SIMPLE RELATIONS			
1. $0+0=0$	5. $0 \cdot 1=0$	9. $A+A=A$	13. $0+A=A$
2. $0 \cdot 0=0$	6. $0+1=1$	10. $A \cdot A=A$	14. $0 \cdot A=0$
3. $1+1=1$	7. $\overline{0}=1$	11. $\overline{A} \cdot A=0$	15. $1+A=1$
4. $1 \cdot 1=1$	8. $\overline{1}=0$	12. $\overline{A}+A=1$	16. $1 \cdot A=A$
LAWS			
COMMUTATIVE	ASSOCIATIVE	DISTRIBUTIVE	
17. $A+B=B+A$	19. $(A+B)+C=A+(B+C)$	21. $A \cdot (B+C)=A \cdot B+A \cdot C$	
18. $A \cdot B=B \cdot A$	20. $(A \cdot B) \cdot C=A \cdot (B \cdot C)$		
SIMPLIFICATION RULES			
22. $A+A \cdot B=A$	25. $(\overline{A \cdot B})=\overline{A}+\overline{B}$ (NAND)	DeMORGAN'S THEOREM	
23. $A+\overline{A} \cdot B=A+B$	26. $(\overline{A+B})=\overline{A} \cdot \overline{B}$ (NOR)		
24. $A \cdot (A+B)=A$			

USEFUL RELATIONSHIPS

Table 5.1

Since "0" and "1" are the only two possible values we may have, it follows that "not 0" (written $\overline{0}$) must be "1" and "not 1" (written $\overline{1}$) must be "0." Negation in this manner is sometimes called INVERT or simply NOT. $\overline{A}$ would be a switch which was closed whenever A was open and open whenever A was closed.

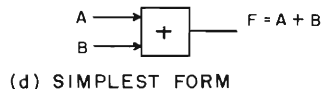
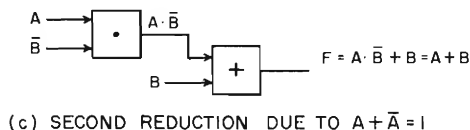
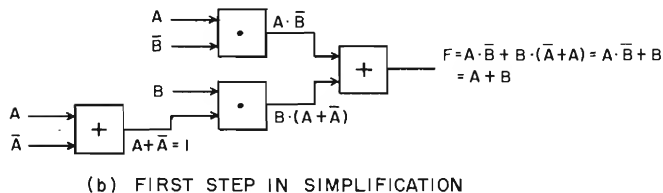
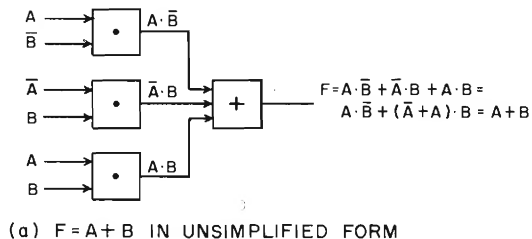
Table 5.1 tabulates some of the more useful rules for this form of algebra. Most of these can be demonstrated with simple switch arrangements or by use of a table of combination or both.

To illustrate the usefulness of the relations given in Table 5.1, refer to Figure 5.2(b). F is "1" whenever we have the combination "A AND *not* B, OR *not* A AND B, OR A AND B." That is, $F = A \cdot \overline{B} + \overline{A} \cdot B + A \cdot B$. To simplify we first use (21) from Table 5.1 to obtain $F = A \cdot \overline{B} + B \cdot (\overline{A} + A)$. By using first (12) and then (16) from the table we arrive at $F = A \cdot \overline{B} + B \cdot 1 = A \cdot \overline{B} + B$. Finally, from application of (23) we obtain $F = A + B$. Figure 5.4 shows the black box arrangement for each of these steps.

(a) F=A+B IN UNSIMPLIFIED FORM

(b) FIRST STEP IN SIMPLIFICATION

(c) SECOND REDUCTION DUE TO A+Ā=1

(d) SIMPLEST FORM

DIFFERENT WAYS OF OBTAINING THE SAME FUNCTION
Figure 5.4

One of the basic problems in digital design is obtaining the minimum number of circuits to synthesize a given function and hence much of the work in this area is devoted to simplification techniques. It is beyond the scope of this book to describe the many simplification methods which have been developed and, therefore, only the Karnaugh Map will be discussed.

The following example is given to illustrate the ideas discussed above as applied to a real problem.

Consider a simplified hot air heating system using oil as a fuel. It is desirable to control the fan for circulating the air and the motor-ignition system for turning on the furnace automatically.

The first condition that must be met is that the furnace is to be turned on when the temperature in the building falls below a certain value. A thermostat remotely located with respect to the furnace can be used to provide a variable T which will have the value 0 when the temperature is too low and the value 1 when the temperature is above that desired.

A second condition is that the fan should not operate until the furnace is warm enough to heat the air. This lower temperature limit can be obtained from a thermostat connected to the furnace itself. Let this variable be designated L and have the value 1 when the temperature of the furnace is sufficiently high, and 0 otherwise.

A third variable might be introduced for preventing overheating of the furnace. Let this variable, H, be 0 as long as the temperature of the furnace is not excessive, and 1 otherwise. Naturally if H is 1 then L must be 1 also.

There are three variables (T, L, and H) involved and two functions, the fan F and the motor-ignition M, which must be controlled. Table 5.2 is a listing of all possible combinations.

VARIABLES			FUNCTIONS		
T	L	H	F	M	
0	0	0	0	1	
0	0	1			NOT POSSIBLE
0	1	0	1	1	
0	1	1	1	0	
1	0	0	0	0	
1	0	1			NOT POSSIBLE
1	1	0	1	0	
1	1	1	1	0	

TRUTH TABLE FOR SIMPLE FURNACE SYSTEM
Table 5.2

Ignoring those combinations which cannot happen (i.e. the furnace at an excessively high temperature, $H = 1$, but not hot enough to turn on the fan, $L = 0$) it can be seen that $M = 1$ when

$$M = \overline{T} \cdot \overline{L} \cdot \overline{H} + \overline{T} \cdot L \cdot \overline{H}.$$

From Table 5.1, relation 21, this expression may be factored to obtain

$$M = \overline{T} \cdot \overline{H} \cdot (L + \overline{L}).$$

Since relation 12 gives $\overline{L} + L = 1$, M may be written as

$$M = \overline{T} \cdot \overline{H} \cdot 1 = \overline{T} \cdot \overline{H}$$

where the last step is obtained by applying relation 16 from Table 5.1.
In a similar manner we may obtain

$$\begin{aligned} F &= \overline{T} \cdot L \cdot \overline{H} + \overline{T} \cdot L \cdot H + T \cdot L \cdot \overline{H} + T \cdot L \cdot H \\ &= \overline{T} \cdot L \cdot (\overline{H} + H) + T \cdot L \cdot (\overline{H} + H) \\ &= \overline{T} \cdot L \cdot 1 + T \cdot L \cdot 1 = \overline{T} \cdot L + T \cdot L \\ &= L \cdot (\overline{T} + T) = L \cdot 1 = L \end{aligned}$$

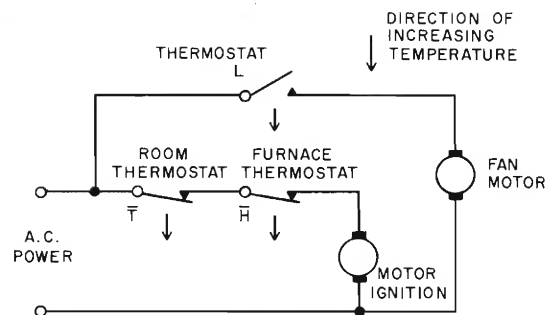
This arrangement of switches is shown in Figure 5.5. Although this example is very simple, it does illustrate the simplification which is possible by the application of a very few rules.

FINAL SIMPLIFIED CONTROL CIRCUITRY FOR BASIC FURNACE

Figure 5.5

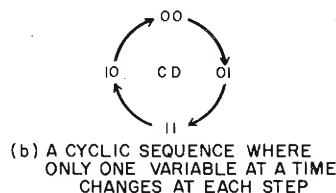
THE KARNAUGH MAP

It is sometimes convenient to arrange the truth table in a somewhat different way. Consider the four-variable table of Figure 5.6(a). Glancing at this table it can be seen that there are four rows where CD = 00 (C = 0 and D = 0), four rows where CD = 10, four rows where CD = 01, and finally four rows where CD = 11. Not quite so obvious is the fact that the same statements could be made about any two variables such as AB, BC, AC, etc.

Now consider a change in switch values. Let us say that CD goes from CD = 00 to CD = 11. This implies that two variables, C and D, must change. A similar case

VARIABLES				
A	B	C	D	F
0	0	0	0	f_0
1	0	0	0	f_1
0	1	0	0	f_2
1	1	0	0	f_3
0	0	1	0	f_4
1	0	1	0	f_5
0	1	1	0	f_6
1	1	1	0	f_7
0	0	0	1	f_8
1	0	0	1	f_9
0	1	0	1	f_{10}
1	1	0	1	f_{11}
0	0	1	1	f_{12}
1	0	1	1	f_{13}
0	1	1	1	f_{14}
1	1	1	1	f_{15}

f_i = 0 OR 1 DEPENDING ON THE VALUE DESIRED FOR F AT THE i th ROW

(a) A FOUR VARIABLE TABLE OF COMBINATIONS

(b) A CYCLIC SEQUENCE WHERE ONLY ONE VARIABLE AT A TIME CHANGES AT EACH STEP

F, CD \ AB	00	01	11	10
00	f_0	f_2	f_3	f_1
01	f_8	f_{10}	f_{11}	f_9
11	f_{12}	f_{14}	f_{15}	f_{13}
10	f_4	x	f_7	f_5

(c) A MAP OF ALL POSSIBLE COMBINATIONS OF ABCD ARRANGED IN CYCLIC ORDER

CONSTRUCTING A KARNAUGH MAP

Figure 5.6

occurs for CD = 10 to CD = 01 where C must go from C = 1 to C = 0 and D must change from D = 0 to D = 1. It is desirable to choose a sequence of combinations where only one variable at a time changes. Such a sequence is CD = 00, 01, 11, 10, 00, 01 . . . . . etc. This is illustrated in Figure 5.6(b). This same sequence is used for both AB and CD in the map shown in Figure 5.6(c). Consider the square marked with an X. This square is in the position AB = 01 and CD = 10 or it corresponds to the combination ABCD = 0110 in the truth table of Figure 5.5(a). Reference to the truth table reveals that F should have the value f_6 for this combination of variables. Hence the value f_6 should be placed in the box indicated by an X. The map, called a Karnaugh map, is thus a somewhat more compact way of writing a truth table.

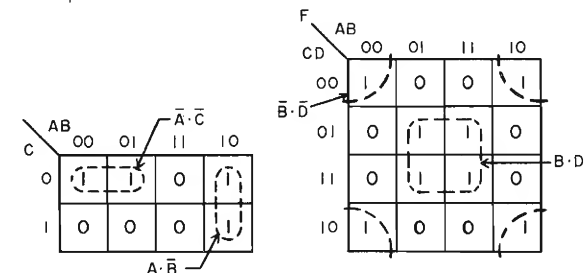
The Karnaugh map is of great value in simplification of switching functions. This comes about because any two adjacent squares differ by only one variable. Consider the three variable map of Figure 5.7(a). Here the values for the f_i have been filled in. F is true when

$$F = \bar{A} \cdot \bar{B} \cdot \bar{C} + \bar{A} \cdot B \cdot \bar{C} + A \cdot \bar{B} \cdot \bar{C} + A \cdot \bar{B} \cdot C$$

Consider the first two terms $\bar{A} \cdot \bar{B} \cdot \bar{C}$ and $\bar{A} \cdot B \cdot \bar{C}$. These terms correspond to the case where AB = 00 and C = 0 for the first term and AB = 01 and C = 0 for the second. The only variable which is different for these two terms is B. AC = 00 for both terms. As a matter of fact, wherever A = 0 and C = 0 on the map, F is 1 and we may replace the first two terms of the expression for F with $\bar{A}\bar{C}$. Similarly the last two terms occur when A = 1 and B = 0 regardless of the value of C and hence they can be replaced with $A\bar{B}$. F becomes

$$F = \bar{A} \cdot \bar{C} + A \cdot \bar{B}$$

C \ AB	00	01	11	10
0	1	1	0	1
1	0	0	0	1

F, CD \ AB	00	01	11	10
00	1	0	0	1
01	0	1	1	0
11	0	1	1	0
10	1	0	0	1

(a) THREE VARIABLE MAP (b) FOUR VARIABLE MAP

SIMPLIFICATION ON KARNAUGH MAPS

Figure 5.7

Of course, the above expression could have been obtained by using the relations in Table 5.1 and juggling the expression for F until it had simplified. It is not always easy to see which of the expressions to use, however, and the map does give a convenient way of visualizing simplifications. It is also interesting to note that the square where AB = 00 and C = 0 and the square where AB = 10 and C = 0 are actually "adjacent" in that B is the only variable that is different in these two positions. Hence we could also write

$$F = \bar{A} \cdot \bar{C} + A \cdot \bar{B} + \bar{B} \cdot \bar{C}$$

The last term, $\bar{B} \cdot \bar{C}$, is however redundant and therefore not necessary since the 1's covered by $\bar{B} \cdot \bar{C}$ are also covered by $\bar{A} \cdot \bar{C} + A \cdot \bar{B}$. The important point is that the map may be pictured as folded to form a cylinder with the first and last columns adjacent at the seam.

In a similar manner, a group of four 1's which are adjacent can be combined. This is indicated in the four variable map shown in Figure 5.6(b). The center group of units are covered by $B \cdot D$ ($B = 1, D = 1$) and the corner units by $\overline{B} \cdot \overline{D}$ ($B = 0, D = 0$) so that

$$F = B \cdot D + \overline{B} \cdot \overline{D}$$

On this four variable map the upper and lower rows are considered adjacent as well as the left and right columns of the map.

NUMBER SYSTEMS

The ordinary, every day number system has the base, or radix, 10. There are ten digits, 0 through 9, which are used to express any quantity desired depending on the order in which they are placed. A decimal number N, such as 2904 is really a contraction for

$$N = (2 \times 10^3) + (9 \times 10^2) + (0 \times 10^1) + (4 \times 10^0)$$

Suppose, however, that instead of the ten digits, 0 through 9, with which we are familiar, only 8 digits, or 5 digits, or 3 digits, or even only 2 digits had been invented. How would counting be established? A possible way of counting is shown in Table 5.3 and in each case the method is identical in nature to that followed in the ordinary decimal system.

COMPARISON OF VARIOUS COUNTING SYSTEMS

Table 5.3

BASE	10	8	5	3	2
NAME	DECIMAL	OCTAL	QUINARY	TERTIARY	BINARY
	0	0	0	0	0
	1	1	1	1	1
	2	2	2	2	10
	3	3	3	10	11
	4	4	4	11	100
	5	5	10	12	101
	6	6	11	20	110
	7	7	12	21	111
	8	10	13	22	1000
	9	11	14	30	1001
	10	12	20	31	1010
	11	13	21	32	1011
	12	14	22	100	1100
	13	15	23	101	1101
	14	16	24	102	1110
	15	17	30	110	1111
	16	20	31	111	10000

Notice that in the decimal system, the least significant digit goes from 0 through 9 and then begins the procedure all over again. A unit before the least significant digit indicates that one cycle of 0 through 9 has been completed. In a similar manner, the least significant digits in the octal system, cycle through digits 0 through 7 and then repeat. A digit before the least significant bit indicates how many cycles have already been used.

Using a subscript to indicate the particular number system being used, we may convert from any number system back to the decimal system. For example

$$(1111)_2 = [(1 \times 2^3) + (1 \times 2^2) + (1 \times 2^1) + (1 \times 2^0)]_{10}$$
$$= [8 + 4 + 2 + 1]_{10} = (15)_{10}$$

or

$$(23)_5 = [(2 \times 5^1) + (3 \times 5^0)]_{10} = [10 + 3]_{10} = (13)_{10}$$

The ordinary procedures of everyday arithmetic, namely: addition, subtraction, multiplication, and division, can be carried out in the same manner as for the common decimal system. Naturally, a new multiplication and addition table must be used for each system. Fortunately, as the number of digits becomes smaller the tables become simpler. Table 5.4 and Table 5.5 contain the addition and multiplication tables, respectively, for the decimal, quinary and binary systems.

COMPARISON OF ADDITION TABLES FOR SEVERAL NUMBER SYSTEMS

Table 5.4

+	0	1	2	3	4	5	6	7	8	9
0	0	1	2	3	4	5	6	7	8	9
1	1	2	3	4	5	6	7	8	9	10
2	2	3	4	5	6	7	8	9	10	11
3	3	4	5	6	7	8	9	10	11	12
4	4	5	6	7	8	9	10	11	12	13
5	5	6	7	8	9	10	11	12	13	14
6	6	7	8	9	10	11	12	13	14	15
7	7	8	9	10	11	12	13	14	15	16
8	8	9	10	11	12	13	14	15	16	17
9	9	10	11	12	13	14	15	16	17	18

(a) DECIMAL ADDITION

+	0	1	2	3	4
0	0	1	2	3	4
1	1	2	3	4	10
2	2	3	4	10	11
3	3	4	10	11	12
4	4	10	11	12	13

(b) QUINARY ADDITION

+	0	1
0	0	1
1	1	10

(c) BINARY ADDITION

COMPARISON OF MULTIPLICATION TABLES FOR SEVERAL NUMBER SYSTEMS

Table 5.5

X	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	0	0	0	0	0	0
1	0	1	2	3	4	5	6	7	8	9
2	0	2	4	6	8	10	12	14	16	18
3	0	3	6	9	12	15	18	21	24	27
4	0	4	8	12	16	20	24	28	32	36
5	0	5	10	15	20	25	30	35	40	45
6	0	6	12	18	24	30	36	42	48	54
7	0	7	14	21	28	35	42	49	56	63
8	0	8	16	24	32	40	48	56	64	72
9	0	9	18	27	36	45	54	63	72	81

(a) DECIMAL MULTIPLICATION

X	0	1	2	3	4
0	0	0	0	0	0
1	0	1	2	3	4
2	0	2	4	11	13
3	0	3	11	14	22
4	0	4	13	22	31

(b) QUINARY MULTIPLICATION

X	0	1
0	0	0
1	0	1

(c) BINARY MULTIPLICATION

It is very obvious that, of all the systems here suggested, the binary system is the simplest. Because there are only two digits, 0 and 1, the multiplication and addition tables are much less complex than for the decimal system. Again, the fact that there are only two digits means that any device with only two distinct states can be used to represent binary numbers. The simplest such device is a mechanical switch which is either in a closed position or an open position. It follows that binary numbers can be represented by very simple devices. A four place binary number such as 1101 can be represented by four switches, three of which are closed and one is open.

ARITHMETIC OPERATIONS

In general, arithmetic operations are carried out just as in ordinary decimal arithmetic. These can best be described by comparative examples. The first two examples are written in considerable detail to clarify the carry and borrow operation while the last two examples assume the carry and borrow is understood.

Addition

	Decimal		Binary
Carry Note	(1)	Carry Note	(1111)
	46		101110
	+28		+ 10110
	74		1000100

Subtraction

	Decimal		Binary
Borrow	(1)	Borrow	(1)
	42		101010
	−18		− 10010
	24		011000

Multiplication

Decimal	Binary
42	101010
21	10101
42	101010
84	000000
882	101010
	000000
	101010
	1101110010

Division

Decimal	Binary
3.75	11.11
16 √60.00	10000 √111100.00
48	10000
120	11100
112	10000
80	11000
80	10000
	10000
	10000

Division obviously can produce answers which are fractional. The binary point need cause no confusion, however, if it is kept in mind that a decimal number 3.75 means

$$(3.75)_{10} = (3 \times 10^{0})_{10} + (7 \times 10^{-1})_{10} + (5 \times 10^{-2})_{10}.$$

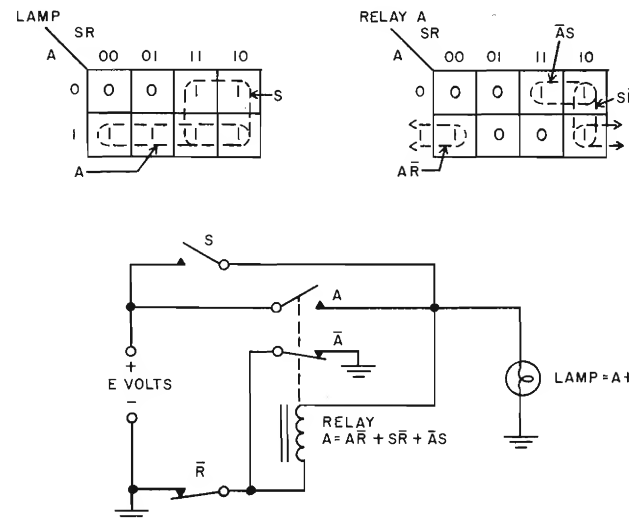
By direct analogy then, a binary number 11.11 means

$$(11.11)_{2} = (1 \times 2^{1})_{10} + (1 \times 2^{0})_{10} + (1 \times 2^{-1}) + (1 \times 2^{-2}).$$

MEMORY ELEMENTS

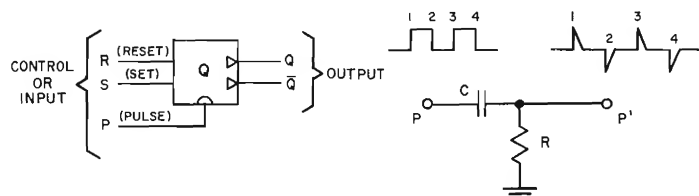
Just as there are many types of switching elements, so there are many types of memory elements which may be used. Briefly, a memory element is an element whose present state depends on what has happened in the past. A simple delay line can be used as a memory element for the output at any given moment depends on what the input was at some previous time. Magnetic materials are frequently used as memory elements as the direction of magnetization at the present moment is determined by the direction of current flow through a coil. This current flow may have occurred quite some time ago and thus the memory is not limited in time as a delay line is. In electronic circuitry, a standard bistable flip-flop with some means of triggering to cause a change of state can be employed as a memory element.

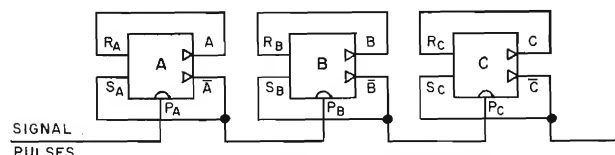
A relay is used as a memory element in Figure 5.8 as this is a very simple and versatile element familiar to almost everyone associated with electronics. Switch S is used to turn on the lamp and switch R is used to turn the lamp off. Whenever S is closed, the lamp will light and relay A will be activated through either a normally closed relay contact ($\overline{A}$) or the normally closed ($\overline{R}$) switch. Of course, once the relay is operated, normally open contact A provides an alternative path for the current which flows through the relay and the lamp. Therefore, even if switch S is released, the lamp will stay lit.

A	S	R	LAMP	RELAY A
0	0	0	0	0
0	0	1	0	0
0	1	0	1	1
0	1	1	1	1
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	1	0

A SIMPLE MEMORY ELEMENT UTILIZING A RELAY
Figure 5.8

Once relay A is operated, the normally closed contact ($\bar{A}$) is open and thus only the normally closed position of R ($\bar{R}$) provides a return path for current. Closing R (or opening $\bar{R}$) removes exitation from relay A, thereby turning off the lamp provided S is off. Thus the relay acts as a memory element for the lamp enabling the circuit to "remember" which switch, S or R, was last operated.

There are many variations of memory element of which the above was chosen because of its extreme simplicity. Practical circuits are discussed in the chapter on digital circuits. This section will discuss very briefly some common applications of memory elements.

Figure 5.9(a) is a symbol frequently used for memory elements. The output line is labelled Q and in some circuits, such as the Eccles-Jordan flip-flop, the complement,

(a) A SIMPLE REPRESENTATION FOR MEMORY ELEMENTS

(b) A SIMPLE TECHNIQUE FOR GENERATING PULSES FROM RECTANGULAR WAVES

(c) MEMORY ELEMENTS INTERCONNECTED TO FORM A SIMPLE BINARY COUNTER

AFTER PULSE	BEFORE PULSE	MEMORY ELEMENTS C	B	A	DECIMAL EQUIVALENT
0	1	0	0	0	0
1	2	0	0	1	1
2	3	0	1	0	2
3	4	0	1	1	3
4	5	1	0	0	4
5	6	1	0	1	5
6	7	1	1	0	6
7	8	1	1	1	7

(d) COMPLETE SEQUENCE FOR THE COUNTER IN TRUTH TABLE FORM

COUNTING WITH BINARY ELEMENTS

Figure 5.9

or "not Q" ($\bar{Q}$), is also available. The P signal is usually a "clock" or chain of uniformly separated pulses which enable the memory element to change state. In effect, the P pulses are ANDed with each of the input lines R and S so that the element can respond to the input lines only at discrete intervals of time coinciding with the presence of a clock pulse.

Sometimes a square wave is used as the clock in which case it is frequently convenient to use an RC differentiating network to cause the flip-flop to respond to either the leading or trailing edge (never both) of the clock signal P. This is also indicated in Figure 5.9(b).

The R line, commonly called a reset, is used to set the memory element to a zero ($Q \rightarrow 0$ when $R = 1$). The S line is used to cause the memory element to assume a "one" state ($Q \rightarrow 1$ when $S = 1$). Due to the internal ANDing of the P line with both R and S, neither input can have an effect until a clock pulse appears. It is also true that it is quite meaningless to make R and S both unity and then apply a clock pulse as this is logically equivalent to asking the Q line to become 0 and 1 simultaneously.

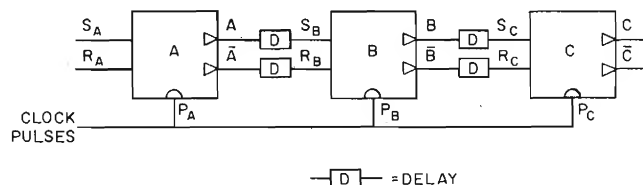
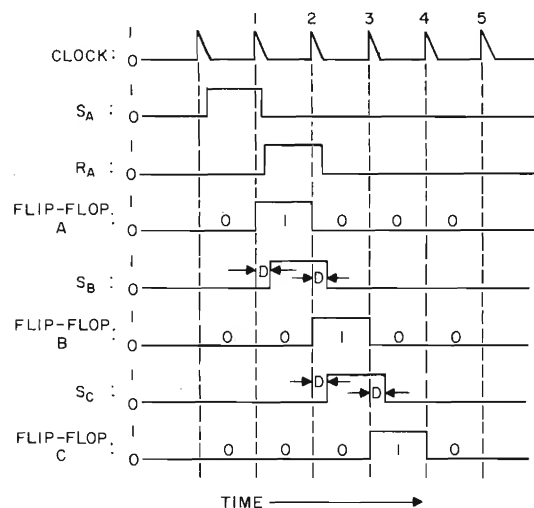
Figure 5.9(c) shows a particular way of connecting three such memory elements. Assuming that the P inputs do use differentiating RC networks and that the elements are sensitive only to positive going pulses on the P lines, then quite obviously whenever $\bar{A}$ changes from 0 to 1, an active pulse will be applied to input P_B on element B and this pulse will cause flip-flop B to go to whatever state is being asked for by the control lines R_B and S_B. The same remark applies to the connection from $\bar{B}$ to P_C.

The outputs of each element are fed back to the inputs. Whenever, for example, the A line is a 1, then the reset line R_A is also a one so that the next pulse at P_A must set $A = 0$. When $\bar{A}$ is a 1, A is 0 and hence the set line S_A would not be energized under this condition. Since A can never be equal to $\bar{A}$, there can never be a case where both R_A and S_A are one (or zero) simultaneously, thus avoiding an illogical possibility.

The manner of interconnection on each of the flip-flops is such that they will change state each time a positive going signal enters a P line. Assume that the elements are all in the zero state ($A = B = C = 0$). The first signal pulse into P_A will cause A to change state so that $A = 1$. This means that $\bar{A}$ must change from $\bar{A} = 1$ to $\bar{A} = 0$. Since this would cause a negative going pulse into P_B, the B element will not be affected and the state of the flip-flops CBA is 001. By following this analysis for a number of pulses, the truth table of Figure 5.9(d) may be obtained. If these combinations are compared with the binary column of Table 5.3, it can be seen that each combination represents a binary number equivalent to the number of signal pulse which have entered P_A. (Recall that zero's to the left of a number are not meaningful). An arrangement such as that in Figure 5.9(c) is frequently referred to as a *counter*. With only three memory elements, such a counter can only count from 0 to 7 and then must repeat itself. By adding more stages, the counter can be used to count as high as desired.

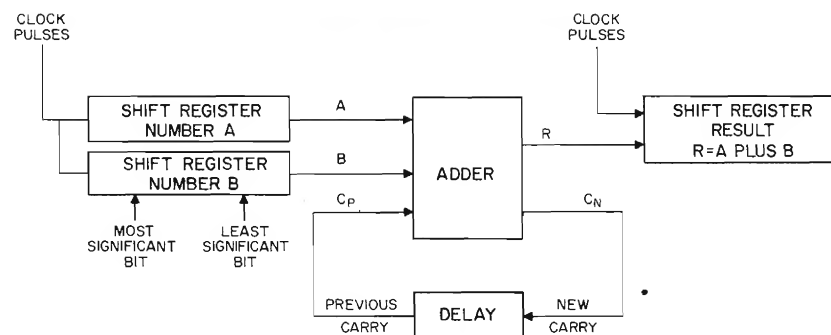
A slightly different arrangement of elements is given in Figure 5.10(a). In addition, to memory elements, small delay units, D, are also used. In many practical cases, there is an inherent delay from the instant a signal is applied to an R or S line to the moment this signal becomes effective (or recognized) inside the memory element. In these cases, the external delay elements may be eliminated. In any event, the total delay time must be less than the interval between clock pulses. The purpose of the delay elements is only to prevent the input lines, R and S, from changing while a clock pulse is actually present. It can be seen that all elements receive the same clock pulse and a possibility for confusion exists if the inputs to B are changing, for example, at the instant P_B is energized.

In order to understand the operation of this arrangement, consider the case where all elements are in the zero state ($A = B = C = 0$), and $S_A = R_A = 0$. Let S_A become 1 just long enough for one clock pulse to enter element A and cause the flip-flop to go to the one state. Thereafter, let S_A return to 0. When S_A returns to zero, let R_A become 1 long enough to catch a clock pulse and thereafter let R_A go to 0 and remain there. This sequence of events is depicted graphically in Figure 5.10(b).

Before the first clock pulse, the setting of the three elements were all zero (ABC = 000). After the first pulse, but before the second pulse, we have ABC = 100. Between the second and third pulse ABC = 010, between the third and fourth ABC = 001, and after the fourth pulse ABC = 000. The effect is that a 1 has been propagated from left-to-right in Figure 5.10(a), advancing one step with each clock pulse. Such an arrangement of memory elements is commonly termed a *shift register.* When the output (in this case C and $\bar{C}$) is tied back to the input (in this example S_A and R_A), the arrangement is termed a *circulating register* or a *ring counter.*

(a) SIMPLE SHIFT REGISTER INTERCONNECTION

(b) TIMING CHART FOR THE SHIFT REGISTER

SHIFT REGISTER
Figure 5.10

CIRCUIT IMPLICATIONS

In order to discuss the areas which have a bearing on the design of circuitry, a problem common to many digital computers will be illustrated. Suppose that it is desirable to design a "black box" which will add two binary numbers together and have as an output the sum of the two numbers. A coarse diagram is given in Figure 5.11 which indicates one possible way in which this task might be performed.

ONE METHOD OF PERFORMING BINARY ADDITION
Figure 5.11

The two numbers, A and B, are each stored in shift registers in the manner indicated so that the least significant *bits* of the numbers will be first into the box labelled Adder. The Adder must do two things. It must produce a bit for the result register and must also determine whether or not a *carry* would result that should be applied to the next set of bits from A and B. The result register is used to accept and store the sum as it is developed by the Adder. It should be kept firmly in mind that only one bit of each number is present at any one time at the input to the Adder.

	PRESENT BINARY VALUE A	PRESENT BINARY VALUE B	PREVIOUS CARRY C_p	NEW CARRY C_N	RESULT VALUE R
0.	0	0	0	0	0
1.	0	0	1	0	1
2.	0	1	0	0	1
3.	0	1	1	1	0
4.	1	0	0	0	1
5.	1	0	1	1	0
6.	1	1	0	1	0
7.	1	1	1	1	1

Table 5.6

Table 5.6 lists all possible combinations of carry and bit values for A and B which can occur at the input of the Adder. In line 3, for example, bit A is a 0, B is a 1, and the previous addition had produced a carry. Since

$$0 + 1 + 1 = (10)_2$$

the result R must be 0 and the new carry should be 1. In line 7, all three bits are 1 and since $1 + 1 + 1 = (11)_2$, the result should be $R = 1$ and $C_N = 1$.
From Table 5.6, it is seen that

$$R = \bar{A} \cdot \bar{B} \cdot C_p + \bar{A} \cdot B \cdot \bar{C}_p + A \cdot \bar{B} \cdot \bar{C}_p + A \cdot B \cdot C_p$$

$$C_N = A \cdot B + A \cdot C_p + B \cdot C_p$$

The complete logic arrangement of the Adder is shown in Figure 5.12. Instead of delaying the carry with a delay line, a memory element in the form of a flip-flop is used to store the new carry. This allows the carry to change with the same clock pulses used to shift the registers thus avoiding the need for a delay and clock with very tight tolerances.

The C_P line of the C flip-flop in Figure 5.12 is attached to four AND gates while the complement line $\bar{C}_P$ is attached to two AND gates. To the circuit designer this means that the flip-flops must be designed so as to be capable of driving these gates without undue loading. If all flip-flops are to be identical (to save on engineering effort) rather than individually designed for each trivial variance in use, then one must also be able to make a shift register with them. In the counter shown in Figure 5.9(c), the flip-flops must be capable of driving the P line as well as an input S line. Although the AND circuits need drive only one input on an OR gate, the OR gate in Figure 5.12 must be capable of driving at least an S line on a flip-flop and an INVERT circuit. It follows that no circuit should be designed to operate only without a load. Every circuit has at least one load and frequently has more than one.

It is customary to consider the current required to drive one input on a logic gate (OR or AND) as a unit load. The maximum current available from any circuit for driving other circuits is divided by the current required by a unit load. The resulting number is the number of logic gates that the circuit can drive and is called the "fan-out" capability of the circuit. In general, the fan-out should be three or greater although special cases may not require this.

A study of Figure 5.12 reveals that the AND gates can be divided in two groups according to the number of inputs. Four of the gates have 3 inputs and three have 2 inputs. One of the OR gates has 4 inputs and the other has 3 inputs. The number of inputs is called the "fan-in" of a circuit. Frequently the circuits are built as 3 input, 5 input, and 9 input gates. If a 4 input AND is needed, for example, a 5 input AND is used with one of its inputs tied to a voltage which represents the 1 level as $A \cdot B \cdot C \cdot D \cdot 1 = A \cdot B \cdot C \cdot D$. Thus the number of different types of circuits which must be manufactured for a given machine is minimized.

Beside fan-in and fan-out considerations, there is one rather subtle point that is not directly apparent from Figure 5.12. Current flow can be either into or out of a circuit. The output of the 3 input OR gate in Figure 5.12, for example, indicates an I_1 which flows into the circuit and an I_2 which flows out of the circuit. A current out of the output of a circuit, I_2, is considered as flowing in a positive direction whereas I_1 is considered as flowing in a negative direction.

In a similar fashion an input may be driven either by "pulling" current out or "pushing" current in as shown by I_4 and I_3 respectively. A current entering the input is considered as a positive flowing current while a current leaving the input is considered as a negative flowing current. Since it is desirable that circuits be capable of driving each other and in particular that any logic circuit be capable of driving another circuit like itself, it is necessary that all currents be positive or that all currents be negative. A set of circuits for which this is true is called a *compatible set.*

A compatible set is called complete if it is possible to generate any arbitrary switching function whatever and includes a general-purpose compatible memory element. The AND, OR, INVERT circuits with the R-S flip-flop of Figure 5.12 form a complete set. Actually, it is possible to eliminate either the AND or the OR gate (but not both) from this set without affecting its completeness. In general, the circuit designer must produce a complete set if his efforts are to be usable.

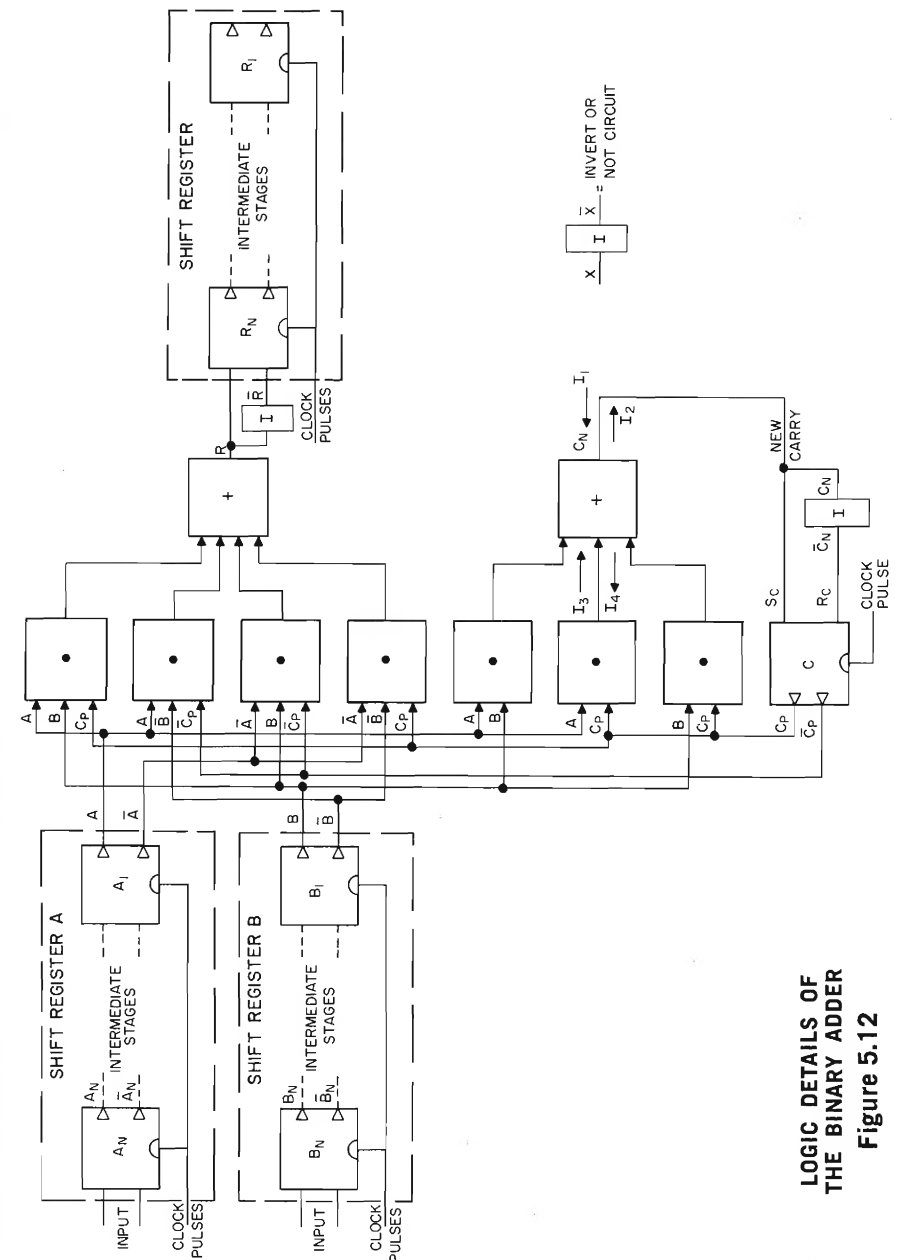



Figure 5.12 LOGIC DETAILS OF THE BINARY ADDER

NOTES

SWITCHING CHARACTERISTICS

CHAPTER 6

Semiconductor transistors and diodes have rapidly become the most useful, versatile, and widely used devices in switching applications. Among the many devices which are used and will continue to be used in this area, only semiconductors have so broad a combination of desirable features. Among these are low power consumption, high speed, small size, no filament power, low cost, good fan-out, and remarkably long life. Any number of devices may have superior qualities in any one area but not in all these areas. A relay, for example, has much greater fan-out capabilities (many relays may be operated by a single relay contact) but is poor in speed, power, and life compared to a transistor. Relays will be life tested many hours for several million operations without failure to qualify as highly reliable while a good transistor switch can make a million or more operations in one second without impairing its useful life. Furthermore, problems of contact bounce and arcing are non-existent with either transistors or diodes.

THE BASIC SWITCH

Any device which has, or can be made to have, two distinct states may be considered for possible application in digital equipment. This property need not always resemble a mechanical switch in being open or closed. For example, a device which can be made to oscillate on one of two distinct frequencies, or a device which operates as an oscillator on a single frequency but which can be made to have one of two distinct phases, or even a device that can be made to oscillate or not oscillate could be used. Frequently switches are made of two components such as a light-emitting diode and a photo-diode where the photo-diode is necessary to detect the presence or absence of a light from the light emitter. In short, there are many ways of producing an analog of the simple mechanical switch.

The most common usage for transistors and diodes is as a direct analog of the mechanical switch. That is, the diode and transistor are made to have a high resistance (open) state and a low resistance (closed) state.

THE BASIC DIODE SWITCH

A diode can be changed from a low resistance state to a high resistance state by the simple expedient of altering the bias conditions across the diode junction. Figure 6.1 gives the voltage-current characteristic for a PN junction and from this it can be seen that a very small voltage in the forward direction can cause an appreciable current flow (low resistance) while a voltage in the reverse direction (but to the right of the avalanche region) will produce only a small leakage current (high resistance).

This figure is somewhat misleading in that it is not drawn to scale. A typical value for leakage current for the 1N3605 at room temperature is 15 nano-amperes at a reverse voltage of 50 volts which corresponds to an "open" circuit resistance of more than 3000 megohms. On the other hand, a forward bias of 0.8 volts will typically produce a current of 80 milliamperes at room temperature which corresponds to 10 ohms for the "closed" circuit resistance. Thus a diode can be a very good switch.

THE BASIC TRANSISTOR SWITCH

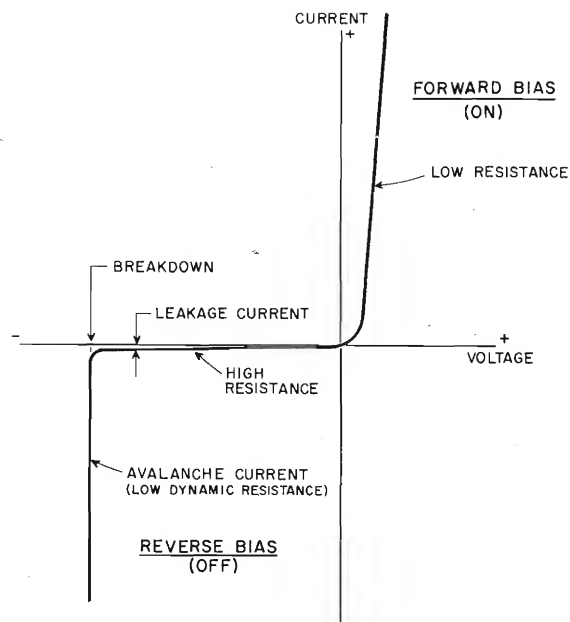
A generalized volt-current characteristic for an NPN transistor is shown in Figure 6.2. That portion of the load line between point A and point B lies in what is commonly referred to as the active-region of the transistor. This region is bounded on the

GENERAL VOLT-CURRENT CHARACTERISTIC OF A DIODE

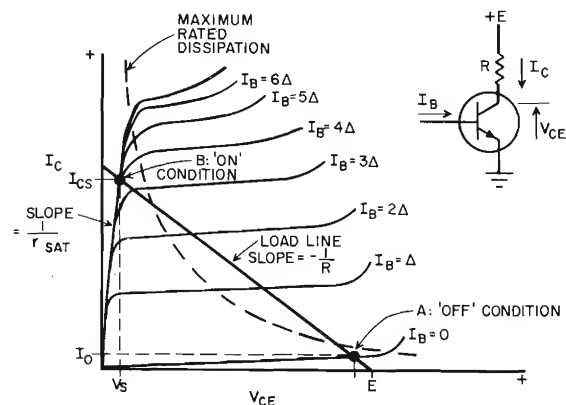
Figure 6.1

GENERALIZED VOLT-CURRENT CHARACTERISTICS FOR AN NPN TRANSISTOR

Figure 6.2

left by the line formed by the superposition of the base current lines with a slope of $1/r_{SAT}$ and on the bottom by the $I_B = 0$ base current line. Thus point A is on one boundary of the active region and point B is on the other.

Point A occurs at a low current, I_o, and a relatively high voltage implying a high resistance or "open" condition. In a properly designed circuit, I_o will approach I_{co}. This current can be extremely small in a modern transistor of the silicon planar type. The 2N914, for example, has a guaranteed maximum of 25 nano-amperes at 20V at room temperature which implies a resistance of about 800 megohms. Typically the value is about four times this or 3200 megohms. Germanium devices, however, have appreciably higher leakage currents. The 2N404, for example, has a guaranteed maximum leakage of 5 micro-amperes at 12 volts at room temperature implying a resistance of only 2.4 megohms. In this one respect silicon is a better choice for a switch. It will be seen, however, that other factors are important also.

Point B occurs at a relatively low voltage and high current point implying low resistance. The ratio of V_s to I_{CS} in Figure 6.2 is often called the saturation resistance. The 2N914, with $I_C = 10\ I_B$, has a typical value of $V_s = 0.35$ volts at $I_C = 200$ ma which is equivalent to about 1.75 ohms for r_{SAT}. Actually r_{SAT} is a somewhat misleading parameter as will be shown.

The high value of "off" resistance and low value of "on" resistance associated with a transistor make the device valuable for switching applications on a par with the diode. The transistor has one very important advantage over the diode in that its state is easily controllable from the base lead. This is because a relatively small current in the base can control a large current in the collector. The diode can only be switched by altering its bias. This switching "gain" makes the transistor a more versatile device. By analogy, a mechanical switch is to a diode what a relay is to a transistor.

STATIC PARAMETERS

The parameters of interest may be separated into static and transient groupings. This is, of course, somewhat arbitrary in that the same parameters may influence both aspects of device behavior, but it is convenient for purposes of discussion.

POWER

Examination of the load line of Figure 6.2 reveals that a considerable portion of the line is in an area where the power dissipation is excessive. This is a common characteristic of many switching circuits. Since the device is operated either "on" (point B) or "off" (point A), the device will not dwell for any appreciable time in the region of excessive power and therefore the average power will not be influenced appreciably at moderate switching rates by this transient excursion into normally forbidden regions. At high switching rates, however, the average power will definitely be influenced by this condition.

Consider Figure 6.3 where a typical waveform has been linearized. It is assumed periodic in form and the transitions are assumed to be ramp functions. The power dissipated in the collector circuit is

$$P = \frac{1}{T}\int_o^T ei\,dt$$

Evaluating this integral we have as a result

$$P = I_S V_S + (\Delta V\, I_S - V_S\, \Delta I)\left(\frac{2\,t_{off} + t_r + t_f}{2T}\right) - \Delta V\, \Delta I\left(\frac{3\,t_{off} + t_r + t_f}{3T}\right)$$

where

$$\Delta V = E - I_o R - V_S$$

$$\Delta I = I_S - I_o$$

$$T = t_f + t_{off} + t_r + t_{on}$$

If $V_S = 0$ and $I_o = 0$ are assumed, then the power dissipated in one cycle is due

only to the transient during switching and not to the power dissipated when fully on or fully off. Under these conditions the power becomes

$$P = \frac{E\,I_S}{6}\left[\frac{t_r + t_f}{T}\right]$$

If the on-time and off-time are reduced to zero, then $T = t_r + t_f$ and this represents a limiting case for a given voltage and current swing. The transistor simply cannot operate at a higher repetition rate than this and still maintain a full swing. Fortunately, most transistors have sufficiently high power handling capabilities that this is not a serious problem for many applications. For example, if $E = 6$ volts and $I_S = 10$ milliamperes, only 10 milliwatts will be dissipated at this ultimate rate.

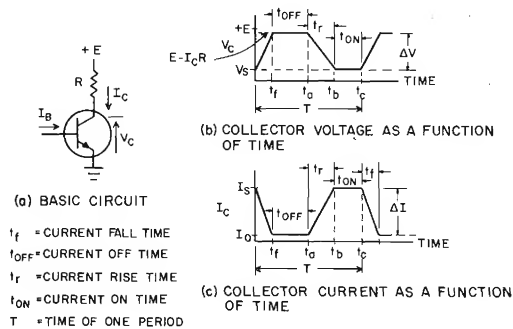
It is interesting to note that the limiting repetition rate is determined only by the rise-time, t_r and fall-time t_f, of the device and circuit itself.

LINEARIZED SWITCH WAVEFORM FOR POWER CALCULATIONS

Figure 6.3

For cases where power is very critical, the dissipation in the base should be added to that of the collector. Normally this is quite small compared to the collector power but, especially in heavily saturating circuitry, this is not necessarily so. The base power is given by

$$P_B = I_B V_B - \left[\Delta V_b I_B + V_B \Delta I_b\right]\left[\frac{2t_{off} + t_r + t_f}{2T}\right] + \Delta V_b \Delta I_b \left[\frac{3t_{off} + t_r + t_f}{3T}\right]$$

where

V_B = base voltage when transistor is on

I_B = base current when transistor is on

ΔV_b = "on" base voltage minus "off" base voltage or the total change in base voltage from on to off

ΔI_b = change in base current from on to off

P_B = power dissipated in the base

and the switching times are the same as for the collector. If the device is actually reverse biased in the off condition, then ΔV_b and ΔI_b will be larger than V_B and I_B. All equations are taken for the NPN configuration.

The limiting factor in transistor (or diode) power dissipation is the temperature of the junction. In a sense, the power dissipated is immaterial as long as the junction temperature does not exceed its maximum rated value. Figure 6.4 is a typical curve of the maximum permissible power as a function of ambient temperature. At room temperature (25°C) the maximum rated power is P. This implies that at a temperature of 25°C and P watts, the junction temperature is at its maximum permissible value.

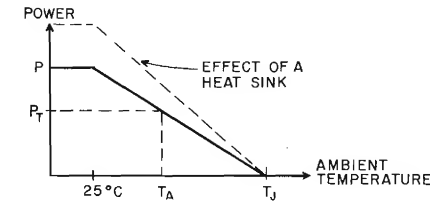
At an ambient temperature T_J, the maximum power that may be dissipated is zero which also implies that the junction temperature is at its maximum permissible value. As a matter of fact, at each point along the sloping portion of the curve the junction temperature is at its maximum value.

TYPICAL POWER DERATING CURVE

Figure 6.4

Two problems arise in practice. In the first case, the power dissipated in the transistor, P_T, is known and it is desired to know the maximum ambient temperature, T_A, which may be permitted. This may be determined graphically as indicated by the dotted lines starting at P_T and T_A in Figure 6.4 or the ratio

$$\frac{P_T}{T_J - T_A} = \frac{P}{T_J - 25}$$

may be used. If the ratio is used, then obviously

$$T_A = T_J - \frac{P_T}{P}(T_J - 25)$$

The second case is the problem of determining the maximum permissible operating power if the maximum ambient temperature is known. Again this may be determined graphically, or using the ratio method we have

$$P_T = P\left[\frac{T_J - T_A}{T_J - 25}\right]$$

The use of a heat sink can increase the power capability of a transistor considerably for ambient temperatures below T_J. It cannot, however, enable operation above that imposed by the junction. The dashed curve in Figure 6.4 shows the effect of a heat sink on the power capability.

It sometimes happens that the manufacturer will specify two power ratings at two different ambient temperatures. Since the shape of the derating curve is known, this is generally sufficient to reconstruct the curve. For example, suppose the two points given are (P_1, T_1) and (P_2, T_2) with $T_2 > T_1$, $P_1 > P_2$. The power along the sloping portion of the curve is given by

$$P = \left(\frac{P_1 T_2 - P_2 T_1}{T_2 - T_1}\right) - \left(\frac{P_1 - P_2}{T_2 - T_1}\right) T$$

The maximum junction temperature occurs when $P = 0$ and hence

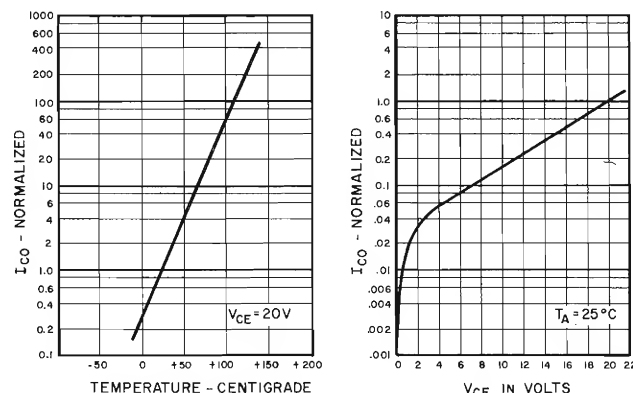
$$T_J = \frac{P_1 T_2 - P_2 T_1}{P_1 - P_2}$$

while the maximum rated power occurs when $T = 25$°C. Hence

$$P_{max} = \left(\frac{P_1 T_2 - P_2 T_1}{T_2 - T_1}\right) - 25\left(\frac{P_1 - P_2}{T_2 - T_1}\right)$$

To reconstruct the graph, power remains at P_{max} for all temperatures below 25°C. From the 25°C point to T_J a straight line is drawn which starts at $(P_{max}, 25)$ and ends at $(0, T_J)$.

LEAKAGE CURRENT, I_{CO}

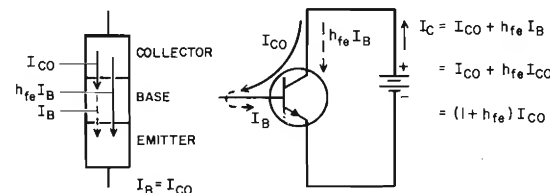
This current, along with the current gain, determines to a large extent the minimum off current, I_O, as indicated in Figure 6.3(c). The physical nature of I_{CO} is discussed elsewhere. In this section only the manner in which it influences the circuit designer will be discussed.

BEHAVIOR OF I_{CO} WITH TEMPERATURE AND VOLTAGE
Figure 6.5

I_{CO} is defined as the dc collector current when the collector junction is reverse biased and the emitter is open-circuited. Its value is determined by the voltage applied and the temperature at which it is measured as is indicated in Figure 6.5. As the curves indicate, I_{CO} essentially varies exponentially with temperature and above the "knee" of the voltage curve tends to follow an exponential variation with voltage.

The use of normalized values for I_{CO} is simply a convenience. For example, at 25°C and 20V the normalized value of I_{CO} is unity. If the specification sheet reads $I_{CO} = 5\ \mu a$ at 25°C and 20 volts then all values along the ordinate should be multiplied by 5 micro-amperes. Thus at 100°C where the normalized value reads 60, the actual value would be 60×5 microamperes or 300 microamperes.

In order to eliminate the need to take voltage variation into account each time a circuit is designed, I_{CO} is almost always specified at a voltage near the maximum rating of the transistor. The circuit designer then assumes I_{CO} constant for voltages less than this value (in some cases this is nearly true). This means that the designer is nearly always conservative; the actual I_{CO} is always less than he has assumed and therefore the design is on the "safe" side. The temperature which determines I_{CO} is the junction temperature of the device, not the ambient. If the basic measuring circuit is studied, however, it is seen that the power dissipated in the transistor is the product of I_{CO} and E. Since I_{CO} is very small the power is very small and the junction temperature is essentially that of the ambient temperature. Many manufacturers label the I_{CO} versus temperature curve with ambient rather than junction temperature.

To the designer of switching circuits, I_{CO} is important in that it determines how close he may approach to a true open circuit condition. As has been shown, this current can be very small indeed. Unfortunately, another phenomena enters into this consideration. Consider the circuit of Figure 6.6 in which the base lead is open rather

than the emitter. Leakage current I_{CO} flows across the reverse biased collector-to-base diode junction as before. Now, however, this current cannot return to the battery source unless it flows across the base-to-emitter diode junction. Since polarities are such that this junction tends to be forward biased, this leakage current is essentially indistinguishable from a base current supplied externally. The transistor therefore amplifies this current to produce an additional current, $h_{fe}\ I_{CO}$, in the collector. The net result is that a total collector current of $(1 + h_{fe})\ I_{CO}$ appears.

EFFECT OF TRANSISTOR GAIN ON LEAKAGE CURRENT
Figure 6.6

If a finite resistance is placed between the base and the emitter, some of the I_{CO} current can be shunted through this resistor. This shunted portion of the leakage current would not be amplified and therefore a collector current, I_O, will flow such that $I_{CO} \leq I_O \leq (1 + h_{fe})\ I_{CO}$. This is the I_O shown in Figure 6.3 and used in the power calculations.

By reverse-biasing the base to emitter by approximately 0.2 volts, I_O can be made to approach I_{CO} quite closely for germanium transistors. Because of the higher thresholding effect of silicon, I_O approaches I_{CO} quite closely at zero bias. It is not always desirable, however, to return the base to zero bias in some circuits and frequently I_O is specified for some specific forward bias on silicon units. Thus the 2N914 is specified for a maximum current of 10 microamperes at a collector-to-emitter voltage of 20V, an ambient temperature of 25°C and a forward bias of 0.25 volts. I_O under these conditions is only 25 nanoamperes maximum. Because germanium has such low base-emitter voltages and because leakage current is very much greater than in silicon, it is not very practical to apply this type of specification to germanium transistors.

If the base to emitter of a transistor is reverse biased, there will be a leakage current, I_{EBO}, similar in every way to I_{CO} except that it flows from emitter to base. Thus to reverse bias a transistor, it is necessary to allow for I_{CO} and I_{EBO} to flow out of the base lead. When I_{EBO} is not specified it is usually assumed to be equal to I_{CO}.

CURRENT GAIN, h_{FE}

The current gain of greatest interest to the designer of switching circuits is the direct-current gain. This is defined as

$$h_{FE} = \frac{I_C}{I_B}$$

where I_B and I_C is the absolute value of the base current and collector current respectively. The more commonly used parameter, h_{fe}, is essentially the ratio of a change in collector current for a small change in base current.

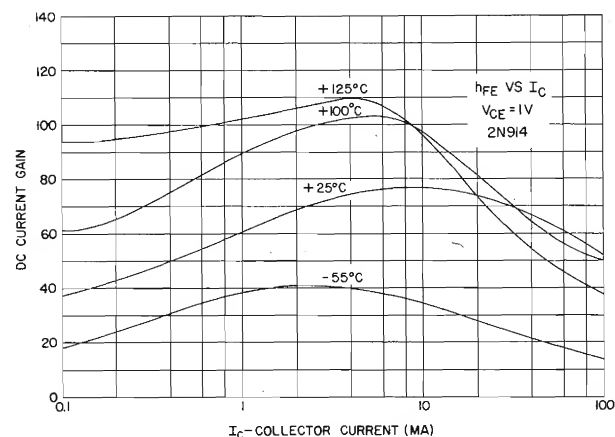
The value of h_{FE} is usually measured at a voltage between collector and emitter which is rather close to the saturation voltage as this represents a minimum value. Speaking loosely, h_{FE} is not a very strong function of collector-emitter voltage outside of saturation. It is, however, a rather strong function of junction temperature and of

VARIATION OF h_{FE} WITH TEMPERATURE AND CURRENT

Figure 6.7

collector current. Figure 6.7 is a set of typical curves for h_{FE} as a function of I_C for the 2N914. Each curve is associated with a different temperature.

The most important feature is that over most of the current range, the gain decreases with decreasing temperature. Obviously, this rule cannot be applied indiscriminately. The reverse begins to be true beyond 10 milliamperes and 100°C. A second feature of interest is that the gain has a definite maximum which may be quite broad (at room temperature for example) or rather sharp (at 125°C). The collector current at which this maximum occurs is a function of the junction temperature. It follows that the selection of operating (on) current to be used should take into consideration the temperature range over which the circuit will be expected to operate.

It sometimes happens that a decreasing gain with increasing temperature is desirable. Magnetic cores, for example, often require less drive at high temperatures than at low. Generally, however, this characteristic cannot be controlled sufficiently well to be useful.

h_{FE} should not be confused with *forced* current gain. Consider Figure 6.2. When $I_C = E/R$, $V_{CE} = 0$ and therefore all collector bias is removed from the transistor. Actually this cannot quite happen. As shown by point B, further transistor action ceases at a voltage V_s (which is quite small). Hence the collector current is actually limited to $I_{CS} = (E - V_s)/R$. It is, however, quite possible to force more base current than necessary for $I_C = I_{CS}$. This, of course, cannot change I_C appreciably. The ratio of I_{CS} to I_B when $I_B > I_{CS}/h_{FE}$ is called the forced current gain and it is always less than the natural gain h_{FE}. The forced current gain is sometimes referred to simply as the *circuit current ratio.*

COLLECTOR SATURATION VOLTAGE, $V_{CE\,(SAT)}$

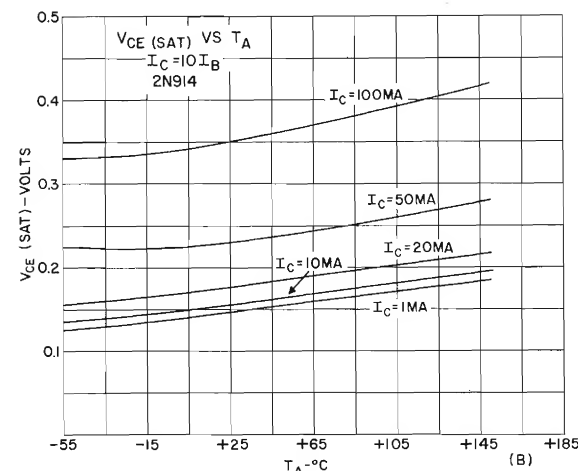
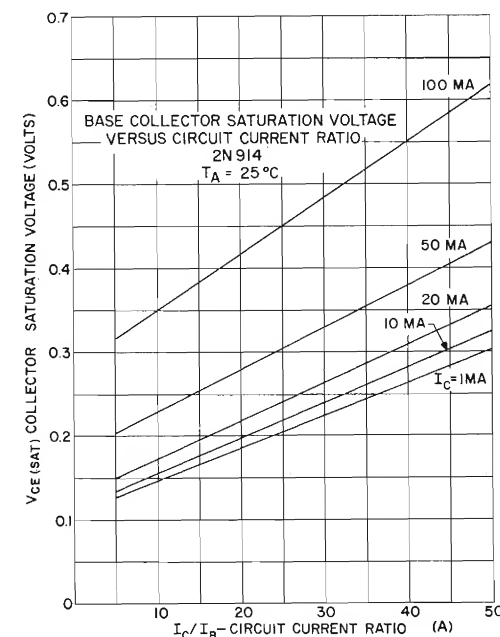
The collector saturation voltage, $V_{CE\,(SAT)}$, which has been abbreviated to V_s in Figure 6.2 and in the equations for power, is the parameter that effectively limits how closely the transistor may approximate a closed switch. Figure 6.8 contains two curves which show how this parameter varies with the circuit current ratio, collector current, and temperature.

VARIATIONS IN $V_{CE\,(SAT)}$ WITH TEMPERATURE, COLLECTOR CURRENT, AND FORCED GAIN

Figure 6.8

In the first set of curves the temperature is held constant while the circuit current ratio is increased (or I_B decreased) and the saturation voltage changes linearly. The fact that the saturation voltage changes with the circuit current ratio makes the concept of $r_{(SAT)}$ as the reciprocal of the slope of the characteristic curve below V_s in Figure 6.2

rather awkward. This is probably the reason $r_{(SAT)}$ has never been widely accepted. The two curves of Figure 6.8 represent the best method yet devised to describe saturation voltage over a wide range of operating conditions.

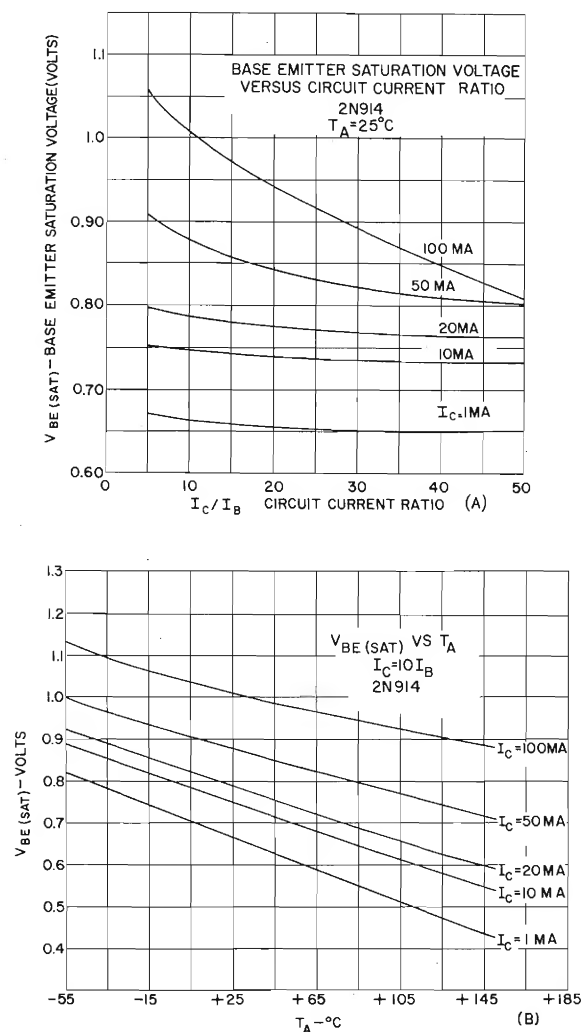
The second of the two sets of curves indicate that temperature is not a particularly strong influence and that the saturation voltage increases with increasing temperature. This depends very much on the device being used. In some devices the saturation voltage is almost completely independent of temperature while in others the temperature coefficient can be negative over all or part of the temperature range.

VARIATIONS IN $V_{BE\,(SAT)}$ WITH OPERATING CONDITIONS

Figure 6.9

BASE-EMITTER SATURATION VOLTAGE, $V_{BE\,(SAT)}$

A set of curves similar to the curves for collector saturation are shown in Figure 6.9 for the 2N914. The most characteristic feature is that the slopes of these curves are opposite to those shown in Figure 6.8. The temperature coefficient is negative and varies little over the entire range. A common rule of thumb is to allow 2 millivolts change per degree centigrade in the base-emitter voltage. This rule is surprisingly good, even for germanium at moderate current levels. At higher current levels this value tends to be too large.

TRANSIENT RESPONSE CHARACTERISTICS

The factors which influence the transient response of the transistor are basically associated with the diffusion time of the carriers across the base region, the effect of capacitances due to the collector-base and base-emitter junctions, the associated parasitic capacitances between leads and from case to leads and, just as important, the operating conditions of the circuit. In predicting transient response it is convenient to think of the turn-on delay time, t_d, the current rise time, t_r, the storage or turn-off delay time, t_s, and the current fall time, t_f, as dependent variables whose value depends upon the operating conditions of the device as well as the capacitances and diffusion parameters. These latter are also affected by the operating conditions of the circuit. It follows that the calculations of the time intervals (t_d, t_r, t_s, and t_f) can be very complex.

DEFINITION OF TIME INTERVALS AND CURRENTS

The time intervals are defined in Figure 6.10. This set of definitions has become almost universally accepted for measurements and therefore requires no further explanation beyond pointing out that the 10% and 90% points of the collector waveform are taken as the points at which measurements are to be made. The collector waveform is, of course, the voltage from collector to emitter. For most calculations we shall use collector current rather than collector voltage as the reference thereby avoiding some difficulty with what is meant by rise-time, t_r. In Figure 6.10(c), the voltage is *falling* during t_r but, of course, this is due to the fact that the current is increasing (or *rising*) during this interval.

TURN-ON DELAY, t_d

Consider the circuit of Figure 6.10(a) with the switch in its open position. Under static conditions there exists only a −10V source connected to the base, B, through the 100 ohm resistor in series with R_B. Thus the base must be reverse biased at −10V, plus a very slight voltage drop due to leakage currents, and the transistor is off. The collector, C, must, therefore, be at +10V minus a very small voltage due to collector leakage, I_O, and the total voltage between collector and base is +20 volts. Any capacitance between base and collector is, therefore, charged to 20 volts, and any capacitance between base and emitter must be charged to 10 volts as shown in Figure 6.11(a). Since the transistor is off, it is effectively not in the circuit.

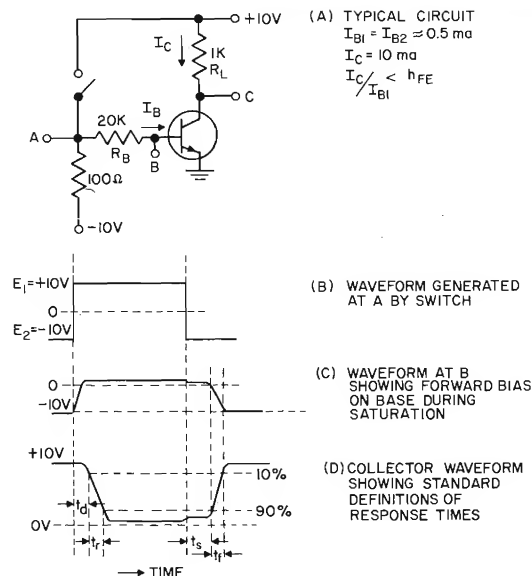
At the instant of switch closure, the voltage at the base cannot change immediately because of the capacitances associated with the base. This means that effectively 20 volts has been placed across R_B thus making I_B = 1 ma as indicated in Figure 6.11(b). Until the base-emitter voltage vanishes, there is no way the transistor can turn-on. As current continues to flow, the transistor base-to-emitter becomes forward biased and the transistor begins to turn-on. This occurs when V_{BE} approaches about +0.1 volt for germanium and +0.5 volts for silicon. Beyond this point the base-emitter diode acts as a clamp so that the voltage cannot continue to rise at the base. Since 0.5 volts is very small compared to 10 volts, the final base-current will be about 0.5

TRANSIENT RESPONSE

Figure 6.10

ma as indicated in Figure 6.11(c).

The time required to reach the threshold of transistor turn-on may be calculated, assuming C_E and C_C are simple capacitances whose value is known. This time interval is not t_d since the collector current has not reached its ten percent point at this time. Calling this time interval t_d' and realizing that t_d is the sum of t_d' plus a small portion of the rise time, Δt_r, we have, for this particular circuit

$$t_d = t_d' + \Delta t_r$$

Due to the fact that the circuit of Figure 6.11 gives rise to two time constants, it is not a simple matter to solve explicitly for t_d'. For this reason it is customary to make some reasonable approximation for t_d'. The change in voltage at the base is $\Delta V_b = 10V$. Assuming that the collector voltage does not change, the change in charge, Q_{CD}, on C_C is $Q_{CD} = C_C \Delta V_b$ and the change in charge on Q_E is $C_E \Delta V_b$. The total charge which has flowed into both capacitors is thus $(C_C + C_E) \Delta V_b$. Since this occurred in a time t_d', then the average current must have been

$$I_{B(avg.)} = (C_C + C_E)\frac{\Delta V_b}{t_d'}$$

The average current is very nearly given by the arithmetic mean of the initial current and final current.

$$I_{B(avg.)} \cong \frac{[I_B(o) + I_B(t_d')]}{2}$$

This gives 0.75 ma for $I_{B(avg.)}$ although in this example the true value would be closer to 0.7 ma. Using this value (0.75 ma) for $I_{B(avg.)}$ we have

$$t_d' \cong (C_C + C_E)\left[\frac{\Delta V_b}{I_{B(avg.)}}\right] = 13.3\,(C_C + C_E) \times 10^3$$

If 0.7 ma (obtained by assuming an exponential decay from 1 to 0.5 ma and averaging) had been used, t_d' would have been $14.3\,(C_C + C_E) \times 10^3$ and the error would be about seven percent.

(a) STEADY-STATE 'OFF' CONDITION WITH ALL CURRENTS DECAYED TO ZERO.

(b) CURRENT FLOW AT THE INSTANT OF SWITCH CLOSURE.

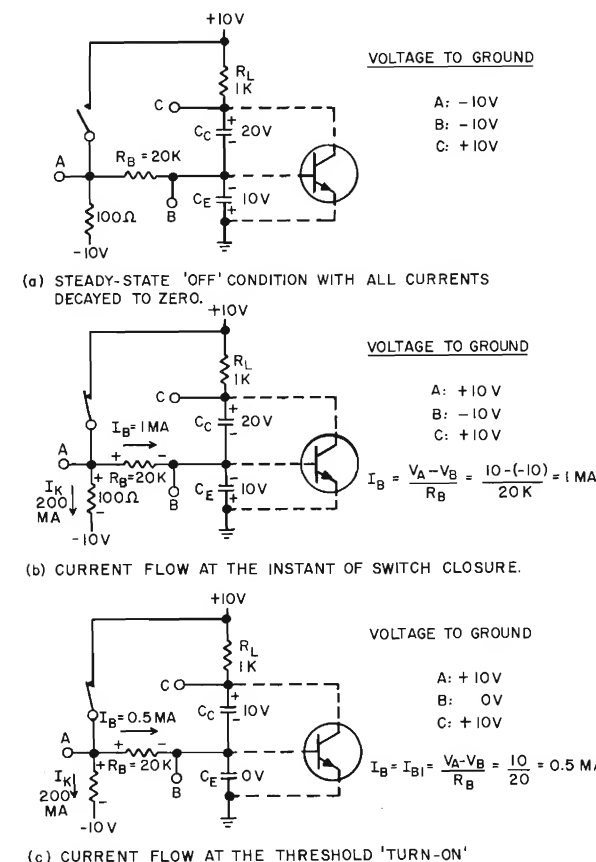
(c) CURRENT FLOW AT THE THRESHOLD 'TURN-ON'

PHYSICAL REASONS FOR t_d

Figure 6.11

COLLECTOR AND EMITTER TRANSITION CAPACITANCES

Although these calculations are quite simple and give reasonably good results, there is a significant drawback inherent in this method. This has to do with the nature of the capacitances involved. Consider Figure 6.12 where the capacitances C_C and C_E are depicted as functions of voltage. A swing of ten volts, for example, causes C_C to change from approximately 4 picofarads at 10 volts to 6 picofarads at 0.1 volts. It is thus rather difficult to state precisely what value of C_C to use in calculating t_d'.

It is frequently mentioned in the literature that C_C is a function of voltage. If this function is known, then the total change in charge on the capacitor for a change in voltage from V_1 to V_2 is

$$\Delta Q_{CD} = \int_{V_1}^{V_2} C_C(V)\, dV$$

This value for the change in charge for a change in voltage $V_2 - V_1 = \Delta V$ may then be used to calculate an equivalent linear capacitance, $\bar{C}_C$. Thus

$$\bar{C}_C = \frac{\Delta Q_{CD}}{\Delta V} = C_{CD}$$

and this value may then be used. Unfortunately, this evaluation requires a knowledge of the proper analytical expression for C_C as a function of V_C.

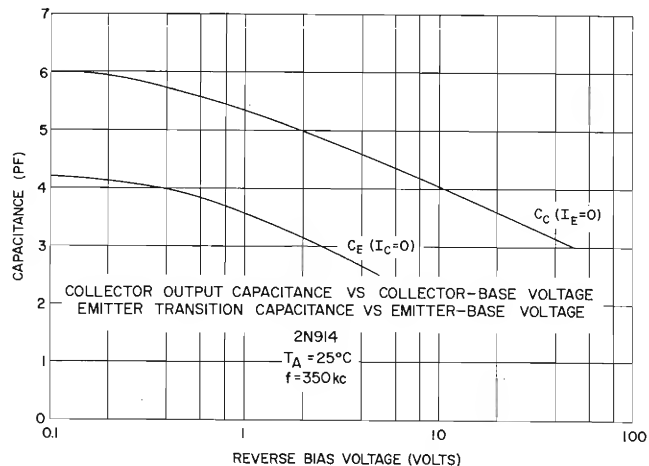



Figure 6.12

It is generally easier and simpler to use the graph of Figure 6.12 directly. Initially V_{CB} was at 20V as indicated in Figure 6.11. Using the graph of Figure 6.12, it can be seen that C_C is about 3.6 picofarads at this voltage. This implies that the charge, $Q_C = C_C V_{CB}$ is 72 picocoulombs. At the edge of turn-on, V_{CB} is 10 volts (Figure 6.11(c)) and C_C is 4 picofarads (Figure 6.12) giving $Q_C = 40$ picocoulombs. Since $\Delta Q_C = Q_{CD} = 72 - 40 = 32$ picocoulombs, we have

$$C_{CD} = \bar{C}_C = \frac{\Delta Q_C}{\Delta V} = \frac{32}{10} = 3.2 \text{ picofarads}$$

and the effective linear capacitance is actually less than the capacitance at each point. Using the minimum capacitance (at 20V) in this case would be somewhat conservative.

The same process may be used for C_E except that in this case the voltage across C_E is reduced to zero (or even slightly reversed) as indicated in Figure 6.11(c). Thus the total charge to be removed is determined only by the charge at the 10 volt point. The net result is that the time interval, t_d', is modified as

$$t_d' = (\bar{C}_C + \bar{C}_E)\frac{\Delta V_b}{I_{B\,(avg.)}} = (C_{CD} + \bar{C}_E)\frac{\Delta V_b}{I_{B\,(avg.)}}$$

Supposing that C_E is 2 picofarads at 10 volts for some particular transistor (not a 2N914), then ΔQ_E will be 20 picocoulombs for a 10-volt change from 10 volts to zero volts. Hence the effective capacity, $\bar{C}_E$, is 2 pf. Using the previous estimate $t_d' = 14.3\,(\bar{C}_C + \bar{C}_E) \times 10^3$ we have $t_d' = 14.3\,(5.2) \times 10^{-9} = 74.4$ nanoseconds.

FORWARD BASE CURRENT, I_{B1}

When the circuit of Figure 6.10(a) reaches the edge of transistor turn-on, as indicated in Figure 6.11(c), the base-emitter diode acts as a clamp to hold the base voltage near ground. Under these conditions the value of I_B remains constant throughout the rise time and "on" time of the device. This constant current is denoted as I_{B1} and in applications where I_B is not constant it is usually understood that I_{B1} is some sort of average or effective value in the formulas. It is frequently referred to as the *forward base current.*

GAIN BANDWIDTH PRODUCT

The common base current gain, generally denoted as α, is a function of frequency. One of the better approximations, obtained by solving the diffusion equation (with some simplifying assumptions regarding boundary conditions) is

$$\alpha = \text{Sech}\left[a\sqrt{1 + j\omega T}\right]$$

where a = W/L << 1, W= base width, L = diffusion length of carriers in the base, and T is the carrier life time. Such a formula is rather awkward to use and an approximation occasionally suggested is

$$\alpha = \frac{\alpha_o \epsilon^{-jk(\omega/\omega_\alpha)}}{1 + j\frac{\omega}{\omega_\alpha}}$$

where α_o is the low frequency gain, ω_α is the 'alpha cutoff' frequency in radians per second and determined as that frequency where the magnitude of α is —3 db, or 0.707, of its low frequency value, and k is an empirically determined constant (about 0.2 - 0.4) for a particular device. Even this formula, however, is somewhat awkward to use and thus the most common approximation is simply

$$\alpha = \frac{\alpha_o}{1 + j\frac{\omega}{\omega_\alpha}}$$

This final approximation has the same magnitude at all frequencies as the previous estimate but the predicted phase can be in considerable error.

As ω/ω_α becomes large compared to 1, the magnitude of α becomes $|\alpha| \cong \alpha_o(\omega_\alpha/\omega)$, or, rearranging, we have

$$\omega\,|\alpha| \cong \alpha_o\,\omega_\alpha = \omega_T = 2\pi f_T$$

That is, the product of the frequency ω and the magnitude of the gain at this frequency is approximately equal to the product of the low frequency gain and the alpha cutoff frequency, both of which are constants of the device. The product is termed the *gain-bandwidth product* and may be given in terms of radians/second (ω_T) or cycles/second (f_T) and is widely used as a figure-of-merit for transistors.

The small-signal common-emitter gain, β, is defined as

$$\beta = \frac{\alpha}{(1 - \alpha)} = \frac{\beta_o}{1 + j\beta_o\left(\frac{\omega}{\omega_T}\right)}$$

where $\beta_o = \alpha_o/(1 - \alpha_o)$. The frequency at which the magnitude of β is —3 db down (or 0.707 of) from β_o occurs when $\omega = \omega_T/\beta_o$ and is usually referred to as the "beta cutoff frequency." It can be seen that the beta cutoff frequency is considerably lower than the alpha cutoff frequency. As ω becomes larger than ω_T/β_o, the magnitude of β rapidly approaches

$$|\beta| \cong \beta_o\left(\frac{\omega_T}{\beta_o\,\omega}\right) = \frac{\omega_T}{\omega}$$

or

$$\omega\,|\beta| \cong \omega_T$$

Thus the gain-bandwidth product is the same in the common-emitter configuration as it is in the common-base configuration.

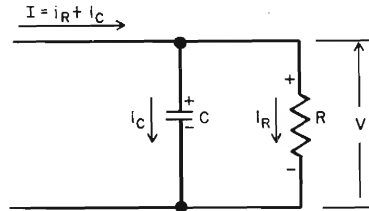
For switching applications it is usually assumed that β is approximately h_{FE}. This is due to the fact that β (as a small-signal parameter) changes at different operating points and h_{FE} is a sort of *average* value over the entire switching range. Thus the frequency dependent relation for I_B and I_C becomes

$$I_C = \frac{h_{FE}\, I_B}{1 + j\, h_{FE} \frac{\omega}{\omega_T}}$$

or, rewriting,

$$j\, \omega\, I_C + \frac{\omega_T}{h_{FE}}\, I_C = \omega_T\, I_B$$

Examining this last statement, it can be seen that this corresponds to the sinusoidal solution of the differential equation

$$\frac{d}{dt}(i_c) + \frac{\omega_T}{h_{FE}}(i_c) = \omega_T\, i_b$$

$v = i_R R \qquad i_R = \frac{V}{R} = \frac{CV}{CR} = \frac{q}{T}$

$q = CV \qquad \mathcal{T} = RC \qquad I = \text{CONSTANT}$

$i_C = C\frac{dv}{dt} = C\frac{d}{dt}(i_R R) = \mathcal{T}\frac{di_R}{dt} = \frac{d}{dt}(CV) = \frac{dq}{dt}$

(a) BASIC CIRCUIT AND FUNDAMENTAL RELATIONS

	DIFFERENTIAL	SOLUTION
CURRENT:	$I = \mathcal{T}\frac{di_R}{dt} + i_R$	$i_R = I(1 - \epsilon^{-t/\mathcal{T}})$
VOLTAGE:	$I = C\frac{dv}{dt} + \frac{V}{R}$	$v = IR(1 - \epsilon^{-t/\mathcal{T}})$
CHARGE:	$I = \frac{dq}{dt} + \frac{q}{\mathcal{T}}$	$q = I\mathcal{T}(1 - \epsilon^{-t/\mathcal{T}})$

(b) TIME SOLUTION FOR BASIC CONCEPTS OF CHARGE, VOLTAGE, AND CURRENT

DEVELOPMENT OF EQUIVALENT CONCEPTS

Figure 6.13

The solution for i_c, if $i_b = I_{B1}$ (a constant), is very simply

$$i_c = h_{FE}\, I_{B1}\left(1 - \epsilon^{\frac{-\omega_T t}{h_{FE}}}\right)$$

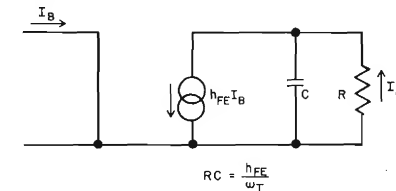
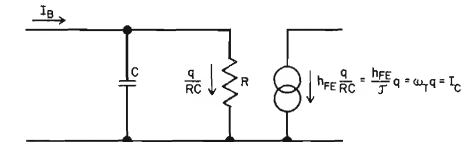
which is a well known form given by simple RC circuits. Indeed, if the very simple circuit of Figure 6.13 is considered, we have several possible forms for expressing the basic differential equation. Provided

$$\tau = \frac{h_{FE}}{\omega_T}$$

$$I = h_{FE}\, I_{B1} = I_C$$

the circuit of Figure 6.13 exactly represents the equivalent circuit for the *approximate* transistor relation

$$I_C = \frac{h_{FE}\, I_B}{1 + j\, h_{FE} \frac{\omega}{\omega_T}}$$

$RC = \frac{h_{FE}}{\omega_T}$

(a) SIMPLE EQUIVALENT CIRCUIT WITH CHARGE IN COLLECTOR

(b) SIMPLE EQUIVALENT CIRCUIT WITH CHARGE REFERRED TO BASE

SIMPLE EQUIVALENT CIRCUIT WITH CHARGE REFERRED TO BASE

Figure 6.14

If a circuit is desired which will distinguish I_B and h_{FE} this can be done by using a current generator as shown in Figure 6.14.

The current solution of Figure 6.13 indicates that i_R is directly equivalent to the collector current, I_C. The voltage and the charge are related to the collector current by constants. Thus

$$V = I_C\, R \text{ or } I_C = \frac{V}{R}$$

$$Q = I_C\, \tau \text{ or } I_C = \frac{Q}{\tau}$$

It is immaterial at this point from what viewpoint (current, voltage, or charge) the device is viewed, as the viewpoints can be shown to be equivalent. Thus the transistor may be considered as: a current-controlled device, in which the current in

the base controls the collector current; a voltage-controlled device in which the junction voltages are considered the controlling factors; or a charge-controlled device in which the charge within the transistor controls the device (and base current is needed only to replenish *charge* which has 'leaked' away) — just as one may consider the simple circuit of Figure 6.13 as having i_R controlled by the input current I, or controlled by the voltage across the capacitor, or controlled by the charge in the capacitor. As developed, however, the charge concept appears to offer some slight advantage in reducing the number of required parameters needed to describe switching behavior, as well as providing a mental concept of the device which can aid intuition.

CHARGE CONTROL CONCEPTS

The emitter and collector junctions of a transistor when in the cutoff condition are reversed biased; in this condition only leakage currents flow across the junctions, the base charge is negligible, and the junction depletion layers are wide because of the reverse bias applied as shown in Figure 6.15(a). In Figure 6.10 (a), this condition exists in the transistor when the switch is open; V_{BE} is equal to −10 volts and V_{CB} is equal to 20 volts. Immediately after the switch is closed, no collector current flows since the emitter junction is reverse biased, thus the initial base current which flows supplies charge to the emitter and collector junction depletion layers and soon causes the emitter junction to become forward biased and begin emitting as shown in Figure 6.15(b). The quantity of charge which has been supplied to the emitter junction depletion region is called Q_E and is a function of the reverse bias voltage which was applied to the junction prior to the application of the turn-on signal. The charge supplied to the collector depletion region during this time is denoted Q_{CD} and is a function of the reverse bias on the emitter, and the collector supply voltage being switched. Looking again at Figure 6.10(a), the condition illustrated in Figure 6.15(b) exists when V_{BE} equals about 0.3 volts and V_{CB} equals about 10 volts.

With the emitter junction now forward biased, the transistor enters the active region. Collector current begins to flow and the voltage at the collector begins to drop because of the presence of the collector load resistor, R_L, shown in Figure 6.10(a). During this time a gradient of charge is established in the base region of the transistor. The slope of this charge gradient is proportional to the collector current which is flowing. If the base current supplied is greater than the rate of recombination of charge in the base region, the gradient will continue to rise until an equilibrium condition is reached. If equilibrium is reached before the collector junction is forward biased, the transistor will not saturate. Since the recombination rate of charge in the base is I_C/h_{FE} (or I_{B1}), the collector current will rise to $h_{FE}\ I_{B1}$ if the device does not saturate. If, on the other hand, the collector current causes the collector-base junction to become forward biased before equilibrium is reached, the device will saturate. The existing condition within the transistor at the edge of saturation is depicted in Figure 6.15(c). The time required to move from the edge of cutoff to the edge of saturation is the rise time. Charge quantities involved are the base gradient of charge Q_B, which is a function of collector current flowing, and Q_C, which is a function of V_{CB}. Q_C is the charge required to cause the collector junction to narrow and becomes forward biased. Since measurement of Q_B and Q_C is frequently accomplished by measuring the two quantities together and then separating them as shown in Chapter 18, the sum of Q_B and Q_C is frequently used and is called $Q_B{}^*$. At the edge of saturation the V_{BE} is about 0.3 volt and V_{CB} is 0 volts if the bulk resistance of the collector body is neglected. Since equilibrium is not established with respect to the base current, charge in excess of that required to saturate the transistor is introduced into the base region. The base gradient of charge remains constant since the collector current is at a maximum for the circuit; the excess charge, Q_{BX}, is a function of the current which is

permitted to flow into the base in excess of that required to saturate the transistor. This current is called I_{BX}. Distribution of Q_{BX} in the transistor is shown in Figure 6.15(d).

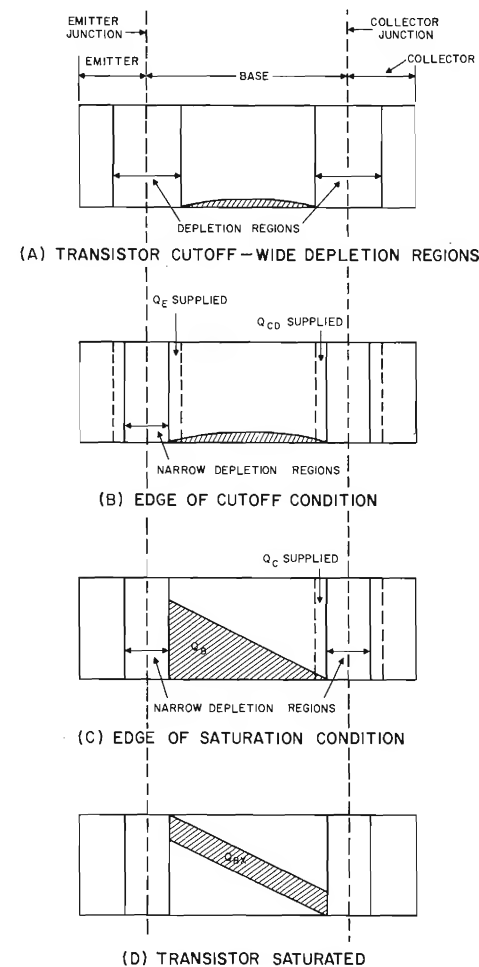
In the alloy type transistor, essentially all of the stored charge is in the base region. In devices where the collector bulk region has high minority carrier lifetime, excess carriers can also be stored in the collector. These carriers reach the collector from the base since the collector junction is now forward biased and base majority carriers are free to flow into the collector region during saturation. These stored carriers have no effect during turn-on time. Storage time, however, is the time required to remove these stored carriers as well as those stored in the base. Both the mesa and planar devices

CHARGE DISTRIBUTION IN TRANSISTOR DURING SWITCHING
Figure 6.15

exhibit collector minority carrier storage. The epitaxial process used in General Electric transistors 2N781, 2N914, 2N994 and the 2N2193 minimizes collector storage while not adversely effecting collector breakdown voltage or other desirable characteristics of the transistor. Incidentally, it may be possible to meet the electrical specification of a given registration without using epitaxial techniques. Component manufacturer's data should be consulted for process information.

From the various charge quantities introduced, a number of time constants can be described that relate the charge quantities to the currents flowing; these time constants are defined in the following equations

$$\tau_a = \frac{Q_B}{I_{BS}}$$

$$\tau_c = \frac{Q_B}{I_{CS}}$$

$$\tau_b = \frac{Q_{BX}}{I_{BX}}$$

τ_a is called the *active region lifetime*, τ_c is called the *collector time constant*, and τ_b is the *effective lifetime in the saturated region*. In some literature τ_b has been called τ_s. Where collector minority carrier storage exists the measurement method for τ_b shown in Chapter 18 does not only measure Q_{BX}/I_{BX} but includes much of the collector stored charge; as such, this parameter is still a valuable tool in rating the storage characteristics of various transistors since a low τ_b value indicates a low storage time. The time constants defined are *constant* over large regions of device usage and are normally specified as device constants.

To determine the transient response using the charge approach, the required charge for the time in question is divided by the current available to supply that charge; thus, the basic equations are

$$t_d = \frac{Q_E + Q_{CD}}{I_{B1}}$$

$$t_r = \frac{Q_B + Q_C}{I_{B1}} = \frac{\tau_c I_C + Q_C}{I_{B1}}$$

$$t_s = \frac{Q_{BX}}{I_{B2}} = \tau_b \frac{I_{BX}}{I_{B2}}, \text{ and}$$

$$t_f = \frac{Q_B + Q_C}{I_{B2}} = \frac{\tau_c I_C + Q_C}{I_{B2}}$$

The simplicity of these equations is readily seen. Their accuracy is dependent upon the assumption made in the equations that I_{B1} and I_{B2} truly are constant. Refinements in these equations arise from the fact that some of the charge in the base recombines on its own and must be accounted for in determining transient speed.

APPLICATION OF STORED CHARGE CONCEPTS

In calculating that portion of the delay time before the current begins to rise t_d', it was found necessary to employ the approximation

$$t_d' = \frac{Q_E + Q_{CD}}{I_{B\,(avg.)}}$$

in order to obtain a reasonably simple solution. Q_E is essentially the total charge which must be removed from the base emitter junction to turn on the device. Q_{CD}, however, is but a portion of the total charge stored at the base collector junction. During actual rise time, the remaining portion of this charge must be removed. Letting Q_{TC} be the total charge due to this capacitive effect, it is wise to separate Q_{TC} into two components, Q_{CD} and Q_C. Q_{CD} is then the charge removed during t_d' and Q_C is the charge removed during the rise time. It is rather obvious that the calculation for t_d' lends itself nicely to charge concepts.

RISE-TIME, t_r

Basically, only one mathematical relationship is involved in the remaining discussion. This will be briefly examined before dealing with the full solutions.

The equation,

$$\int_0^t i_B\, dt = \int_0^t \frac{dQ}{dt}\, dt + \int_0^t \frac{Q}{\tau_a}\, dt,$$

which may also be written in differential form as

$$i_B = \frac{d\,Q_B}{dt} + \frac{Q_B}{\tau_a},$$

is the fundamental governing equation in most practical approaches for determining the switching time intervals. This equation represents a *first order approximation* and should never be regarded as more than this.

The first term on the right hand side is simply the rate of change of Q_B with time (coulombs per second) and essentially represents the capacitive element in the equivalent circuit. The second term (often called the recombination term) is associated with resistance in the equivalent circuit and accounts for loss (leakage) of charge with time through the shunt resistance. τ_a is the RC time constant of the equivalent circuit and is often referred to as the recombination time constant. Initially, Q_B and the collector current are zero. At the end of the rise-time, Q_B and the collector current are at their final value. Two cases immediately present themselves. In the first case, the transistor does not enter saturation and the collector current stabilizes at $I_C = h_{FE} I_{B1}$, while in the second case the transistor enters saturation and the collector current is $I_{CS} < h_{FE} I_{B1}$ where the s in the subscript merely indicates saturation. I_{BS}, defined as I_{CS}/h_{FE}, is merely that base current which is just sufficient to bring the transistor to the edge of saturation. Thus $I_{B1} = I_{BS} + I_{BX}$ where I_{BX} is the *excess* base drive above that necessary to saturate the device.

As indicated in Figure 6.14(b), Q_B is related to I_C by the constant ω_T. Thus the final value of Q_B in the unsaturated case is $Q_B = I_C/\omega_T = I_C \tau_C$ while in the saturating case the final value for Q_B is given by $Q_B = I_{CS}/\omega_T = I_{CS} \tau_C$. Since $I_C = h_{FE} I_{B1}$ and $I_{CS} = h_{FE} I_{BS}$, then Q_B is related to I_B or I_{BS} as well. Thus $Q_B = I_{B1} h_{FE} \tau_C = I_{B1} \tau_a$.

For $I_B = I_{B1}$ where I_{B1} is a constant, the solution to the basic equation is

$$Q_B = A\epsilon^{\frac{-t}{\tau_a}} + B$$

where A and B are arbitrary constants determined by the boundary conditions. For example, at $t = 0$ we expect Q_B to be zero if the device is off and ready to be turned on. The above equations immediately reduce to $A + B = 0$ at $t = 0$. At $t = \infty$, the exponentional term has vanished and hence Q_B must be at its final value, Q_F. This makes $B = Q_F$ and we have

$$Q_B = -Q_F\epsilon^{\frac{-t}{\tau_a}} + Q_F = Q_F\left(1 - \epsilon^{\frac{-t}{\tau_a}}\right)$$

Naturally, if the device does not saturate, $Q_F = \tau_a I_{B1}$ and we then have

$$Q_B = \tau_a I_{B1}\left(1 - \epsilon^{\frac{-t}{\tau_a}}\right)$$

This equation may be solved for t as follows,

$$t_r = \tau_a \ln \frac{\tau_a I_{B1}}{\tau_a I_{B1} - Q_B(t)}$$

To find the rise time it is necessary to determine t_a, the time at which Q_B reaches 0.1

$\tau_a I_{B1}$ and t_b, the time at which Q_B reaches 0.9 $\tau_a I_{B1}$. The rise time from the 10 to 90 percent points is simply $t_b - t_a$ and we have

$$t = \tau_a \ln \frac{\tau_a I_{B1}}{\tau_a I_{B1} - 0.9\,\tau_a I_{B1}} - \tau_a \ln \frac{\tau_a I_{B1}}{\tau_a I_{B1} - 0.1\,\tau_a I_{B1}} = \tau_a \ln 9 = 2.2\,\tau_a$$

The rise time from zero to 90 percent is simply $t_r = \tau_a \ln 10 \cong 2.3\,\tau_a$. Thus the turn-on time is

$$T_{ON} = \frac{Q_E + Q_{CD}}{I_{B\,(avg.)}} + 2.3\,\tau_a$$

and the total turn on delay is given by

$$t_d = \frac{Q_B + Q_{CD}}{I_{B\,(avg.)}} + 0.1\,\tau_a$$

For the saturating case a more complicated situation arises. Q_B is limited to Q_{BS}, the charge required to just reach the edge of saturation. Q_{BS}, of course, is simply equal to $\tau_a I_{BS}$ and hence if the 10 to 90 percent points of $\tau_a I_{BS}$ are taken, the solution becomes

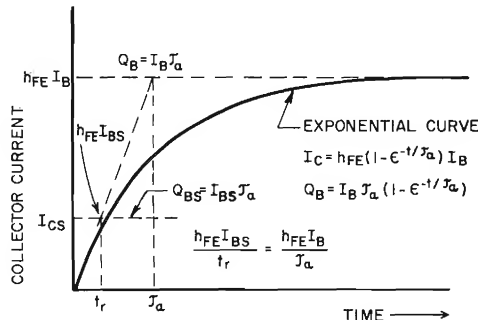
$$t_r = \tau_a \ln \frac{I_{B1} - 0.1\,I_{BS}}{I_{B1} - 0.9\,I_{BS}}$$

Frequently approximations are made in solving for t in order to simplify the mathematics. For example, for $t << \tau_a$, $d\,Q_B/dt$ is the only factor of importance and we have

$$I_{B1} \cong \frac{d\,Q_B}{dt} \cong \frac{\Delta Q_B}{\Delta t}$$

or

$$\Delta t = \frac{\Delta Q_B}{I_{B1}} = \frac{Q_{BS}}{I_{B1}} = \tau_a \frac{I_{BS}}{I_{B1}}$$

where Δt is simply the time interval of interest and ΔQ the total change in charge. For $\Delta t = t_r$, Q_B must go from zero to Q_{BS} and hence $\Delta Q_B = Q_{BS}$ and $t_r \cong Q_{BS}/I_{B1}$. As can be seen from Figure 6.16, for t appreciably less than τ_a, it is necessary that Q_{BS} be appreciably less than $\tau_a I_{B1}$. This occurs, of course, in the saturating case.

APPROXIMATE SOLUTION FOR RISE-TIME
Figure 6.16

A second approximation, which attempts to correct somewhat for the recombination term is sometimes used. Essentially, the original differential equation is written as

$$\frac{d\,Q_B}{dt} = I_{B1} - \frac{Q_B}{\tau_a}$$

The final value of Q_B is $Q_{BS} = I_{BS}\, t_r$. Assuming that Q_B is roughly linear with

time, we have $Q_B \cong I_{BS}\, t$ for $0 \leq t \leq t_r$. It follows that

$$\int_0^{t_r} \frac{d\,Q_B}{dt}\,dt = \int_0^{Q_{BS}} d\,Q_B = Q_{BS} = I_{B1}\,t_r - \frac{I_{BS}\,t_r^2}{2\tau_a} = \left[I_{B1} - \frac{Q_{BS}}{2\tau_a} \right] t_r$$

or

$$t_r = \frac{Q_{BS}}{I_{B1} - \frac{Q_{BS}}{2\tau_a}} = \frac{Q_{BS}}{I_{B1} - 0.5\,I_{BS}} = \frac{\tau_a I_{BS}}{I_B - 0.5\,I_{BS}}$$

Although the logarithmetic solution is the exact solution for the basic equation while these last two are only approximate solutions, it should be kept in mind that the *basic equation itself* is only an approximation.

The three solutions obtained for t_r should be compared.

$$t_r \cong \tau_a \frac{I_{BS}}{I_{B1}} (0 \text{ to } 100\%) \qquad (6a)$$

$$t_r \cong \tau_a \frac{I_{BS}}{I_B - 0.5\,I_{BS}} (0 \text{ to } 100\%) \qquad (6b)$$

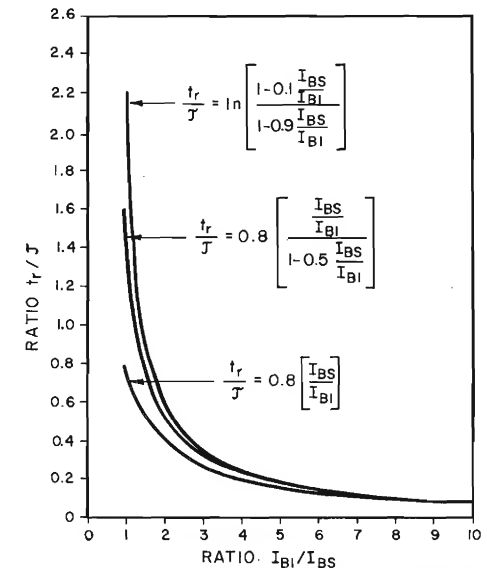
$$t_r \cong \tau_a \ln \left[\frac{I_B - 0.1\,I_{BS}}{I_B - 0.9\,I_{BS}} \right] (10\% \text{ to } 90\%) \qquad (6c)$$

To alter (6a and 6b) to read from 10% to 90% we need only multiply by the factor 0.8. Thus

$$t_r \cong 0.8\,\tau_a \frac{I_{BS}}{I_B} \qquad (6d)$$

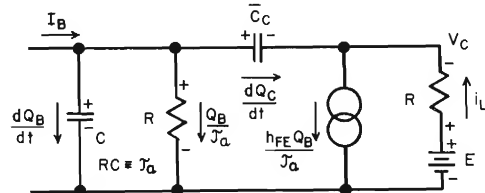
$$t_r \cong 0.8\,\tau_a \frac{I_{BS}}{I_B - 0.5\,I_{BS}} \qquad (6e)$$

Figure 6.17 gives a comparison of the predicted rise-time for each of the three approximations. The steepness of the curve below $I_B/I_{BS} = 3$ indicates that none of the equations will be in good agreement, whereas above $I_B/I_{BS} = 3$ all the curves tend to converge.

COMPARISON OF CALCULATED SWITCHING TIME FOR SEVERAL APPROXIMATIONS
Figure 6.17

COMPLETE SOLUTIONS

The simple solutions obtained for rise time in the previous section are not really adequate in that two very important factors have been ignored. The most important of these two remaining factors is the effect of C_C on the rise and fall times. During either of these two intervals, the device is passing through the active region and C_C acts as a feedback capacitor from output to input. Hence the effects produced by this parameter are much greater than one would assume from its capacitive value alone.

To modify the basic charge equation, it is only necessary to realize that at saturation all charge is effectively removed from C_C due to the fact that the collector voltage approaches very closely that of the base. Thus a charge $Q_C = \bar{C}_C\,dV$ must be removed during the rise-time. (Note that C_C is no longer the same as C_{CD}, as the base voltage is not changing very much during this interval.) Thus the modified charge equation becomes

$$I_{B1} = \frac{d\,Q_B}{dt} + \frac{Q_B}{\tau_a} + \frac{d\,Q_C}{dt}$$

(a) $Q_C \cong -\bar{C}_C V_C$

(b) $i_L = \frac{h_{FE}Q_B}{\tau_a} - \frac{dQ_C}{dt} \cong \frac{h_{FE}Q_B}{\tau}$

(c) $\frac{dQ_C}{dt} \cong -\bar{C}_C \frac{d}{dt}\left[E - \frac{h_{FE}Q_B}{\tau_a}R_L\right] = \frac{\bar{C}_C R_L h_{FE}}{\tau_a}\frac{dQ_B}{dt}$

EFFECT OF C_C ON SWITCHING WITH SIMPLIFYING ASSUMPTIONS

Figure 6.18

An equivalent circuit is given in Figure 6.18. A word of caution is in order here. The base voltage is not changing appreciably during the rise-time and this circuit indicates that it should. Any derivations, therefore, should assume that only V_C is effectively present across C_C while still permitting C_C to rob base current.

By using the relationships shown in Figure 6.18, the equation may be rearranged as follows:

$$\frac{I_{B1}}{1 + \left[\frac{h_{FE}\,\bar{C}_C\,R_L}{\tau_a}\right]} = \frac{d\,Q_B}{dt} + \frac{Q_B}{\tau_a + h_{FE}\,\bar{C}_C\,R_L}$$

The solution to this equation is, after applying the necessary boundary values,

$$Q_B = I_{B1}\,\tau_a\left(1 - \epsilon^{-\frac{t}{\tau_a + h_{FE}\bar{C}_C R_L}}\right)$$

which indicates that the effective time constant has been increased from τ_a to $\tau_a + h_{FE}\,\bar{C}_C\,R_L$. The effect of $\bar{C}_C$ has been multiplied by h_{FE}. Thus the simple formulas

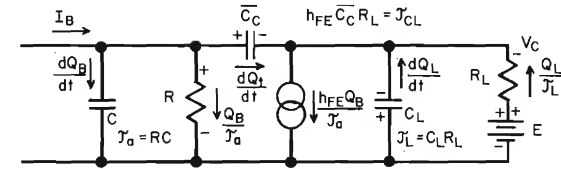
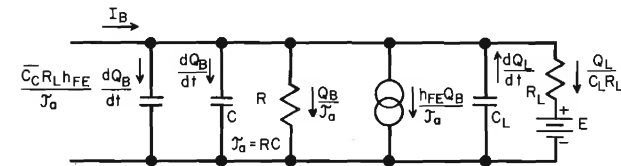
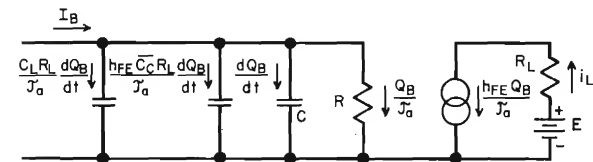
previously given are still valid provided the time constant is replaced with the new value.

We now consider the last effect, namely the effect of a shunt capacitance across the load. Figure 6.19 is an equivalent circuit of this condition. The basic charge equation is simply enlarged to include the charge Q_L, which must be removed from C_L during the switching interval.

$$I_B = \frac{d\,Q_B}{dt} + \frac{Q_B}{\tau_a} + \frac{d\,Q_C}{dt} + \frac{d\,Q_L}{dt}$$

By inspection, it is evident that Q_L will increase the effective time constant in a manner analogous to the increase in the effective time-constant with Q_C. There will, however, be some interaction between $\bar{C}_C$ and C_L, and it is obvious that an exact solution to this equation will involve several time constants and, indeed, be transcendental in nature. It is best, therefore, to make some approximations in order to achieve a solution which will be solvable for time.

The component of current flowing through $\bar{C}_C$ is very much less effective in the collector circuit than it is in the base circuit where it robs some of the driving current available for turning on the device. From the previous discussion where $\bar{C}_C$ alone was considered, it was found that the current taken by $\bar{C}_C$ was

$$\frac{d\,Q_C}{dt} \cong \frac{\bar{C}_C\,R_L\,h_{FE}}{\tau_a}\,\frac{d\,Q_B}{dt}$$

(a) EQUIVALENT CIRCUIT INCLUDING $\bar{C}_C$ AND C_L

(b) REDUCED EQUIVALENT CIRCUIT

(c) APPROXIMATION FOR OBTAINING A USEFUL SOLUTION

APPROXIMATE SOLUTION TO THE COMPLETE SWITCH PROBLEM

Figure 6.19

Figure 6.19(b) is a simplification of Figure 6.19(a) in that $\bar{C}_C$ has been removed and an equivalent capacitance placed in the base circuit to account for this effect.

The collector circuit contains two components of current which are related by

$$\frac{h_{FE} Q_B}{\tau_a} = \frac{d Q_L}{dt} + \frac{Q_L}{C_L R_L}$$

After steady state conditions are achieved, the capacitive current disappears and we obtain

$$\frac{h_{FE} \Delta Q_B}{\tau_a} = \frac{\Delta Q_L}{C_L R_L}$$

or

$$\Delta Q_L = \frac{h_{FE} C_L R_L}{\tau_a} \Delta Q_B$$

where ΔQ_L is the change in the charge on C_L and ΔQ_B is the change in the charge on C in the base circuit. Since these changes are essentially complete in a time interval Δt, an average or equivalent steady current, i_{CL}, must have been supplied which may be written

$$i_{CL} = \frac{h_{FE} C_L R_L}{\tau_a} \frac{\Delta Q_B}{\Delta t} = \frac{\Delta Q_L}{\Delta t}$$

and must correspond to a component of the base current, i_{BL}. With $i_{BL} = i_{CL}/h_{FE}$, we have

$$i_{BL} = \frac{C_L R_L}{\tau_a} \frac{\Delta Q_B}{\Delta t} = \frac{1}{h_{FE}} \frac{\Delta Q_L}{\Delta t}$$

This base current must act to rob some of the drive current available for driving the load during the switching interval only. If the approximations

$$\frac{\Delta Q_B}{\Delta t} \cong \frac{d Q_B}{dt}$$

$$\frac{\Delta Q_L}{\Delta t} \cong \frac{d Q_C}{dt}$$

are used, then one may write

$$i_{BL}(t) \cong \frac{C_L R_L}{\tau_a} \frac{d Q_B}{dt}$$

Thus the equivalent circuit of Figure 6.19(b) may be further reduced to that of Figure 6.19(c). It is now possible to write the expanded charge equation as

$$I_B = \frac{d Q_B}{dt} + \frac{Q_B}{\tau_a} + \left(\frac{h_{FE} \bar{C}_C R_L}{\tau_a}\right) \frac{d Q_B}{dt} + \left(\frac{C_L R_L}{\tau_a}\right) \frac{d Q_B}{dt}$$

which has as the general solution

$$Q_B = I_{B1} \tau_a \left(1 - \epsilon^{-\frac{t}{\tau_a + h_{FE} \bar{C}_C R_L + C_L R_L}}\right)$$

in which it is immediately seen that the time constant is $\tau_a + h_{FE} \bar{C}_C R_L + C_L R_L$ and the time solution from the 10 to 90 percent points would be

$$t_r = \tau_R \ln \left[\frac{I_{B1} - 0.1 I_{BS}}{I_{B1} - 0.9 I_{BS}}\right]$$

where

$$\tau_R = \tau_a + h_{FE} \bar{C}_C R_L + C_L R_L$$

$$= h_{FE}\left[\frac{1}{\omega_T} + \bar{C}_C R_L + \frac{C_L R_L}{h_{FE}}\right] = h_{FE} \tau_{RE}$$

if $\tau_a/h_{FE} = 1/\omega_T$. The constant τ_{RE} insert is called the rise-time constant by J. A. Ekiss and C. D. Simmons.[1] The development here, while not quite identical to the work of Simmons and Ekiss, nevertheless has the same result.

Although the time constant τ_a has been treated as a constant, in general τ_a does vary somewhat with operating conditions. Since τ_a is taken as h_{FE}/ω_T and both h_{FE} and ω_T are functions of operating point, this is only reasonable. The assumption of constancy is frequently justified in that the variation of τ_a is less than either h_{FE} or ω_T alone, the variation with operating point is frequently less than the variation from unit to unit in many types, and the variation is frequently masked to some extent by $h_{FE} \bar{C}_C$ which can have an appreciable influence on rise-time.

Storage-Time, t_s

Of all the switching time intervals, storage-time has generally been the most difficult to predict. No one has, as yet, determined a sufficiently general approach for calculating storage-time with reasonable accuracy, and with a reasonably (useful) simple solution that will apply to any junction transistor regardless of type or geometry. The stored charge approach has a simple solution but is reasonably accurate for a limited number of transistor processes.

Reverse Drive, I_{B2}

During the storage interval of the transistor, the base voltage remains virtually at the same value as during the "on" interval. Examination of Figure 6.10(c), for example, indicates that immediately after the switch is opened, the base to emitter remains slightly forward biased. Since point A is no longer held at +10V, this implies a current flow from base, through R_B and the 100Ω resistor, to the −10V supply. This current, whose magnitude is about 0.5 milliamperes, must flow from the base of the transistor and is usually referred to as I_{B2}. It represents a *reverse* current from the base to shut the device off. The symbol I_{B2} represents magnitude only and $I_B = -I_{B2}$ during this interval.

Circuit Conditions and Initial Conditions

During storage-time, the collector voltage and current and the base to emitter voltage remain constant. Since this is so, the capacitances C_C and C_E are not effective since no voltage change implies no capacitive current. Thus the only parameters of interest for the basic charge equation are the active region charge Q_B and the excess stored charge Q_{BX}. The basic equation becomes

$$I_B = \frac{d Q_B}{dt} + \frac{Q_B}{\tau_a} + \frac{d Q_{BX}}{dt} + \frac{Q_{BX}}{\tau_b}$$

Before turn-off, the base current was $I_B = I_{B1}$. At the point where $I_C = I_{CS}$, the base current necessary to maintain I_{CS} is $I_{BS} = I_{CS}/h_{FE} = Q_B/\tau_a$. The difference $I_{B1} - I_{BS}$ is I_{BX}, an excess base drive which forces the device into saturation. At this time Q_B has reached its final value and hence $d Q_B/dt = 0$. Thus initially we have

$$I_{B1} = \frac{Q_B}{\tau_a} + \frac{d Q_{BX}}{dt} + \frac{Q_{BX}}{\tau_b}$$

or

$$I_{B1} - I_{BS} = \frac{d Q_{BX}}{dt} + \frac{Q_{BX}}{\tau_b} = I_{BX}$$

which has the simple solution

$$Q_{BX} = \tau_B I_{BX} \left(1 - \epsilon^{\frac{-t}{\tau_b}}\right) \qquad (6f)$$

Obviously, the value of Q_{BX} is a function of the length of time the device is in saturation. Assuming the device has been in saturation for a time interval t_x, then the accumulated stored charge at the instant of turn-off will be some value $Q_{BX}(t_x)$.

For convenience, the storage-time is treated in two parts very similar to the treatment of the delay interval. That is, we have $t_s = t_s' + \Delta t_f$ in order to account for the

fact that t_s is actually measured to the point at which the collector current has fallen to its ten percent point. Thus t_s' is simply that interval before the collector current has begun to fall. The point at which Q_{BX} has been reduced to zero is the end of t_s'. It is furthermore assumed that Q_B does not change during t_s' and therefore $d\,Q_B/dt = 0$.

During t_s' the basic equation becomes

$$-I_{B2} - I_{BS} = \frac{d\,Q_{BX}}{dt} + \frac{Q_{BX}}{\tau_b}$$

which has the solution

$$Q_{BX} = [Q_{BX}(t_x) + \tau_b(I_{B2} + I_{BS})]\,\epsilon^{\frac{-t}{\tau_b}} - \tau_b(I_{B2} + I_{BS}) \qquad (6g)$$

Since $Q_{BX} = 0$ when $t = ts$, equation (6g) may be set equal to zero and solved for t_s' to give

$$t_s' = \tau_b \ln\left[\frac{Q_{BX}(t_x) + \tau_b(I_{B2} + I_{BS})}{\tau_b(I_{B2} + I_{BS})}\right] \qquad (6h)$$

For $t_x > 3\,\tau_b$ equation (6h) reduces to the more familiar form

$$t_s' = \tau_b \ln\left[\frac{I_{B2} + I_{B1}}{I_{B2} + I_{BS}}\right] \qquad (6i)$$

since Q_{BX} approaches $I_{BX}\,\tau_b$ as t_x becomes large.

As with the rise time solutions, various approximations are frequently used. The simplest being $t_s' = Q_{BX}/I_{B2}$. Naturally if $Q_{BX} = \tau_b\,I_{BX}$, this simply becomes $t_s' = \tau_b\,I_{BX}/I_{B2}$.

LIMITATIONS

The above approach has been most successful in describing the alloy type transistor, but far less successful in mesa and planar devices where minority charge can be stored not only in the base material but also in the bulk material of the rather high resistivity collector. Epitaxial construction essentially minimizes this by minimizing the amount of high resistivity material in the collector. It follows that some devices will follow very closely the solution for t_s' as given above, while other devices will only approximate this solution and still others will be wildly different.

To some extent the validity of the solution can be extended by considering τ_b as strictly a function of I_{CS}. Thus at different current levels there will be different values for τ_b, Figure 6.20 is an example of τ_b as a function of collector current for a planar device. From the τ_b curve, it is very obvious that τ_b is reasonably constant only at very low or very high currents. In the middle range, where the device is used most widely, τ_b is far from constant. If a curve of t_s and a curve of h_{FE} as functions of collector current are given, τ_b may be calculated for any collector current. If τ_b is given directly as a function of collector current, no calculations need be made and the proper value to use may be taken directly from the graph.

By using the corrected values of τ_b for the proper collector current level, changes in the drive conditions (I_{B1}, I_{B2}) act as small perturbations which alter the predicted result in roughly the proper direction to account for the observed change in storage time. The simple model, if used with care, can therefore be an effective tool in circuit analysis despite its weaknesses.

τ_s SPECIFICATION

A time constant τ_s is frequently used on specification sheets. This is a measurement of storage time, t_s, under the condition that $I_{CS} = I_{B1} = I_{B2}$. Assuming that $I_{BS} << I_{CS}$

under these conditions ($h_{FE} >> 1$), then

$$\tau_s = \tau_b \ln 2$$

or

$$\tau_b = 1.44\,\tau_s$$

τ_b is essentially the same as C. D. Simmons' Hole Storage Factor K's[2] used to describe the behavior of alloy devices.

VARIATION OF τ_b, t_s', AND h_{FE} WITH I_C

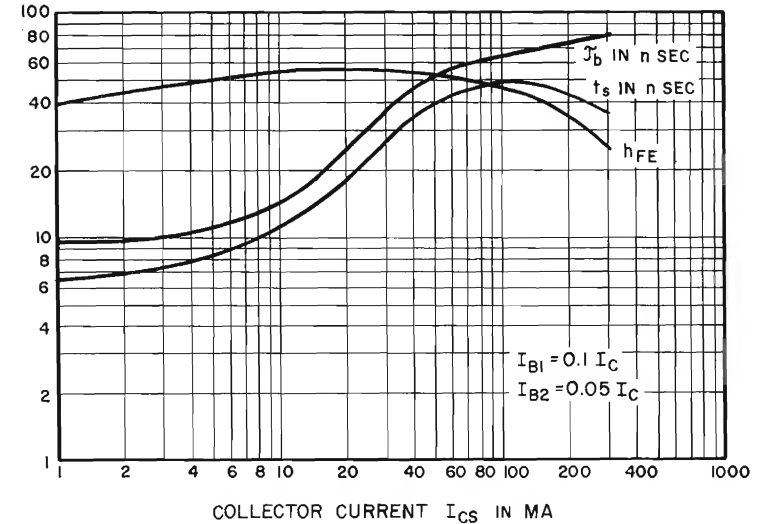



Figure 6.20

Method of Grinich and Noyce [3]

Because of the generally unsatisfactory nature of the simple approximation used above for storage time, a second approach has been suggested for diffused base structures in which minority carrier lifetime in the collector region is quite large.

In saturation, the collector-base diode becomes forward biased. Figure 6.21 is a simple sketch of an NPN transistor with a diode connected between base and collector to represent this forward biased collector-base diode. Thus the transistor is conceived as essentially unsaturated and the diode accounts for the saturation effect. In trying to turn off the device, it is necessary that the charge stored in the diode be removed before turn off can properly start. The recovery time of the diode is essentially the storage time interval of the transistor.

The standard diode reverse recovery formula as used in this analysis[2] is

$$\text{erf}\sqrt{\frac{t_s'}{\tau}} = \frac{I_f}{I_f + I_r}$$

where t_s' is the storage time or the time required by the diode to become reverse biased, I_f is the current (I_D) in the diode just prior to turn-off, I_r is the current ($-I_D$) in the diode during turn-off, and τ is the minority carrier lifetime in the collector. Solving for t_s' there is obtained

$$t_s' = \tau\left[\text{erf}^{-1}\left(\frac{I_f}{I_f + I_r}\right)\right]^2$$

Prior to turn-off $I_f = +I_D$ and $I_B = I_{B1}$. It follows that

$$I_f = I_D = \frac{h_{FE} I_{B1} - I_{CS}}{1 + h_{FE}}$$

After turn-off commences, $I_D = I_r$ and $I_B = -I_{B2}$. Therefore

$$I_r = -I_D = \frac{h_{FE} I_{B2} + I_{CS}}{1 + h_{FE}}$$

Making the proper substitutions the solution for t_s' becomes

$$t_s' = \tau \left[erf^{-1} \left(\frac{I_{B1} - I_{BS}}{I_{B2} + I_{B1}} \right) \right]^2 = \tau \left[erf^{-1} \left(\frac{I_{BX}}{I_{B2} + I_{B1}} \right) \right]^2$$

While theoretically τ should be the lifetime of minority carriers in the collector, the picture is somewhat confused by the available tables for the error function (erf). The error functions differ to the extent of a multiplying constant and thus it would appear that, in effect, $\tau = k\,\tau'$ where k is determined by the particular table being used and τ' is the lifetime of minority carriers in the collector.

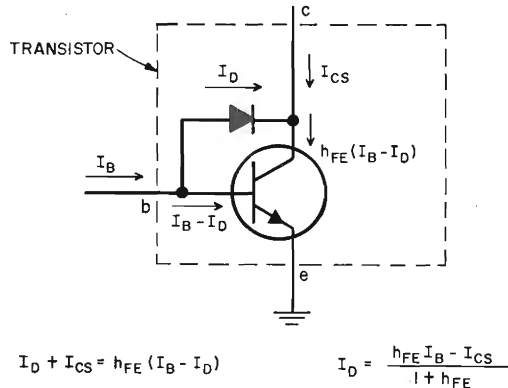
Essentially this approach assumes that the major portion of the storage time lies in clearing minority carriers from the high resistivity collector material and the excess base charge is quite insignificant.

SIMPLE EQUIVALENT CIRCUIT FOR ESTIMATING STORAGE TIME WHEN APPRECIABLE CHARGE IS LOCATED IN COLLECTOR

Figure 6.21

CALCULATION OF FALL-TIME, t_f

For devices where collector body storage is not an important factor, the parameters which affect fall-time are the same, or nearly the same, as those affecting the rise-time. The effect of C_C, C_L, τ_a, and R_L are all present during the turn-off interval. The basic charge equation is

$$I_B = \frac{d\,Q_B}{dt} + \frac{Q_B}{\tau_a} + \frac{d\,Q_C}{dt} + \frac{d\,Q_L}{dt}$$

which can be referred to Q_B only, as with rise-time, to obtain

$$I_B = \frac{d\,Q_B}{dt} + \left[1 + \frac{h_{FE} C_C R_L}{\tau_a} + \frac{C_L R_L}{\tau_a} \right] + \frac{Q_B}{\tau_a}$$

or

$$-I_{B2} = \frac{d\,Q_B}{dt} \frac{\tau_F}{\tau_a} + \frac{Q_B}{\tau_a}$$

where

$$\tau_F = \tau_a + h_{FE} C_C R_L + C_L R_L$$

which has the simple solution

$$Q_B = \tau_a (I_{B2} + I_{BS})\, \epsilon^{-t/\tau_F} - \tau_a I_{B2}$$

At the point where $Q_B = 0.9\, \tau_a I_{BS}$ the collector current has decreased 10 percent while at $Q_B = 0.1\, \tau_a I_{BS}$ the collector current has decreased 90 percent. The difference in time is t_f and given by

$$t_f = \tau_F \ln \left[\frac{I_{B2} + 0.9\, I_{BS}}{I_{B2} + 0.1\, I_{BS}} \right]$$

If there is any collector storage, or any other factor implied by saturation, the effective fall time-constant will be greater than the τ_F calculated. It is frequently the practice, therefore, to make separate measurements of the *effective* rise and fall time-constants.

In cases where collector storage is a very important phenomenon, the fall time-constant must be measured in order to use the above results. For this reason Simmons[1] uses $h_{FE}\, \tau_{RE}$ as the rise time-constant and $h_{FE}\, \tau_{FE}$ as the fall time-constant.

SUMMARY OF RESULTS

Of great importance to a proper appreciation of the problem involved in the prediction of transition times is an understanding that there is no exact solution which is applicable to every device. Furthermore, solutions obtained from a solution of the diffusion equation are usually based on an assumed geometry with simple boundary conditions which are not necessarily the same as the actual device. At any rate, the need to assume a geometry necessarily implies that the solution may not be valid for all geometries.

A solution which cannot be solved explicitly for time is of limited use to most design engineers and certainly even more limited in usefulness to hobbyists, experimenters, etc., most of whom do not have large scale digital computers available to solve any problem numerically. It is necessary to have available techniques for approximating the answers needed despite the fact that the approximations are limited in scope and do not always work very well.

Any transistor is a temperature dependent device. This means that any and all of the parameters involved are affected by temperature. In general, both the turn-on and turn-off intervals tend to increase with temperature. Turn-off, essentially that portion due to saturation, is generally affected more than the turn-on time.

Table 6.1 summarizes the most frequently encountered solutions. Obviously expressions other than those shown may be derived if one chooses a more elaborate model than the very simple RC circuit.

ANTI-SATURATION TECHNIQUES

Saturation implies the presence of turn-off delay or storage-time, t_s. The storage time is every bit as important as the rise or fall times, which are influenced primarily by $\tau_a = h_{FE}/\omega_T$ and parasitic capacities. Unfortunately, storage-time is not directly related to τ_a. That is, a small value of τ_a does not necessarily imply a small value for τ_b. The relationship of τ_b to the time constant developed by Moll[3,4] becomes quite remote when appreciable minority carrier storage begins to occur in the collector. Indeed, it is not incorrect to state that the gain-bandwidth product of a device is not a measure of its storage-time capabilities. Attempts are frequently made to operate the transistor in such a manner as to avoid saturation entirely. In pulsed systems,

TIME INTERVAL	FIRST APPROXIMATION	SECOND APPROXIMATION	THIRD APPROXIMATION	FOURTH APPROXIMATION
$t_d = T_{ON}$ (0 to 10%)	$\frac{Q_{CD}+Q_E}{I_{B1(AVG)}} + 0.1\frac{Q_B^*}{I_{B1}}$	$\frac{Q_{CD}+Q_E}{I_{B1(AVG)}} + 0.1\frac{Q_B^*}{I_{B1}-0.5I_{BS}}$		$\frac{Q_{CD}+Q_E}{I_{B1(AVG)}} + \tau_R \, LN \frac{I_{B1}}{I_{B1}-0.1I_{BS}}$
	$\frac{Q_{CD}+Q_E}{I_{B1(AVG)}} + 1/9\frac{Q_{B90}^*}{I_{B1}}$	$\frac{Q_{CD}+Q_E}{I_{B1(AVG)}} + 1/9\frac{Q_B^*}{I_{B1}-0.5I_{BS}}$		
$t_r = T_{ON}$ (10% to 90%)	$\frac{0.8\,Q_B^*}{I_{B1}}$	$0.8\frac{Q_B^*}{I_{B1}-0.5I_{BS}}$	$\tau_R \, LN\left[\frac{I_{B1}}{I_{B1}-I_{BS}}\right]$	$\tau_R \, LN\left[\frac{I_{B1}-0.1I_{BS}}{I_{B1}-0.9I_{BS}}\right]$
	$8/9\frac{Q_{B90}^*}{I_{B1}}$	$8/9\frac{Q_{B90}^*}{I_{B1}-0.5I_{BS}}$		
$t_s = T_{OFF}$ (90% to 100%)	$\tau_b\frac{I_{BX}}{I_{B2}} + 0.1\frac{Q_B^*}{I_{B2}}$	$\frac{\tau_b I_{BX}}{I_{B2}+0.5I_{BX}} + 0.1\frac{Q_B^*}{I_{B2}+0.5I_{BS}}$	$\tau\left[ERF^{-1}\left(\frac{I_{BX}}{I_{B2}+I_{B1}}\right)\right]^2$	$\tau_b \, LN\left[\frac{I_{B2}+I_{B1}}{I_{B2}+I_{BS}}\right]$
	$\tau_b\frac{I_{BX}}{I_{B2}} + 1/9\frac{Q_{B90}^*}{I_{B2}}$	$\frac{\tau_b I_{BX}}{I_{B2}+0.5I_{BX}} + 1/9\frac{Q_{B90}^*}{I_{B2}+0.5I_{BS}}$	$+\tau_F \, LN\left[\frac{I_{B2}+I_{BS}}{I_{B2}+0.9I_{BS}}\right]$	$+\tau_F \, LN\left[\frac{I_{B2}+I_{BS}}{I_{B2}+0.9I_{BS}}\right]$
$t_f = T_{OFF}$ (10% to 90%)	$0.8\frac{Q_B^*}{I_{B2}}$	$0.8\frac{Q_B^*}{I_{B2}+0.5I_{BS}}$	$\tau_F \, LN\left[\frac{I_{B2}+I_{BS}}{I_{B2}}\right]$	$\tau_F \, LN\left[\frac{I_{B2}+0.9I_{BS}}{I_{B2}+0.1I_{BS}}\right]$
	$8/9\frac{Q_{B90}^*}{I_{B2}}$	$8/9\frac{Q_{B90}^*}{I_{B2}+0.5I_{BS}}$		

$Q_B^* = Q_B + Q_C$

Q_{B90}^* = THAT PORTION OF $Q_B + Q_C$ REQUIRED TO REACH THE 90% 'ON' LEVEL

τ = TIME CONSTANT OR EFFECTIVE LIFETIME OF MINORITY CARRIERS IN COLLECTOR-BASE DIODE

$\tau_R = \tau_a + h_{FE}\overline{C}_C R_L + C_L R_L$ = RISE TIME CONSTANT

$\tau_F \gtrapprox \tau_a + h_{FE}\overline{C}_C R_L + C_L R_L$ = FALL TIME CONSTANT

τ_F NORMALLY SOMEWHAT GREATER THAN τ_R

SUMMARY OF APPROXIMATE SOLUTIONS TO SWITCHING TIME INTERVALS

Table 6.1

where the pulse width is very short compared to τ_b, the device may be permitted to reach saturation without incurring the penalty of long storage-time simply because the narrowness of the pulse does not permit sufficient time to build up appreciable storage charge. The forward recovery characteristics of the base to collector diode governs the rate at which charge is accumulated.

By and large, however, most approaches to the elimination of storage-time are simply techniques to eliminate the possibility of saturating the transistor. Some of the approaches will be discussed in the following paragraphs.

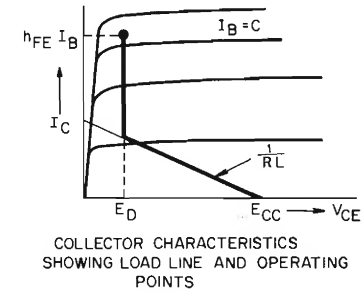
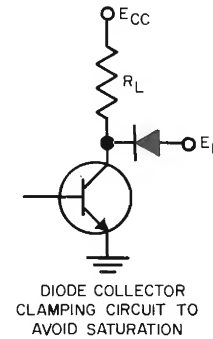
In general, the advantages of saturated switch design are: (a) simplicity of circuit design, (b) well defined voltage levels, (c) fewer parts required than in non-saturating circuits, (d) low transistor dissipation when conducting, and (e) immunity to short stray voltage signals. Against this must be weighed the probable reduction in circuit speed since higher trigger power is required to turn off a saturated transistor than one unsaturated.

COLLECTOR VOLTAGE CLAMP

Figure 6.22

A number of techniques are used to avoid saturation. The simplest is shown in Figure 6.22. The diode clamps the collector voltage so that it cannot fall below the base voltage to forward bias the collector junction. Response time is not improved appreciably over the saturated case since I_C is not clamped but rises to $h_{FE}I_B$. Typical variations of I_B and h_{FE} with temperature and life, for a standard transistor, may vary I_C by as much as 10:1. Care should be taken to ensure that the diode prevents saturation with the highest I_C. When the transistor is turned off I_C must fall below the value given by $(E_{CC} - E_D)/R_L$ before any change in collector voltage is observed. The time required can be determined from the fall-time equations in the section on transient response. The diode can also have a long recovery time from the high currents it has to handle. This can further increase the delay in turning off. Diodes such as the 1N3604 or 1N3606 have recovery times compatible with high speed planar epitaxial transistors.

It is not always obvious in design work that power will be an important consideration. During the on-time the power dissipated in the device is very close to being $h_{FE}\,I_B\,E_D$. Although I_B and E_D may be quite fixed in value, h_{FE} is not.

A much better way of avoiding saturation is to control I_B in such a way that I_C is just short of the saturation level. This can be achieved with the circuit of Figure 6.23(a). The diode is connected between a tap on the base drive resistor and the collector. When the collector falls below the voltage at the tap, the diode conducts diverting base current into the collector and preventing any further increase in I_C. The

voltage drop across R_2 is approximately $I_C R_2/h_{FE}$ since the current in R_2 is I_B. Since the voltage drop across the diode is approximately the same as the input voltage to the transistor, V_{CE} is approximately $I_C R_2/h_{FE}$. It is seen that if the load decreases (I_C is reduced) or h_{FE} becomes very high, V_{CE} decreases towards saturation. Where the change in h_{FE} is known and the load is relatively fixed, this circuit prevents saturation.

$$V_{CE} \approx \frac{R2\ E_{CC}}{R_L h_{FE} + R2} \approx \frac{E_{CC}\ R2}{R_L h_{FE}} \quad \text{IF } V_{CE} << E_{CC}$$

COLLECTOR CURRENT CLAMP WITHOUT BIAS SUPPLY

Figure 6.23(a)

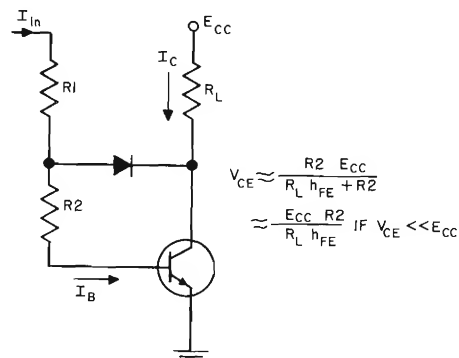
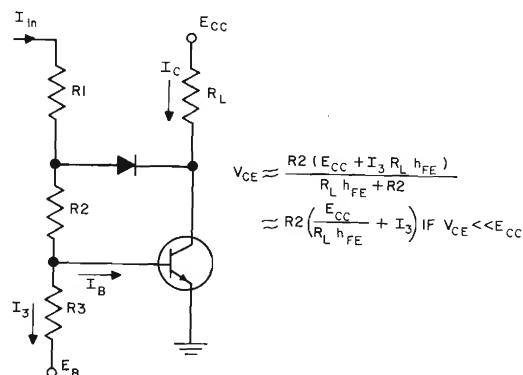
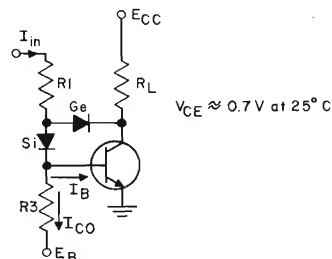
$$V_{CE} \approx \frac{R2\,(E_{CC} + I_3 R_L h_{FE})}{R_L h_{FE} + R2} \approx R2\left(\frac{E_{CC}}{R_L h_{FE}} + I_3\right) \quad \text{IF } V_{CE} << E_{CC}$$

COLLECTOR CURRENT USING BIAS SUPPLY

Figure 6.23(b)

To avoid the dependence of V_{CE} on I_C and h_{FE}, R_3 may be added as in Figure 6.23(b). By returning R_3 to a bias voltage, an additional current is drawn through R_2. Now V_{CE} is approximately $(I_C/h_{FE} + I_3)\ R_2$. I_3 can be chosen to give a suitable minimum V_{CE}.

COLLECTOR CURRENT CLAMP USING SILICON AND GERMANIUM DIODES

Figure 6.23(c)

The power consumed by R_3 can be avoided by using the circuit of Figure 6.23(c), provided a short lifetime transistor is used. Otherwise fall-times may be excessively long. R_3 is chosen to reverse bias the emitter at the maximum I_{CO}. The silicon diode replaces R_2. Since the silicon diode has a forward voltage drop of approximately 0.7 volt over a considerable range of current, it acts as a constant voltage source making V_{CE} approximately 0.7 volt. If considerable base drive is used, it may be necessary to use a high conductance germanium diode to avoid momentary saturation as the voltage drop across the diode increases to handle the large base drive current.

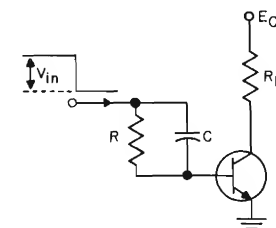
In applying the same technique to silicon transistors with low saturation resistance, it is possible to use a single germanium diode between the collector and base. While this permits V_{CE} to fall below V_{BE}, the collector diode remains essentially non-conducting since the 0.7 volt forward voltage necessary for conduction cannot be reached with the germanium diode in the circuit.

Diode requirements are not stringent. The silicon diode need never be back biased, consequently, any diode will be satisfactory. The germanium diode will have to withstand the maximum circuit V_{CE}, conduct the maximum base drive with a low forward voltage, and switch rapidly under the conditions imposed by the circuit, but these requirements are generally easily met.

Care should be taken to include the diode leakage currents in designing these circuits for high temperatures. All the circuits of Figure 6.23 permit large base drive currents to enhance switching speed, yet they limit both I_B and I_C just before saturation is reached. In this way, the transistor dissipation is made low and uniform among transistors of differing characteristics.

It is quite possible to design flip-flops which will be non-saturating without the use of clamping diodes by proper choice of components. The resulting flip-flop is simpler than that using diodes but it does not permit as large a load variation before malfunction occurs. Design procedure for an unclamped non-saturating flip-flop can be found in *Transistor Circuit Engineering* by R. F. Shea, et al (John Wiley & Sons, Inc).

STORED CHARGE NEUTRALIZATION BY CAPACITOR

Figure 6.24

Another circuit which is successful in minimizing storage-time is shown in Figure 6.24. If the input is driven from a voltage source, it is seen that if the input voltage and capacitor are appropriately chosen, the capacitor charge can be used to neutralize the stored charge, in this way avoiding the storage-time delay. In practical circuits, the RC time constant in the base necessary for this action limits the maximum pulse repetition rate.

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(1) Ekiss, J. A., Simmons, C. D., "Junction Transistor Transient Response Characterization, Parts I and II," *The Solid State Journal,* January and February, 1961.

(2) Simmons, C. D., "Hole, Storage Delay Time and its Prediction," *Semiconductor Products,* May/June 1958.

(3) Grinich, V., and Noyce, R., "Switching Time Calculations for Diffused Base Transistors," presented at IRE — Wescon, August 22, 1958.

(4) Chen, C. H., "Predicting Reverse Recovery Time of High Speed Semiconductor Diodes," General Electric Application Note 90.36.

NOTES

DIGITAL CIRCUITRY

CHAPTER 7

INTRODUCTION

In a digital computer the numerical values change in discrete steps. An example of a digital computer is the ordinary desk calculator or adding machine. In an electronic digital computer numerical values involved in the calculation are represented by the discrete states of flip-flops and other switching circuits in the computer. Numerical calculations are carried out in digital computers according to the standard rules of addition, subtraction, multiplication and division. Digital computers are used primarily in cases where high accuracy is required such as in standard accounting work. For example, most desk calculators are capable of giving answers correct to one part in one million, but a slide rule (analog computer) would have to be about ⅙ of a mile long to be read to the same accuracy.

The transistor's small size, low power requirements and inherent reliability have resulted in its extensive use in digital computers. Special characteristics of the transistor such as low saturation resistance, low input impedance, and complementary NPN and PNP types, have permitted new types of digital circuits which are simple, efficient and fast. Computers operating at speeds of 5 megacycles are a commercial reality, and digital circuits have been proved feasible at 160 megacycles.

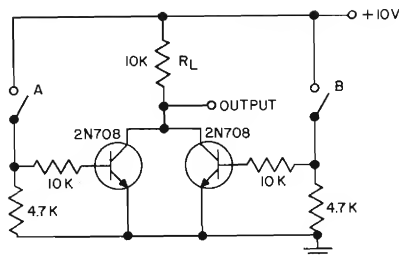
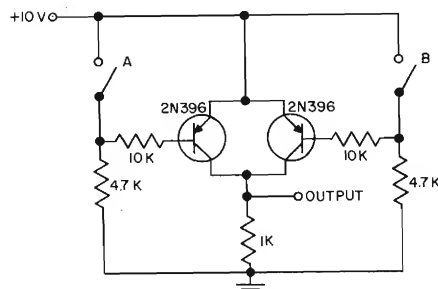
This chapter offers the design engineer practical basic circuits and design procedures based on proven techniques and components. Flip-flops are discussed in detail because of their extensive use in digital circuits as memory elements.

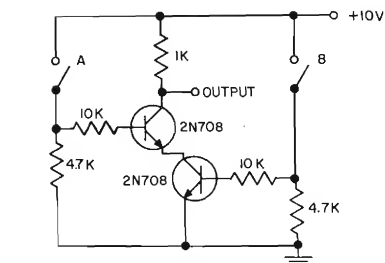
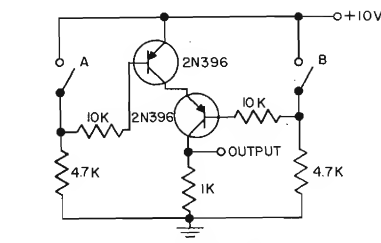
BASIC CIRCUITS

Methods for using transistors in gate circuits are illustrated in Figure 7.1. The base of each transistor can be connected through a resistor either to ground or a positive voltage by operating a switch. In Figure 7.1(A) if both switches are open, both transistors will be non-conducting except for a small leakage current. If either switch A *or* switch B is closed, current will flow through R_L. If we define *closing* a switch as being synonymous with applying an input then we have an "OR" gate. When either switch is closed, the base of the transistor sees a positive voltage, therefore, in an "OR" gate the output should be a positive voltage also. In this circuit it is negative, or "NOT OR". The circuit is an "OR" gate with phase inversion. It has been named a "NOR" circuit. Note that if we define *opening* a switch as being synonymous with applying an input, then we have an "AND" circuit with phase inversion since both switch A *and* switch B must be open before the current through R_L ceases. We see that the same circuit can be an "AND" or an "OR" gate depending on the polarity of the input.

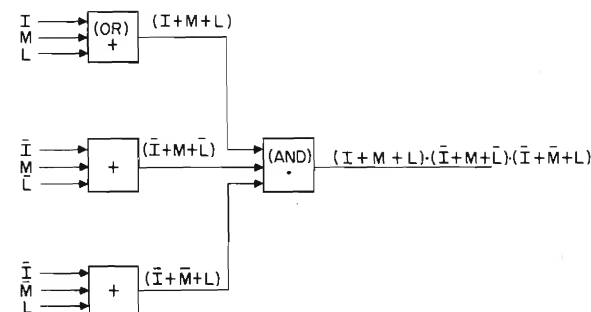
The circuit in Figure 7.1(B) has identically the same input and output levels but uses PNP rather than NPN transistors. If we define closing a switch as being an input, we find that both switches must be closed before the current through R_L ceases. Therefore, the inputs which made the NPN circuit an "OR" gate make the PNP circuit an "AND" gate. Because of this, the phase inversion inherent in transistor gates does not complicate the overall circuitry.

Figure 7.2(A) and (B) are very similar to Figure 7.1(A) and (B) except that the transistors are in series rather than in parallel. This change converts "OR" gates into "AND" gates and vice versa.

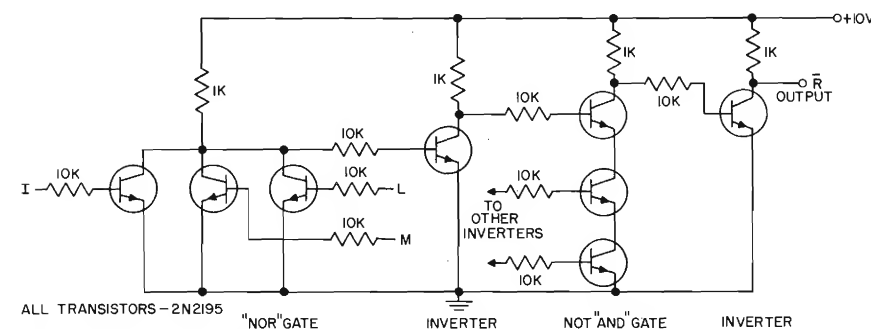
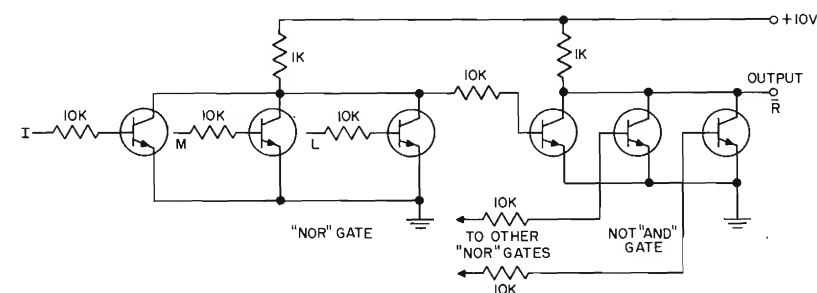
Looking at the logic of Figure 7.2, let us define an input as a positive voltage; a lack of an input as zero voltage. By using the circuit of Figure 7.1(A) with three

(A) GATE USING NPN TRANSISTORS
IF CLOSING A SWITCH IS AN INPUT, THIS IS AN "OR" GATE
IF OPENING A SWITCH IS AN INPUT, THIS IS AN "AND" GATE
NOTE: PHASE INVERSION OF INPUT

(B) GATE USING PNP TRANSISTORS
IF CLOSING A SWITCH IS AN INPUT THIS IS AN "AND" GATE
IF OPENING A SWITCH IS AN INPUT THIS IS AN "OR" GATE
NOTE: PHASE INVERSION OF INPUT

BASIC LOGIC CIRCUITS USING PARALLEL TRANSISTORS
Figure 7.1

(A) GATE USING NPN TRANSISTORS
IF CLOSING A SWITCH IS AN INPUT THIS IS AN "AND" GATE
IF OPENING A SWITCH IS AN INPUT THIS IS AN "OR" GATE
NOTE: PHASE INVERSION OF INPUT

(B) GATE USING PNP TRANSISTORS
IF CLOSING A SWITCH IS AN INPUT THIS IS AN "OR" GATE
IF OPENING A SWITCH IS AN INPUT THIS IS AN "AND" GATE
NOTE: PHASE INVERSION OF INPUT

BASIC LOGIC CIRCUITS USING SERIES TRANSISTORS
Figure 7.2

transistors in parallel, we can perform the "OR" operation but we also get phase inversion. We can apply the output to an inverter stage which is connected to an "AND" gate of three series transistors of the configuration shown in Figure 7.2(A).

TYPICAL LOGIC DIAGRAM
Figure 7.3

An output inverter stage would also be required. This is shown in Figure 7.4(A).

By recognizing that the circuit in Figure 7.1(A) becomes an "AND" gate if the input signal is inverted, the inverters can be eliminated as shown in Figure 7.4(B).

(A) INVERTERS COMPENSATE FOR PHASE INVERSION OF GATES

(B) PHASE INVERSION UTILIZED TO ACHIEVE "AND" AND "OR" FUNCTIONS FROM THE SAME CIRCUIT

CIRCUITS REPRESENTING $(I + M + L)(\bar{I} + M + \bar{L})(\bar{I} + \bar{M} + L) = \bar{R}$
Figure 7.4

If the transistors are made by processes yielding low saturation voltages and high base resistance, the series base resistors may be eliminated. Without these resistors the logic would be called direct-coupled transistor logic DCTL. While DCTL offers extreme circuit simplicity, it places severe requirements on transistor parameters and does not offer the economy, speed or stability offered by other logical circuitry.

The base resistors of Figure 7.4 relax the saturation voltage and base input voltage requirements. Adding another resistor from each base to a negative bias potential would enhance temperature stability.

Note that the inputs include both "on" and "off" values of all variables e.g., both I and $\bar{I}$ appear. In order that the gates function properly, I and $\bar{I}$ cannot both be positive simultaneously but they must be identical and oppositely phased, i.e. when I is positive $\bar{I}$ must be zero and vice versa. This can be accomplished by using a phase inverter to generate $\bar{I}$ from I. Another approach, more commonly used, is to take I and $\bar{I}$ from opposite sides of a symmetrical flip-flop.

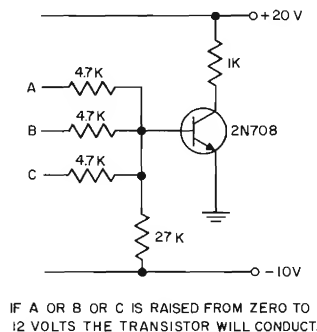
IF A OR B OR C IS RAISED FROM ZERO TO 12 VOLTS THE TRANSISTOR WILL CONDUCT.

BASIC NOR CIRCUIT

Figure 7.5

"NOR" logic is a natural extension of the use of resistors in the base circuit. In the circuit of Figure 7.5, if any of the inputs is made positive, sufficient base current results to cause the transistor to conduct heavily. The "OR" gating is performed by the resistors; the transistor amplifying and inverting the signal. The logic of Figure 7.3 can now be accomplished by combining the "NOR" circuit of Figure 7.5 with the "AND" circuit of Figure 7.2(A). The result is shown in Figure 7.5. In comparing the circuits in Figures 7.4(A) and 7.6, we see that the "NOR" circuit uses one-fourth as many transistors and one-half as many resistors as the brute force approach. In fact if we recall that the equation we are dealing with gives $\bar{R}$ rather than R, we see that we can get R by removing the output phase inverter and making use of the inherent inversion in the "NOR" circuit. In the circuit of Figure 7.5 two supply voltages of +20 and −10 volts are used. The −10 volt supply is to insure that the transistor is held off when I_{co} increases at elevated temperatures. If silicon transistors (such as the 2N708, 2N914, or 2N2193A) are used in NOR logic circuits the hold off supply may not be necessary. Since V_{BE} is larger for silicon devices and I_{co} is very low a resistor returned to the emitter reference may result in sufficient circuit stability.

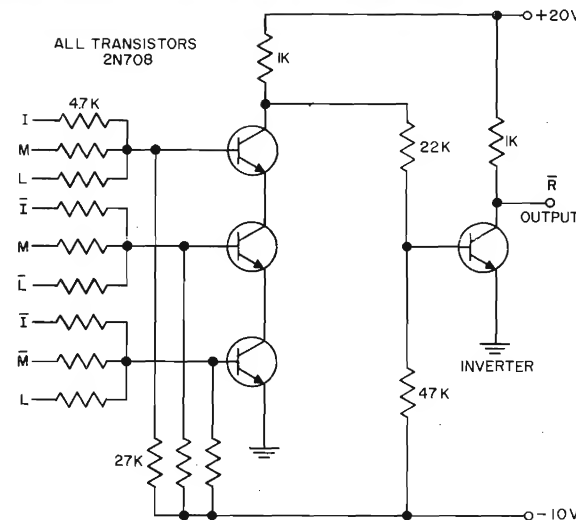
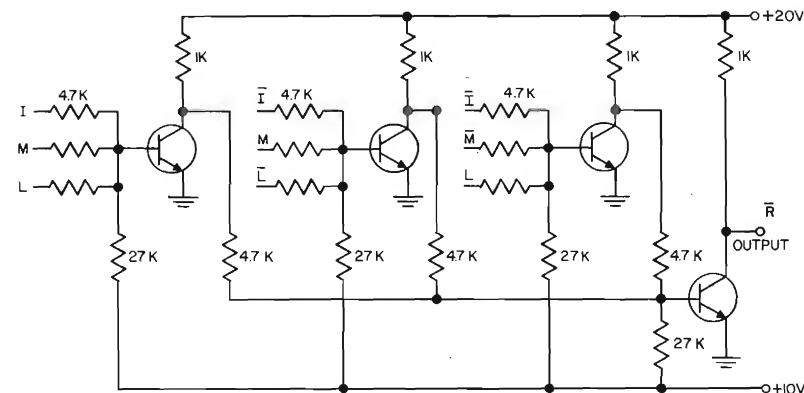
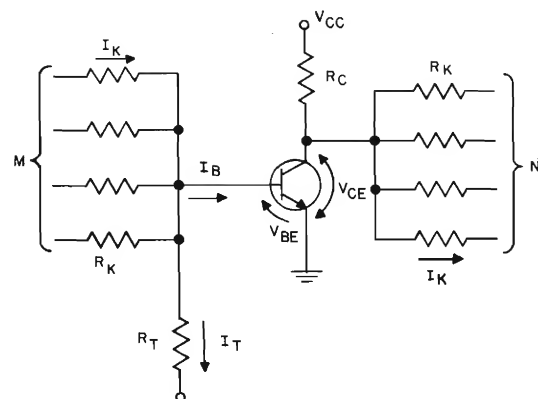
Because of the fact that a generalized Boolean equation can be written as a series of "OR" gates followed by an "AND" gate as was shown, it follows that such equations can be written as a series of "NOR" gates followed by a "NOR" gate. The low cost of the resistors used to perform the logic and the few transistors required make "NOR" logic attractive.

(A) NOR LOGIC USING SERIES TRANSISTORS FOR "AND" GATE

(B) NOR LOGIC USING INVERSION FOR "AND" GATE

Figure 7.6

A detailed "NOR" building block is shown in Figure 7.7. The figure defines the basic quantities. The circuit can readily be designed with the aid of three basic equations. The first derives the current I_K under the worst loading conditions at the collector of a stage.

$$I_K = \frac{V_{CC} - V_{BE} - I_{COM}R_C}{R_K + NR_C} \qquad (7a)$$

where I_{COM} is the maximum I_{CO} that is expected at the maximum junction temperature. The second equation indicates the manner in which I_K is split up at the base of the transistor.

$$I_K = I_B + \frac{M\,(V_{CEM} - V_{CEN} + V_{BE} - V_{EB}) - (V_{BE} - V_{CEN})}{R_K} + I_{COM} \qquad (7b)$$

DEFINITIONS

I_K = MINIMUM CURRENT THROUGH R_K FOR TURNING TRANSISTOR ON
I_B = MINIMUM BASE CURRENT FOR TURNING TRANSISTOR ON
I_T = BIAS CURRENT TO KEEP TRANSISTOR OFF AT HIGH TEMPERATURES
M = MAX. NUMBER OF INPUTS PERMITTED
N = MAX. NUMBER OF OUTPUTS PERMITTED
V_{BE} = MAX. BASE TO EMITTER VOLTAGE WHEN THE TRANSISTOR IS ON.
V_{CE} = MAX. COLLECTOR TO EMITTER VOLTAGE WHEN THE TRANSISTOR IS ON.

CIRCUIT USED FOR DESIGN OF NOR CIRCUITRY
Figure 7.7

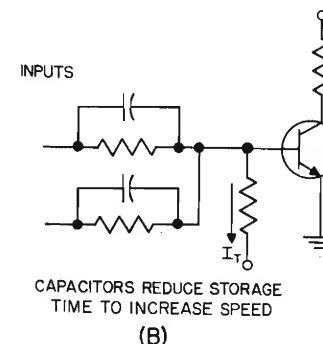
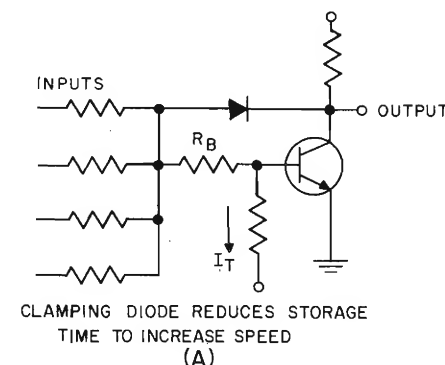
where V_{CEN} is the minimum expected saturation voltage, V_{CEM} is the maximum expected saturation voltage and V_{EB} is the reverse bias required to reduce the collector current to I_{CO}. V_{EB} is a negative voltage. The third equation ensures that V_{EB} will be reached to turn off the transistor.

$$I_T = I_{COM} + \frac{(V_{CEM} - V_{EB})M}{R_K} \qquad (7c)$$

Knowing I_T and choosing a convenient bias potential permits calculation of R_T. In using these equations, first select a transistor type. Assume the maximum possible supply voltage and collector current consistent with the rating of the transistor and the maximum anticipated ambient temperature. This will ensure optimization of N and M. From the transistor specifications, values of I_{COM}, V_{BE}, V_{CEN}, and I_B (min) can be calculated. I_B (min) is the minimum base current required to cause saturation. R_C is calculated from the assumed collector current. In equation (7a) solve for I_K using the desired value of N and an arbitrary value for R_K. Substitute the value for I_K in equation (7b) along with a chosen value for M and solve for I_B. While superficially I_B need only be large enough to bring the transistor into saturation, increasing I_B will improve the rise time.

Circuit speed can be enhanced by using a diode as shown in Figure 7.8(A) to prevent severe saturation. Excess base current is diverted by the diode into the transistor collector. By controlling the maximum base current the diode clamps the collector close to saturation. The voltage across R_B raises the effective clamping voltage. Since R_B carries I_T plus the base current required to barely saturate the transistor, the voltage

CLAMPING DIODE REDUCES STORAGE TIME TO INCREASE SPEED
(A)

CAPACITORS REDUCE STORAGE TIME TO INCREASE SPEED
(B)

METHODS TO INCREASE CIRCUIT SPEED
Figure 7.8

across R_B will vary with transistor beta. Best results are obtained with narrow beta range transistors and I_T large compared to the base current.

If a silicon transistor is used, a germanium diode will generally clamp well enough with $R_B = 0$. Since the diode carries only excess base current its recovery time is generally short compared to the transistor's storage time.

The speed-up capacitor in Figure 7.8(B) helps clean out stored base charge. The capacitors may cause malfunction unless the stored charge during saturation is carefully controlled. The capacitors permit high frequency input transients to appear at the base of the transistor. If the transistor's stored charge is too small, the transients will generate a spurious output. If the stored charge is too large the capacitors cannot sweep it all out with resulting slower speed. In general, it is impractical to exceed two inputs to a common base. The capacitors also aggravate crosstalk between collectors. For this reason it is preferable to use higher frequency transistors without capacitors when additional speed is required.

Table 7.1 lists the characteristics of common logic systems employing transistors.

DIGITAL CIRCUITRY 7

NAME	TYPICAL CIRCUIT (Positive signals are defined as 1)	DESCRIPTION	FEATURES	SUITABLE TRANSISTORS: GERMANIUM Low Speed ($f\alpha < 15$ mcs.)	GERMANIUM High Speed ($f\alpha > 15$ mcs.)	SILICON Low Speed ($f\alpha < 15$ mcs.)	SILICON High Speed ($f\alpha > 15$ mcs.)	SUITABLE DIODES: SILICON High Speed
RTL Resistor transistor logic (NOR)	inputs a, b, c; R_B; output $\overline{a+b+c}$	Logic is performed by resistors. Any positive input produces an inverted output irrespective of the other inputs. Resistor R_B gives temperature stability. (See Fig. 7.7)	The circuit design is straightforward. All logical operations can be performed with only this circuit. Many transistors readily meet the steady state requirements.	2N78* 2N167* 2N169A 2N396A* 2N525 2N526* 2N1305* 2N1924		2N335* 2N656A*	2N706* 2N708 2N914 2N1613* 2N2193	
RCTL Resistor capacitor transistor logic	inputs a, b; R_B; output $\overline{a+b}$	Same as RTL except that capacitors are used to enhance switching speed. The capacitors increase the base current for fast collector current turn on and minimize storage time by supplying a charge equal to the stored base charge.	Faster than RTL at the expense of additional components and stringent stored charge requirements.	2N396A* 2N404			2N1613* 2N2193	
DCTL Direct coupled transistor logic	inputs a, b; outputs $\overline{ab}$, $\overline{a+b}$	Logic is performed by transistors. V_{CE} and V_{BE}, measured with the transistor in saturation, define the two logic levels. V_{CE} must be much less than V_{BE} to ensure stability and circuit flexibility. (See Fig 7.4)	Very low supply voltages may be used to achieve high power efficiency and miniaturization. Relatively fast switching speeds are practical.				2N708 2N914	
DL Diode logic	inputs a, b, c; outputs a+b+c, abc	Logic is performed by diodes. The output is not inverted. Amplifiers are required to maintain the correct logic levels through several gates in series.	Several gates may be used between amplifiers. High speeds can be attained. Non-inversion simplifies circuit design problems. Relatively inexpensive components are used.	2N78* 2N167* 2N396A* 2N526*		2N333* 2N337* 2N656A*	2N706* 2N708 2N914 2N1613* 2N2193	DHD 1N4150 1N4151 1N4152 1N4153 DO-7 1N3604 1N3605 1N3606
LLL Low level logic	inputs a, b, c; D; R; R_B; output $\overline{a+b+c}$	Logic is performed by diodes. The output is inverted. The diode D isolates the transistor from the gate permitting R to turn on the collector current. By proper choice of voltage changes occur. This method is also called current switching diode logic.	The number of inputs to the diode gate does not affect the transistor base current thus giving predictable performance. The small voltage excursions minimize the effects of stray capacitance and enhance switching speed.	2N396A* 2N525 2N526* 2N1305*		2N335* 2N338*	2N914 2N1711* 2N2192	

COMMON LOGIC SYSTEMS

Table 7.1

NAME	TYPICAL CIRCUIT (Positive signals are defined as 1)	DESCRIPTION	FEATURES	SUITABLE TRANSISTORS				SUITABLE DIODES
				GERMANIUM		SILICON		SILICON
				Low Speed ($f_\alpha < 15$ mcs.)	High Speed ($f_\alpha > 15$ mcs.)	Low Speed ($f_\alpha < 15$ mcs.)	High Speed ($f_\alpha > 15$ mcs.)	High Speed
CML Current mode logic		Logic is performed by transistors which are biased from constant current sources to keep them far out of saturation. Both inverted and non-inverted outputs are available.	Very high switching speeds are possible because the transistors are operated at optimum operating conditions. Although the voltage excursion is small the circuitry is relatively unaffected by noise.			2N337* 2N338*	2N708 2N914	
DTL Diode transistor logic		Logic is performed by diodes. The output is inverted. The transistor acts as an amplifier. This is essentially an extension of the diode logic discussed above.	High speeds can be attained. The impedance and voltage levels from stage to stage are well defined.	2N78* 2N167* 2N396A* 2N526* 2N1305*		2N333* 2N337*	2N706* 2N708 2N914 2N1613*	DHD 1N4150 1N4151 1N4152 1N4153
CDL Core diode logic		Logic is performed by cores and transmitted by diodes. Transistors act as drivers to shift information. Each transistor can drive many cores but not successive cores in the logic line.	These core modules can be made very small. Speed is limited by core switching speeds.				2N697* 2N1613* 2N1893 2N2193 2N2243	DO-7 1N3604* 1N3605 1N3606
				SUITABLE DEVICES				
4 Layer Device logic		Logic is performed by silicon controlled switches which are triggered on at the gate lead. The gates can be actuated by pulse or DC levels. The gates have a built in memory and must be reset.	These gates are pulse or dc actuated and the input need not be maintained. High output power capability is available. In general, in the presence of radiation, units will turn on permitting fail-safe design in this atmosphere.	3N58 3N59 3N81 3N82 } Silicon Controlled Switches				
TDL Tunnel diode logic		Logic is performed by tunnel diode switching from low voltage to high voltage state. Whether circuit represents AND or OR gate depends on bias current through resistor R. Tunnel diode biased near peak current for OR gate, and close to ground for AND.	Current flowing through input resistors determines logic. Circuit is basically simple and very high speed is obtainable.	1N3713 1N3715 1N3717 TD-401 } Germanium Tunnel Diodes				

NOTE: Other peak current diodes are listed in Chapter 19.

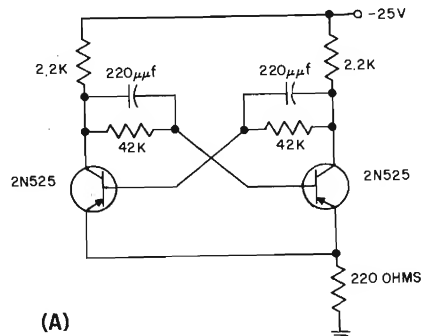
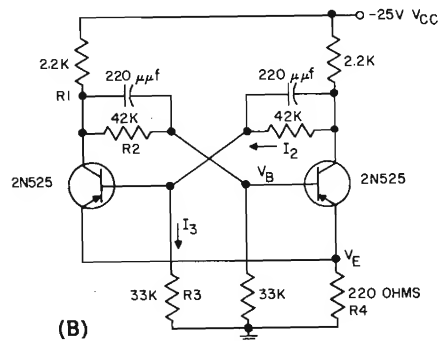
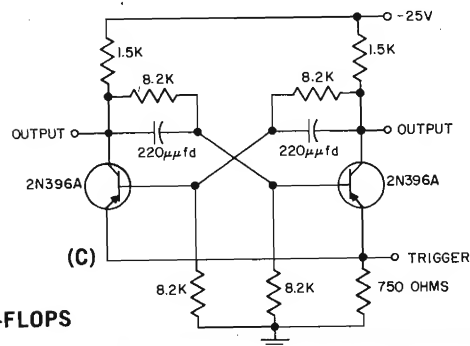
*Military types

COMMON LOGIC SYSTEMS

Table 7.1 (Continued)

FLIP-FLOP DESIGN PROCEDURES

SATURATED FLIP-FLOPS

For standard transistor types the flip-flop circuit in Figure 7.9(A) is preferable at moderate temperatures. We shall refer to the conducting and non-conducting transistors as the on and off transistors respectively. For stability, the circuit depends on the low collector to emitter voltage of the saturated on transistor to reduce the base current of the off transistor to a point where the circuit gain is too low for regeneration. The 220Ω emitter resistor can be removed if emitter triggering is not used. By adding

SATURATED FLIP-FLOPS
Figure 7.9

resistors from base to ground as in Figure 7.9(B), the off transistor has both junctions reverse biased for greater stability. While the 33K resistors divert some of the formerly available base current, operation no longer depends on a very low saturation voltage consequently less base current may be used. Adding the two resistors permits stable operation beyond 50°C ambient temperature.

The circuit in Figure 7.9(C) is stabilized to 100°C. The price that is paid for the stability is: smaller voltage change at the collector, more battery power consumed, more trigger power required, and a low I_{CO} transistor must be used. The capacitor values depend on the trigger characteristics and the maximum trigger repetition rate as well as on the flip-flop design.

By far, the fastest way to design saturating flip-flops is to define the collector and emitter resistors by the current and voltage levels generally specified as load requirements. Then assume a tentative cross-coupling network. With all components specified, it is easy to calculate the on base-current and the off base-voltage. For example, the circuit in Figure 7.9(B) can be analyzed as follows. Assume $V_{BE} = 0.3$ volt and $V_{CE} =$ 0.2 volt when the transistor is on. Also assume that $V_{EB} = 0.2$ volts will maintain the off transistor reliably cut-off. Transistor specifications are used to validate the assumptions.

1. Check for the maximum temperature of stability.

$$V_E = \frac{R4\,V_{CC}}{R1 + R4} = \frac{220}{2200 + 220}(25) = 2.3 \text{ volts}$$

$$V_{C\,on} = V_E + V_{CE\,on} = 2.3 + 0.2 = 2.5 \text{ volts}$$

Assuming no I_{CO}, the base of the off transistor can be considered connected to a potential,

$$V_B' = V_{C\,on}\frac{R3}{R2 + R3} \text{ through a resistor } R_B' = \frac{R2\,R3}{R2 + R3}$$

$$V_B' = \frac{(2.5)(33K)}{(42K + 33K)} = 1.1 \text{ volts}$$

$$R_B' = \frac{(33K)(42K)}{75K} = 18.5K$$

The I_{CO} of the off transistor will flow through R_B' reducing the base to emitter potential. If the I_{CO} is high enough, it can forward bias the emitter to base junction causing the off transistor to conduct. In our example, $V_E = 2.3$ volts and $V_{EB} = 0.2$ volts will maintain off conditions. Therefore, the base potential can rise from 1.1 volts to 2.1 volts (2.3 − 0.2) without circuit malfunction. This potential is developed across R_B' by $I_{CO} = \frac{2.1 - 1.1}{18.5K} = 54\ \mu a$. A germanium transistor with $I_{CO} = 10\ \mu a$ at 25°C will not exceed 54 μa at 50°C. If a higher operating temperature is required, R2 and R3 may be decreased and/or R4 may be increased.

2. Check for sufficient base current to saturate the on transistor.

$$V_{B\,on} = V_E + V_{BE\,on} = 2.3 + 0.3 = 2.6 \text{ volts}$$

The current through R3 $= I_3 = \frac{2.6v}{33K} = .079$ ma

The current through R1 and R2 in series is $I_2 = \frac{V_{CC} - V_{B\,on}}{R1 + R2} = \frac{25 - 2.6}{42K + 2.2K}$ $= 0.506$ ma

The available base current is $I_B = I_2 - I_3 = 0.43$ ma

The collector current is $I_C = \frac{V_{CC} - V_{C\,on}}{R1} = \frac{25 - 2.5}{2.2K} = 10.25$ ma

The transistor will be in saturation if h_{FE} at 10 ma is greater than

$$\frac{I_C}{I_B} = \frac{10.25}{0.43} = 24$$

If this circuit were required to operate to −55°C, allowance must be made for the reduction of h_{FE} at low temperatures. The minimum allowable room temperature h_{FE} should be 50% higher or $h_{FE\ min} = 36$.

Generally it is not necessary to include the effect of I_{CO} flowing through R1 when calculating I_2 since at temperatures where I_{CO} subtracts from the base drive it simultaneously increases h_{FE}. If more base drive is required, R2 and R3 may be decreased. If their ratio is kept constant, the off condition will not deteriorate, and so need not be rechecked.

3. Check transistor dissipation to determine the maximum junction temperature. The dissipation in the on transistor is

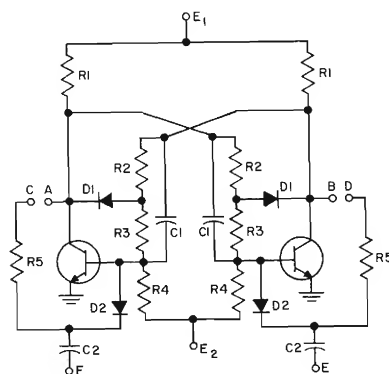
$$V_{BE\ on}\, I_B + V_{CE\ on}\, I_C = \frac{(0.3)\ (0.43)}{1000} + \frac{(0.2)\ (10.25)}{1000} = 2.18 \text{ mw}$$

The dissipation in the off transistor resulting from the maximum I_{CO} is

$$V_{CB}\, I_{CO} \cong \frac{(25)\ (55)}{10^6} = 1.4 \text{ mw}$$

Generally the dissipation during the switching transient can be ignored at speeds justifying saturated circuitry. In both transistors the junction temperature is within 1°C of the ambient temperature if transistors in the 2N394-97 or 2N524-27 series are used.

NON-SATURATED FLIP-FLOP DESIGN

The abundance of techniques to prevent saturation makes a general design procedure impractical if not impossible. While it is a simple matter to design a flip-flop as shown above, it becomes quite tedious to check all the worst possible combinations of component change to ensure manufacturability and long term reliability. Often the job is assigned to a computer which calculates the optimum component values and tolerances. While a number of flip-flop design procedures have been published, they generally make simplifying assumptions concerning leakage currents and the voltages developed across the conducting transistors.

CIRCUIT CONFIGURATION FOR NON-SATURATING FLIP-FLOP DESIGN PROCEDURE

Characteristics:

- Trigger input at points E
- Trigger steering by D2 and R5
- Collector clamping by D1 and R3
- Connect points A, B, C, D, E as shown in Figure 7.11 to get counter or shift register operation
- C1 and C2 chosen on basis of speed requirements

Figure 7.10 (A)

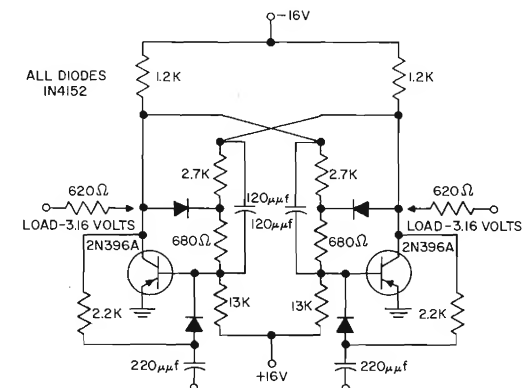
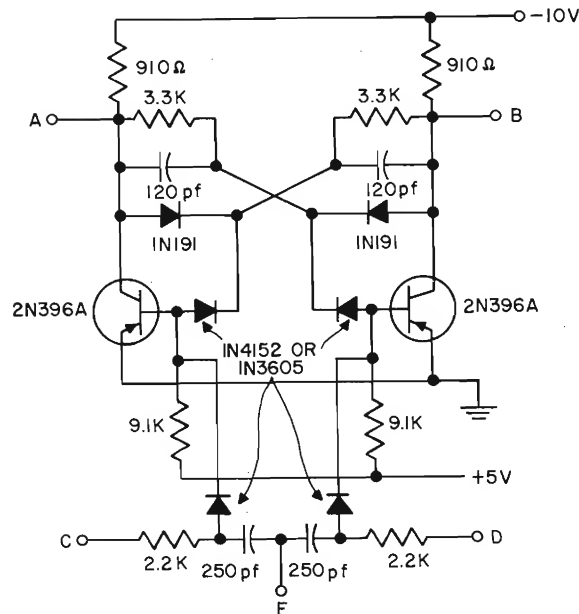
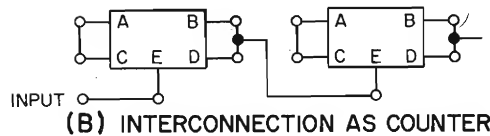
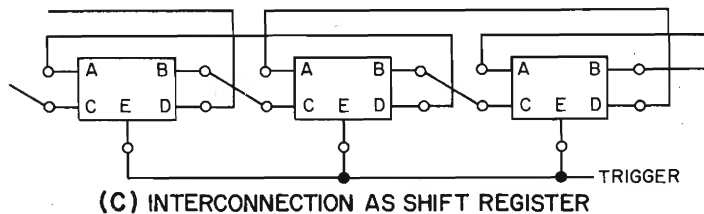
The design procedure described here is for the configuration in Figure 7.10(A). No simplifying assumptions are made but all the leakage currents and all the potentials are considered. The design makes full allowance for component tolerances, voltage fluctuations, and collector output loading. The anti-saturation scheme using one resistor (R3) and one diode (D1) was chosen because of its effectiveness, low cost and simplicity. The trigger gating resistors (R5) may be returned to different collectors to get different circuit functions as shown in Figure 7.11. This method of triggering offers the trigger sensitivity of base triggering and the wide range of trigger amplitude permissible in collector triggering. The derivation of the design procedure would require much space, therefore for conciseness, the procedure is shown without any substantiation. The procedure involves defining the circuit requirements explicitly then determining the transistor and diode characteristics at the anticipated operating points. A few astute guesses of key parameters yield a fast solution. However, since the procedure deals with only one section of the circuit at a time, a solution is readily reached by cut and try methods without recourse to good fortune. A checking procedure permits verification of the calculations. The symbols used refer to Figure 7.11(A) or in some cases are used only to simplify calculations. A bar over a symbol denotes its maximum value; a bar under it, its minimum. The example is based on polarities associated with NPN transistors for clarity. The result is that only E_2 is negative. While the procedure is lengthly, its straightforward steps lend themselves to computation by technically unskilled personnel and the freedom from restricting assumptions guarantees a working circuit when a solution is reached. A circuit designed by this procedure is shown in Figure 7.11(B).

NON-SATURATED FLIP-FLOP

Figure 7.10 (B)

The same procedure can be used to analyze existing flip-flops of this configuration by using the design check steps.

(A) FLIP-FLOP

(B) INTERCONNECTION AS COUNTER

(C) INTERCONNECTION AS SHIFT REGISTER

500 KC COUNTER-SHIFT REGISTER FLIP-FLOP
Figure 7.11

NON-SATURATING FLIP-FLOP DESIGN PROCEDURE

STEP	DEFINITION OF OPERATION	SYMBOL	SAMPLE DESIGN FOR 2N396 TRANSISTOR
(A)	*Circuit Requirements and Device Characteristics*		
1	Assume maximum voltage design tolerance	Δe	Let $\Delta e = \pm 5\%$
2	Assume maximum resistor design tolerance	Δr	Let $\Delta r = \pm 7\%$ (assuming $\pm$ 5% resistors)
3	Assume maximum ambient temperature	T_A	Let $T_A = 40°C$
4	Assume maximum load current out of the off side	I_O	Let $I_O = 1$ ma
5	Assume maximum load current into the on side	I_i	Let $I_i = 0.2$ ma
6	Estimate the maximum required collector current in the on transistor	I_1	Let $I_1 \leq 17.5$ ma
7	Assume maximum design I_{CO} at 25°C		From spec sheet $I_{CO} < 6\ \mu a$
8	Estimate the maximum junction temperature	T_J	Let $T_J = 60°C$
9	Calculate I_{CO} at T_J assuming I_{CO} doubles every 10°C or $I_{COT_J} = I_{CO25}\, e^{.07(T_J-25)}$	I_2	$I_2 = 6e^{.07T_J} = 71\ \mu a$; Let $I_2 = 100\ \mu a$
10	Assume the maximum base leakage current is equal to the maximum I_{CO}	I_3	Let $I_3 = 100\ \mu a$
11	Calculate the allowable transistor dissipation		2N396 is derated at 3.3 mw/°C. The junction temperature rise is estimated at 20°C therefore 67 mw can be allowed. Let $P_C = 67$ mw
12	Estimate h_{FE} minimum taking into account low temperature degradation and specific assumed operating point	β_{min}	Let $\alpha_{min} = 0.94$ or $\beta_{min} = 15.67$
13	Estimate the maximum design base to emitter voltage of the "on" transistor	V_1	Let $V_1 = 0.35$ volts
14	Assume voltage logic levels for the outputs		Let the level separation be $\geq$ 7 volts

NON-SATURATING FLIP-FLOP DESIGN PROCEDURE (CONTINUED)

STEP	DEFINITION OF OPERATION	SYMBOL	SAMPLE DESIGN FOR 2N396 TRANSISTOR
15	Choose the maximum collector voltage permissible for the "on" transistor	V_2	Let $V_2 \leq 2.0$ volts
16	Choose suitable diode types		Let all diodes be 1N4152
17	Estimate the maximum leakage current of any diode	I_4	Maximum leakage estimated as $\leq 0.25\ \mu a$. Let $I_4 = 40\ \mu a$ at end of life
18	Calculate $I_5 = I_3 + I_4$	I_5	$40 + 100 = 140\ \mu a$
19a	Choose the minimum collector voltage for the "off" transistor keeping in mind 14 and 15 above	V_3	Let $V_3 \geq 9.0$ volts
19b	Choose the maximum collector voltage for the "off" transistor	V_4	Let $V_4 \leq 13.0$ volts
20	Choose the minimum design base to emitter reverse bias to assure off conditions	V_5	Let $V_5 = 0.5$ volt
21a	Estimate the maximum forward voltage across the diodes	V_6	Let $V_6 = 0.8$ volt
21b	Estimate the minimum forward voltage	V_7	Let $V_7 = 0.2$ volt
22	Estimate the worst saturation conditions that can be tolerated.		
22a	Estimate the minimum collector voltage that can be tolerated	V_8	Let $V_8 = 0.1$ volt
22b	Estimate the maximum base to collector forward bias voltage that can be tolerated	V_9	Let $V_9 = 0.1$ volt
23a	Calculate $V_2 + V_7$	V_{10}	$2 + 0.2 = 2.2$ volts
23b	Calculate $V_2 + V_6$	V_{11}	$2 + 0.8 = 2.8$ volts
24a	Calculate $V_8 + V_7$	V_{12}	$0.1 + 0.2 = 0.3$ volt

STEP	DEFINITION OF OPERATION	SYMBOL	SAMPLE DESIGN FOR 2N396 TRANSISTOR
24b	Calculate $V_8 + V_6$	V_{13}	$0.1 + 0.8 = 0.9$ volt
25	Calculate $V_8 + V_9$	V_{14}	$0.1 + 0.1 = 0.2$ volt
(B)	*Cut and Try Circuit Design*		
1	Assume E_2	E_2	Let $E_2 = -16$ volts $\pm 5\%$; $\overline{E_2} = -15.2$ v; $\underline{E_2} = -16.8$ v
2a	Calculate $\frac{(1 + \Delta r)}{(1 - \Delta r)}$	K_1	$\frac{1.07}{0.93} = 1.15$
2b	Calculate $\frac{(1 + \Delta e)}{(1 - \Delta e)}$	K_2	$\frac{1.05}{0.95} = 1.105$
2c	Calculate $\frac{I_1}{\beta_{min}}$	K_3	$\frac{17.5}{15.67} = 1.117$ ma
2d	Calculate $I_2 + I_0 + 2I_4$	K_4	$0.1 + 1.0 + 0.08 = 1.18$ ma
2e	Calculate $\frac{V_6 - V_9}{V_8 + V_9 - \underline{E_2}}$	K_5	$\frac{0.8 - 0.1}{0.1 + 0.1 + 15.2} = 0.0454$ volts
3	Calculate $\overline{R4} \leq \frac{1}{K_3}\left[\frac{V_{10} - V_1}{K_1K_5} - K_1(V_1 - \underline{E_2})\right]$		$\frac{1}{1.117}\left[\frac{2.2 - 0.35}{(1.15)(0.0454)} - 1.15(0.35 + 16.8)\right] = 14.03$ K
4	Choose R4	R4	Let R4 = 13 K $\pm$ 7%; $\overline{R4} = 13.91$ K; $\underline{R4} = 12.09$ K
5	Calculate $\underline{R3} \geq K_5 \overline{R4}$		$(0.0454)(13.91K) = 0.632$ K
6	Choose R3	R3	Let R3 = 0.68 K $\pm$ 7%; $\overline{R3} = 0.7276$ K; $\underline{R3} = 0.6324$ K
7	Check R3 by calculating $\overline{R3} \leq \frac{\underline{R4}(V_{10} - V_1)}{V_1 - \underline{E_2} + K_3\underline{R4}}$		$\frac{(12.09\text{ K})(2.2 - 0.35)}{0.35 + 16.8 + (1.117)(12.09)} = 0.730$ K; choice of R3 satisfactory
8	Calculate $\frac{\overline{R4}}{-V_5 - \overline{E_2} - I_5\overline{R4}}$	K_6	$\frac{13.91\text{ K}}{-0.5 + 15.2 - (0.14)(13.91)} = 1.091$ K/V

NON-SATURATING FLIP-FLOP DESIGN PROCEDURE (CONTINUED)

STEP	DEFINITION OF OPERATION	SYMBOL	SAMPLE DESIGN FOR 2N396 TRANSISTOR
9	Calculate $\underline{R2} \geq \frac{K_6 (V_2 + V_5) - \underline{R3}}{1 - K_6 I_4}$		$\frac{(1.091)(2.0 + 0.5)\text{ K} - 0.632\text{ K}}{1 - (1.091)(0.04)} = 2.19\text{ K}$
10	Choose R2 – *If there are difficulties at this point, assume a different E_2.*	R2	Let R2 = 2.7 K ± 7%; $\overline{R2}$ = 2.889 K; $\underline{R2}$ = 2.511 K
11	Calculate $\frac{K_1^2 [V_3 - V_{12} + K_4 \underline{R2}]}{V_4 - V_{11}}$	K_7	$\frac{(1.15)^2[9.0 - 0.3 + (1.18)(2.511)]}{13.0 - 2.8} = 1.51$
12	Calculate $\overline{E_1} \leq \frac{K_7 V_4 - V_3}{K_7 - 1/K_2}$		$\frac{(1.51)(13.0) - 9.0}{1.51 - 1/1.105} = 17.63$
13	Choose E_1	E_1	Let E_1 = 16 volts ± 5%; $\overline{E_1}$ = 16.8 volts; $\underline{E_1}$ = 15.2 volts
14	Calculate $\overline{R1} \leq \frac{(\underline{E_1} - V_3)\underline{R2}}{V_3 - V_{12} + K_4 \underline{R2}}$		$\frac{(15.2 - 9.0)(2.511)}{9.0 - 0.3 + (1.18)(2.511)} = 1.335\text{ K}$
15	Calculate $\underline{R1} \geq \frac{(\overline{E_1} - V_4)(\overline{R2})}{V_4 - V_{11}}$		$\frac{(16.8 - 13.0)(2.889)}{13.0 - 2.8} = 1.077\text{ K}$
16	Choose R1	R1	Let R1 = 1.2 K ± 7%; $\overline{R1}$ = 1.284 K; $\underline{R1}$ = 1.116 K

(C) *Design Checks*

STEP	DEFINITION OF OPERATION	SYMBOL	SAMPLE DESIGN FOR 2N396 TRANSISTOR
1	Check "off" stability. Reverse bias voltage is given by: $V_{EB} \leq \overline{E_2} + \frac{\overline{R4}}{\overline{R4} + \underline{R3} + \underline{R2}} [V_2 - \overline{E_2} + I_4 \underline{R2} + I_5(\underline{R2} + \underline{R3})] V_{EB}$ Circuit stable if $V_{EB} \leq -V_5$	V_{EB}	$-15.2 + \frac{13.91}{17.05}$ $[2 + 15.2 + (0.04)(2.511) + (0.14)(3.14)] = -0.7$ volts The design value of V_5 was 0.5 volts. Therefore, the "off" condition is stable.

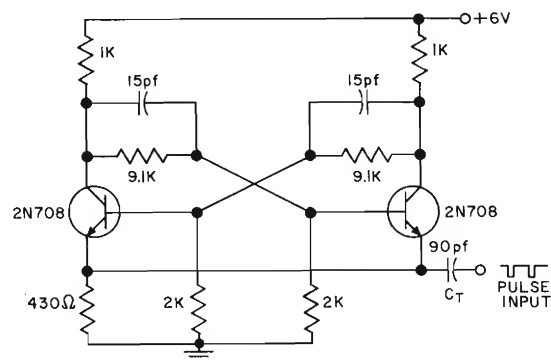
STEP	DEFINITION OF OPERATION	SYMBOL	SAMPLE DESIGN FOR 2N396 TRANSISTOR
2	Check for non-saturation under the worst conditions. $V_{BE} \leq \overline{E_2} + \frac{\overline{R4}(V_{13} - \overline{E_2})}{\overline{R4} + \underline{R3}}$ Circuit non-saturated if $V_{BE} \leq V_{14}$	V_{BE}	$-15.2 + \frac{13.91(0.9 + 15.2)}{14.54} = 0.19$ volts The design maximum of V_{14} was 0.2 volts.
3 3a	Check for stability. Calculate: $R_A = \overline{R1} + \overline{R2}$	R_A	1.284 + 2.889 = 4.173 K
3b	$R_B = \overline{R1} + \overline{R2} + \overline{R3} + \underline{R4}$	R_B	1.284 + 2.889 + 0.728 + 12.09 = 16.99 K
3c	$R_C = \overline{R3} + \underline{R4}$	R_C	0.728 + 12.09 = 12.82 K
3d	$E_1' = \underline{E_1} - K_4 \overline{R1}$	E_1'	15.2 – (1.18) (1.284) = 13.68 volts
3e	$R_D = \underline{R1} + \overline{R2} + \overline{R3} + \overline{R4}$	R_D	1.116 + 2.889 + 0.728 + 13.91 = 18.643 K
3f	$I_6 = \frac{R_D(\overline{E_1} - V_2) - \underline{R1}\,[\overline{E_1} - \underline{E_2} - I_5 \overline{R4} - I_4(\overline{R3} + \overline{R4})]}{\underline{R1}(R_D - \underline{R1})}$	I_6	$\frac{18.64(16.8 - 2) - 1.116\,[16.8 + 16.8 - (0.14)(13.91) - (.04)(0.728 + 13.91)]}{1.116(18.64 - 1.116)} = 12.34$ ma
3g	$I_7 = \frac{R_B}{R_A R_C}(E_1' - V_{10}) - \frac{1}{R_C}(E_1' - \underline{E_2})$	I_7	$\frac{16.99}{(4.173)(12.82)}(13.68 - 2.2) - \frac{(13.68 + 16.8)}{12.82} = 1.266$ ma
3h	$I_8 = \frac{I_1 + I_6 + I_7}{\beta_{min} + \underline{R4}/R_C}$	I_8	$\frac{0.2 + 12.34 + 1.266}{15.67 + 12.09/12.82} = 0.831$ ma
3i	$V_{BE}' = \underline{E_2} + \frac{\underline{R4}}{R_B}\left(1 + \frac{R_A}{R_C}\right)\left(E_1' - \underline{E_2}\right)$ $- \frac{\underline{R4}}{R_C}\left(E_1' - V_{10}\right) - I_8 \frac{\underline{R4}}{R_B}\left(\frac{R_A \underline{R4}}{R_C} - R_A - \overline{R3}\right)$	V_{BE}'	$-16.8 + \frac{12.09}{16.99}\left(1 + \frac{4.173}{12.818}\right)\left(13.683 + 16.8\right)$ $- \frac{12.09}{12.818}\left(13.683 - 2.2\right) - 0.831\frac{12.09}{16.99}$ $\left(\frac{(4.173)(12.09)}{12.818} - 4.173 - 0.7276\right) = 0.55\text{V}$ 0.55V is greater than V_1 = 0.35V, therefore the design is satisfactory.

TRIGGERING

Flip-flops are the basic building blocks for many computer and switching circuit applications. In all cases it is necessary to be able to trigger one side or the other into conduction. For counter applications, it is necessary to have pulses at a single input make the two sides of the flip-flop conduct alternately. Outputs from the flip-flop must have characteristics suitable for triggering other similar flip-flops. When the counting period is finished, it is generally necessary to reset the counter by a trigger pulse to one side of all flip-flops simultaneously. Shift registers and ring counters have similar triggering requirements.

In applying a trigger to one side of a flip-flop, it is preferable to have the trigger turn a transistor off rather than on. The off transistor usually has a reverse-biased emitter junction. This bias potential must be overcome by the trigger before switching can start. Furthermore, some transistors have slow turn on characteristics resulting in a delay between the application of the trigger pulse and the actual switching. On the other hand, since no bias has to be overcome, there is less delay in turning off a transistor. As turn-off begins, the flip-flop itself turns the other side on.

A lower limit on trigger power requirements can be determined by calculating the base charge required to maintain the collector current in the on transistor. The trigger source must be capable of neutralizing this charge in order to turn off the transistor. It has been determined that the base charge for a non-saturated transistor is approximately $Q_B = 1.22\ I_C/2\pi f_\alpha$ using the equivalent circuit approach, or $\tau_c\ I_C$ using charge parameters. The turn-off time constant is approximately $h_{FE}/2\pi f_\alpha$ or τ_α. This indicates that circuits utilizing high speed transistors at low collector currents will require the least trigger power. Consequently, it may be advantageous to use high speed transistors in slow circuitry if trigger power is critical. If the on transistor was in saturation, the trigger power must also include the stored charge. The stored charge is given approximately by $Q_s = \tau_b\ I_{BX}$, where the symbols are defined in the section on transient response time.

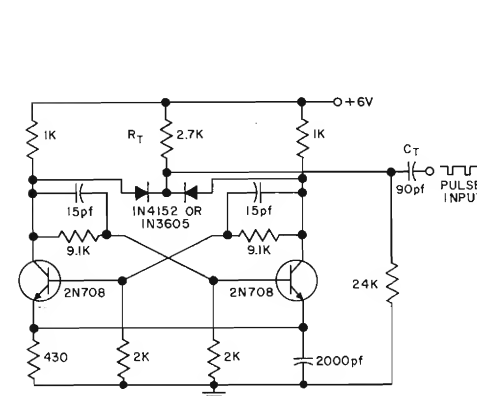
Generally, the trigger pulse is capacitively coupled. Small capacitors permit more frequent triggering but a lower limit of capacitance is imposed by base charge considerations. When a trigger voltage is applied, the resulting trigger current causes the charge on the capacitor to change. When the change is equal to the base charge just

MAXIMUM TRIGGER RATE EXCEEDS 2MC WITH TRIGGER AMPLITUDE FROM 4V TO 12V.

EMITTER TRIGGERING

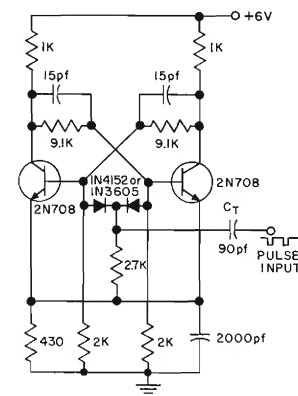
Figure 7.12

calculated, the transistor is turned off. If the trigger voltage or the capacitor are too small, the capacitor charge may be less than the base charge resulting in incomplete turn-off. In the limiting case $C = Q_B/V_T$. The speed with which the trigger turns off a transistor depends on the speed in which Q_B is delivered to the base. This is determined by the trigger source impedance and r_b'.

In designing counters, shift registers or ring counters, it is necessary to make alternate sides of a flip-flop conduct on alternate trigger pulses. There are so-called steering circuits which accomplish this. At low speeds, the trigger may be applied at the emitters as shown in Figure 7.12. It is important that the trigger pulse be shorter than the cross coupling time constant for reliable operation. The circuit features few parts and a low trigger voltage requirement. Its limitations lie in the high trigger current required.

At this point, the effect of trigger pulse repetition rate can be analyzed. In order that each trigger pulse produce reliable triggering, it must find the circuit in exactly the same state as the previous pulse found it. This means that all the capacitors in the circuit must stop charging before a trigger pulse is applied. If they do not, the result is equivalent to reducing the trigger pulse amplitude. The transistor being turned off presents a low impedance permitting the trigger capacitor to charge rapidly. The capacitor must then recover its initial charge through another impedance which is generally much higher. The recovery time constant can limit the maximum pulse rate.

MAXIMUM TRIGGER RATE EXCEEDS 5MC WITH TRIGGER AMPLITUDE FROM 4V TO 12V.

COLLECTOR TRIGGERING

Figure 7.13

MAXIMUM TRIGGER RATE EXCEEDS 5MC WITH TRIGGER AMPLITUDE FROM 0.75 TO 2 VOLTS.

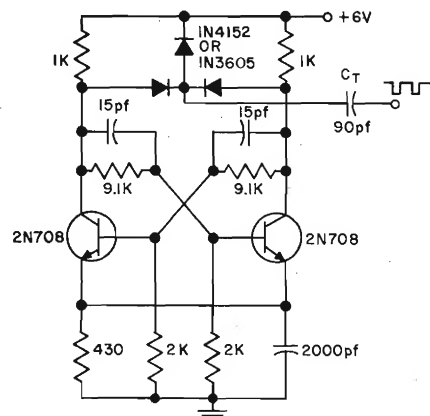
BASE TRIGGERING

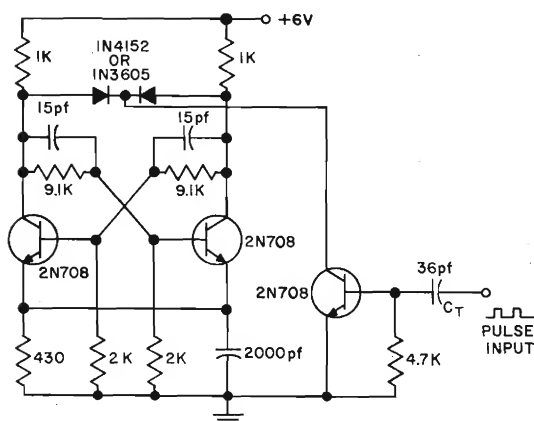
Figure 7.14

Steering circuits using diodes are shown in Figures 7.13 and 7.14. The collectors are triggered in 7.13 by applying a negative pulse. As a diode conducts during triggering, the trigger pulse is loaded by the collector load resistance. When triggering is accomplished, the capacitor recovers through the biasing resistor R_T. To minimize trigger loading, R_T should be large; to aid recovery, it should be small. To avoid the recovery problem mentioned above, R_T can be replaced by a diode as shown in 7.15. The diode's low forward impedance ensures fast recovery while its high back impedance avoids shunting the trigger pulse during the triggering period.

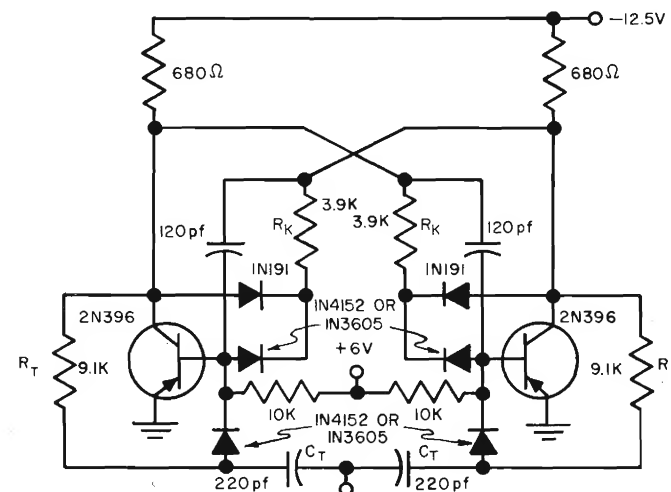
Collector triggering requires a relatively large amplitude low impedance pulse but has the advantage that the trigger pulse adds to the switching collector waveform to

enhance the speed. Large variations in trigger pulse amplitude are also permitted.

In designing a counter, it may be advantageous to design all stages identically the same to permit the economies of automatic assembly. Should it prove necessary to increase the speed of the early stages, this can be done by adding a trigger amplifier as shown in Figure 7.16 without any change to the basic stage.

DIODE TO SUPPLY VOLTAGE REDUCES TRIGGER POWER AND EXTENDS MAXIMUM TRIGGER RATE.

COLLECTOR TRIGGERING
Figure 7.15

FOR IMC TRIGGER RATE LESS THAN I VOLT TRIGGER AMPLITUDE REQUIRED.

COLLECTOR TRIGGERING WITH TRIGGER AMPLIFIER
Figure 7.16

Base triggering shown in Figure 7.14 produces steering in the same manner as collector triggering. The differences are quantitative with base triggering requiring less trigger energy but a more accurately controlled trigger amplitude. A diode can replace the bias resistor to shorten the recovery time.

BASE TRIGGERING WITH HYBRID GATE
Figure 7.17

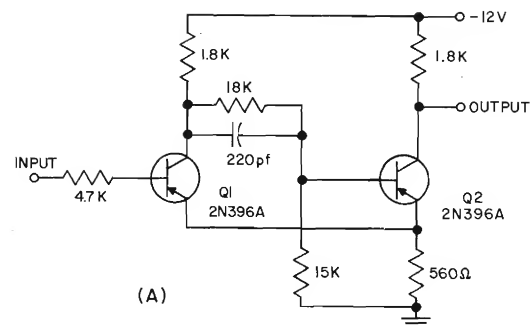
Hybrid triggering illustrated in Figure 7.17 combines the sensitivity of base triggering and the trigger amplitude variation of collector triggering. In all the other steering circuits the bias potential was fixed, in this one the bias potential varies in order to more effectively direct the trigger pulse. By returning the bias resistor to the collector the bias voltage is V_{CB}. For the conducting transistor, V_{CB} is much less than for the off transistor, consequently, the trigger pulse is directed to the conducting transistor. This steering scheme is particularly attractive if V_{CB} for the conducting transistor is very small as it is in certain non-saturating circuits such as shown in Figure 6.23.

Care should be taken that the time constant C_TR_T does not limit the maximum counting rate. Generally R_T can be made approximately equal to R_K, the cross-coupling resistor.

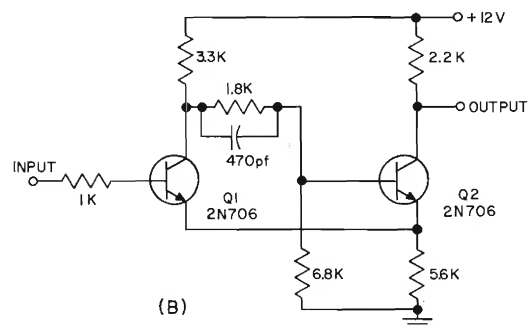
SPECIAL PURPOSE CIRCUITS

SCHMITT TRIGGER

A Schmitt trigger is a regenerative bistable circuit whose state depends on the amplitude of the input voltage. For this reason, it is useful for waveform restoration, signal level shifting, squaring sinusoidal or non-rectangular inputs, and for dc level detection. Practical circuits are shown in Figure 7.18.

Circuit operation is readily described using Figure 7.18(B). Assuming Q1 is non-conducting, the base of Q2 is biased at approximately +6.8 volts by the voltage divider consisting of resistors 3.3K, 1.8K and 6.8K. The emitters of both transistors are then at 6.6 volts due to the forward bias voltage required by Q2. If the input voltage

FREQUENCY RANGE 0-500KC
OUTPUT AT COLLECTOR HAS 8V MINIMUM LEVEL CHANGE
Q1 ALWAYS CONDUCTS IF INPUT IS MORE NEGATIVE THAN -5V
Q2 ALWAYS CONDUCTS IF INPUT IS MORE POSITIVE THAN -2V
AMBIENT TEMPERATURE -55°C TO 71°C

(A)

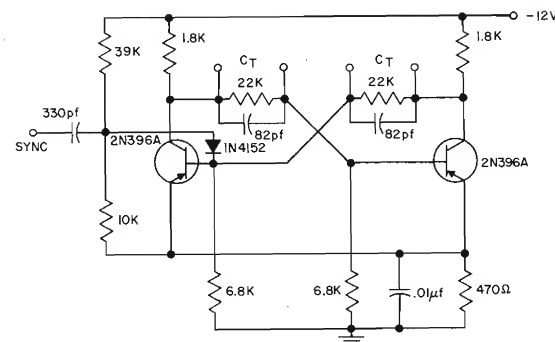
FREQUENCY RANGE 0 TO 1 MC
OUTPUT AT COLLECTOR HAS 2V MINIMUM LEVEL CHANGE
Q1 ALWAYS CONDUCTS IF INPUT EXCEEDS 6.8V
Q2 ALWAYS CONDUCTS IF INPUT IS BELOW 5.2V
AMBIENT TEMPERATURE 0°C TO 71°C

SCHMITT TRIGGERS
Figure 7.18

is less than 6.6 volts, Q1 is off as was assumed. As the input approaches 6.6 volts, a critical voltage is reached where Q1 begins to conduct and regeneratively turns off Q2. If the input voltage is now lowered below another critical value, Q2 will again conduct.

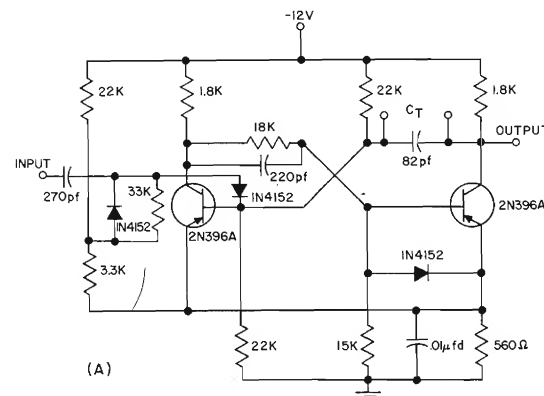
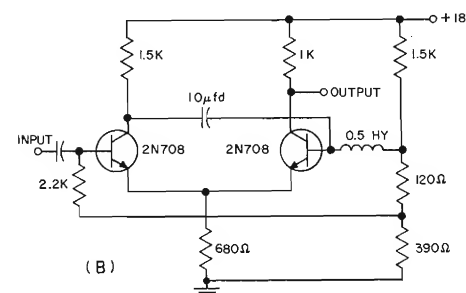
ASTABLE MULTIVIBRATOR

The term multivibrator refers to a two stage amplifier with positive feedback. Thus a flip-flop is a bistable multivibrator; a "one-shot" switching circuit is a monostable multivibrator and a free-running oscillator is an astable multivibrator. The astable multivibrator is used for generating square waves and timing frequencies and for frequency division. A practical circuit is shown in Figure 7.19. The circuit is symmetrical with the transistors dc biased so that both can conduct simultaneously. The cross-coupling capacitors prevent this, however, forcing the transistors to conduct alternately. The period is approximately $T = C_T + 100/28.8$ microseconds where C_T is measured in pf (μμf). A synchronizing pulse may be used to lock the multivibrator to an external oscillator's frequency or subharmonic.

MONOSTABLE MULTIVIBRATOR

On being triggered a monostable multivibrator switches to its unstable state where it remains for a predetermined time before returning to its original stable state. This makes the monostable multivibrator useful in standardizing pulses of random widths or in generating time delayed pulses. The circuit is similar to that of a flip-flop except that one cross-coupling network permits ac coupling only. Therefore, the flip-flop can

FREQUENCY RANGE 1 CPS TO 250KCPS BY CHANGING C_T
OUTPUT AT COLLECTOR HAS 8 VOLT MINIMUM LEVEL CHANGE
AMBIENT TEMPERATURE -55°C TO 71°C
SYNCHRONIZING PULSES PERMIT GENERATING SUBHARMONICS
SYNC PULSE AMPLITUDE MUST EXCEED 1.5V POSITIVE; RISETIME MUST BE LESS THAN 1.0μ SEC.

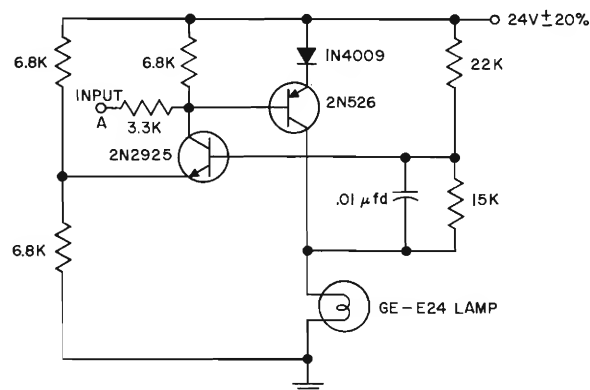
ASTABLE MULTIVIBRATOR
Figure 7.19

only remain in its unstable state until the circuit reactive components discharge. Two circuits are shown in Figure 7.20 to illustrate timing with a capacitor and with an inductor. The inductor gives much better pulse width stability at high temperatures.

OUTPUT AT COLLECTORS HAS 8 VOLT LEVEL CHANGE
OUTPUT PULSE DURATION 2μSEC TO 1 SEC
MAXIMUM INPUT FREQUENCY 250KC
MAXIMUM REQUIRED INPUT PULSE IS 5 VOLTS
DUTY CYCLE EXCEEDS 60%
AMBIENT TEMPERATURE -55°C TO 71°C

OUTPUT AT COLLECTOR HAS 5 VOLT LEVEL CHANGE
OUTPUT PULSE DURATION APPROX 600 MICROSECONDS
MAXIMUM INPUT PULSE REQUIRED 3 VOLTS
AMBIENT TEMPERATURE -55°C TO 71°C

MONOSTABLE MULTIVIBRATOR
Figure 7.20

INDICATOR LAMP DRIVER

The control panel of a computer frequently has indicator lamps to permit monitoring the computer's operation. The circuit in Figure 7.21 shows a bistable circuit which permits controlling the lamp by short trigger pulses.

A negative pulse at point A turns on the lamp, which remains on due to regenerative feedback in the circuit. A positive pulse at A will turn off the lamp. The use of complementary type transistors minimizes the standby power while the lamp is off.

NOTE:
1. TRIGGER PULSE REQUIREMENT 2 VOLTS NEGATIVE WITH RESPECT TO 24 V MAXIMUM.
2. AMBIENT TEMPERATURE -55°C TO 71°C.
3. RESISTOR TOLERANCE ± 10% AT END OF LIFE.

BISTABLE INDICATOR LAMP DRIVER

Figure 7.21

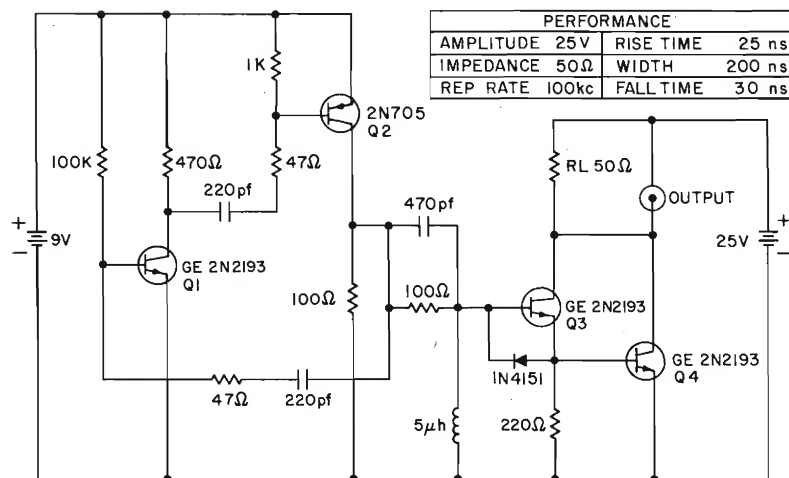
PERFORMANCE			
AMPLITUDE	25V	RISE TIME	25 ns
IMPEDANCE	50Ω	WIDTH	200 ns
REP RATE	100kc	FALL TIME	30 ns

PULSE GENERATOR WITH 0.5 AMPS. IN 25 NSEC.

Figure 7.22

PULSE GENERATOR

Frequently, in computer circuits a clock pulse is required to set the timing in an array of circuits. A pulse generator is shown in Figure 7.22 which delivers a very fast rise time (25 nsec.) pulse of high power. The circuit is basically composed of two parts. A multivibrator is formed by Q1 and Q2 and their associated circuitry and triggers the pulse generator formed by Q3 and Q4.

RING COUNTER

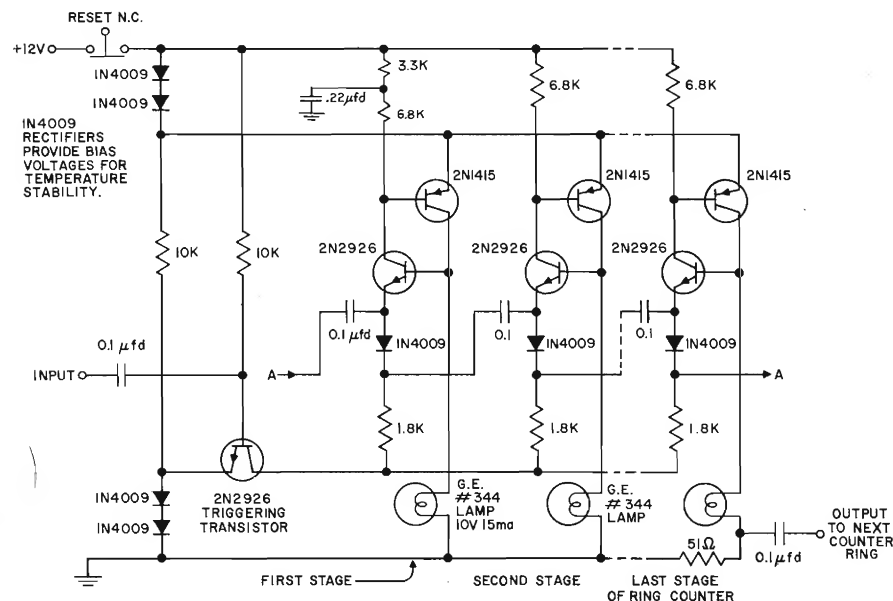
The circuit of Figure 7.23 forms a digital counter or shift register with visual readout. The circuit operates from a 12 volt source and uses six components per stage. The counter and indicator functions are combined to insure low battery drain. The .22 μfd capacitor ensures that the first stage turns on after the reset button is released. No current is drawn by the stages except when a lamp is on. As many stages as desired may be included in a ring.

RING COUNTER WITH VISUAL READOUT

Figure 7.23

DCTL

Some circuits have been designed making specific use of saturation. The direct coupled transistor logic (DCTL) flip-flop shown in Figure 7.24 utilizes saturation. In saturation $V_{CE(SAT)}$ can be so low that if this voltage is applied between the base and emitter of another transistor, as in this flip-flop, there is insufficient forward bias to cause this transistor to conduct appreciably. The extreme simplicity of the circuit is self evident and is responsible for its popularity. However, special requirements are placed on the transistors. The following are among the circuit characteristics:

First, the emitter junction is never reverse biased permitting excessive current to flow in the off transistor at temperatures above 40°C in germanium. In silicon, however, operation to 150°C has proved feasible.

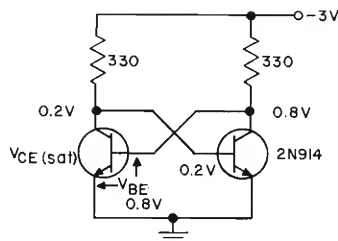
Second, saturation is responsible for a storage time delay slowing up circuit speed.

DIRECT COUPLED TRANSISTOR LOGIC (DCTL) FLIP-FLOP

Figure 7.24

In the section on transient response we see the importance of drawing current out of the base region to increase speed. In DCTL this current results from the difference between $V_{CE(SAT)}$ and V_{BE} of a conducting transistor. To increase the current, $V_{CE(SAT)}$ should be small and r_b' should be small. However, if one collector is to drive more than one base, r_b' should be relatively large to permit uniform current sharing between bases since large base current unbalance will cause large variations in transient response resulting in circuit design complexity. High base recombination rates and epitaxial collectors to minimize collector storage result in short storage times in spite of r_b'.

Third, since $V_{CE(SAT)}$ and V_{BE} differ by less than 0.3 volt in germanium, stray voltage signals of this amplitude can cause faulty performance. While stray signals can be minimized by careful circuit layout, this leads to equipment design complexity. Silicon transistors with a 0.6 volt difference between $V_{CE(SAT)}$ and V_{BE} are less prone to being turned on by stray voltages but are still susceptible to turn-off signals. This is somewhat compensated for in transistors with long storage time delay since they will remain on by virtue of the stored charge during short turn-off stray signals. This leads to conflicting transistor requirements — long storage time for freedom from noise, short storage time for circuit speed.

NOTES

OSCILLATORS

CHAPTER 8

OSCILLATOR THEORY

The study of oscillators forms one of the most interesting fields available to the electronic circuits designer. The anonymous wag quoted as saying "an oscillator amplifies and an amplifier oscillates" underlines the capricious nature of the amplifier which furnishes its own input signal from its own output signal. Vital and fundamental to all oscillators is an amplifier. The process of oscillation simply involves a connection of output to input so that certain conditions are fulfilled. These conditions are called *stability criteria*; and different types of oscillators are classed primarily by the means employed to obey the basic stability criteria.

Although one hears about transistor oscillators, or vacuum tube oscillators, or tunnel diode oscillators, etc., these various classes are as many as the active devices furnishing the gain necessary for oscillation, but do not really reveal much about the nature of the oscillator. Figure 8.1 shows an amplifier having a voltage gain A, whose output is connected to a second amplifier having a voltage gain B. Further, the input of amplifier A is connected to the output of B.

$$e_s = e_i \pm Be_o \tag{8a}$$

$$e_o = Ae_s \tag{8b}$$

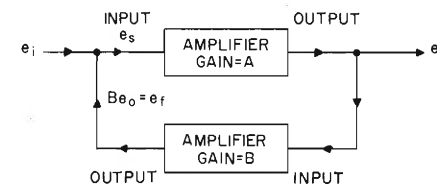
$$\frac{e_o}{e_i} = \frac{A}{1 \pm AB} \tag{8c}$$

STABILITY CRITERIA

Figure 8.1

Nothing is said about the amount of voltage, current or power gains of either amplifier (whether it is greater or lesser than unity), or how the outputs are added. Figure 8.1 writes three simple equations. Equation (8c) is called a *transfer function* and describes how the output voltage/input voltage ratio behaves in terms of the gains of the amplifiers. In an oscillator we might expect that a small input signal would be amplified regeneratively until infinite, or until some limit is imposed. This condition, from equation (8c) is possible if the product of AB = −1. This, in turn, would require us to choose the positive sign in equation (8a). Returning to the block diagram, this positive sign stipulates that $e_f = Be_o$ "add" to e_i or be in phase with e_i. The ratio of e_o/e_i need not be infinite for oscillation to occur, nor must the product of A and B exactly = 1. Exact specification, in general terms, of the conditions for oscillation is most simply stated as AB > 1. In some cases the gain considered in writing the transfer function is most conveniently expressed as power or current

gain. If power gain is considered, then the *loop gain* (net gain) must be greater than unity. This criteria is called the *Barkhausen criteria.*

Four other common approaches are used for analytical determination of the *stability* of the system. These approaches are, from direct examination of the system differential equation solutions: Routh's criterion, Nyquist's criterion, Bode's attenuation and phase shift method, or combinations of all. In nearly all oscillators the amplifier we have labeled A has a voltage gain and current gain greater than unity (in addition to a power gain greater than unity), and the amplifier labeled B has gain less than unity. An active device, such as a transistor, furnishes the gain; resistors, capacitors, and inductors provide the loss and phase shift to insure the proper polarity of output to input feedback.

PHASE SHIFT OSCILLATORS

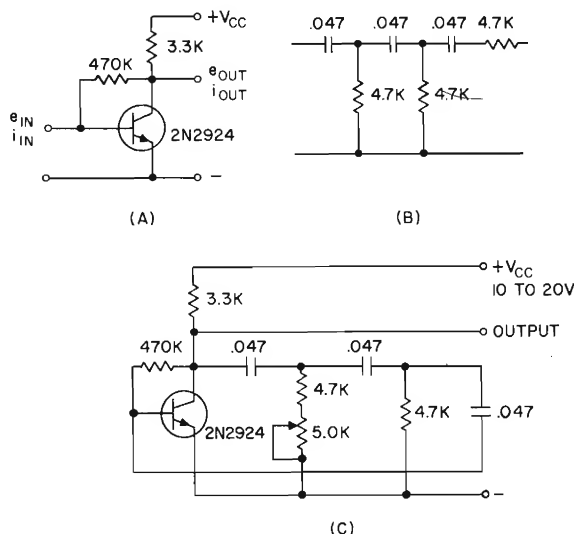
Figure 8.2(A) depicts a simple, versatile transistor amplifier. (Chapter 4, Figure 4.3 and accompanying text as well as Chapter 2 give detailed design of this type of amplifier.) Its current gain is stabilized against transistor variation. The means used to stabilize both operating point and small signal current gain also allow it to be used over a collector voltage range of 2 to 24 volts.

AMPLIFIER TO OSCILLATOR

Figure 8.2

When this simple amplifier is combined with the phase shift network in Figure 8.2(B) oscillation will occur at a frequency where there is a 360° total phase shift; 180° of this 360° total is furnished by the grounded emitter amplifier, and 180° is furnished by the high pass network. Figure 8.2(C) connects both together and provides a 5K pot for frequency adjust. This pot adjusts frequency from about 200 to 400 cps. Both h_{ie} and h_{ob} enter as terms in the expression for frequency, but the unusually low impedances chosen provide excellent temperature and voltage stability.

Output is derived across the collector and is approximately equal to V_{CC}. Frequency of oscillation is

$$f \cong \frac{1}{2\pi\sqrt{6R^2C^2 + 4RR_LC^2}} \qquad (8d)$$

(This equation assumes $R > 10\ h_{ie}$ and $1/h_{oe} > 10\ R_L$)

The h_{fe} for sustained oscillation is

$$h_{fe} \cong 22 + \frac{30R}{R_L} + \frac{4R_L}{R} \qquad (8e)$$

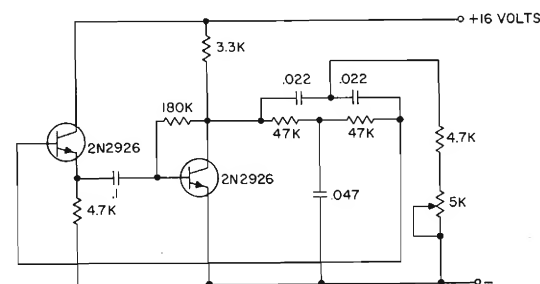
Figure 8.3 details yet another RC phase shift oscillator using a *bridged-T* network. In this case the simple amplifier is supplemented by an emitter follower to eliminate h_{ie} loading variations. Exceptional frequency stability (.2%) is possible over the temperature range of −55°C to +80°C. In both phase shift oscillators the affect of h_{oe} variations is swamped by the low (3.3K) collector load.

HIGH STABILITY BRIDGED-T OSCILLATOR

Figure 8.3

RESONANT FEEDBACK OSCILLATORS

Among the most prevalent, useful oscillators is a class termed *resonant-feedback* circuits. These use either inductance-capacitance combinations or their equivalent (electro-mechanical resonators). They are characterized by having circuit simplicity, good power efficiency, and good frequency stability. Figure 8.4(A) demonstrates how ac coupling between input and output of a transistor amplifier is accomplished. This circuit is classed as a *tuned collector oscillator*. L_1 and **C** in the collector of transistor Q, form a parallel resonant circuit. Further, the mutual coupling between L_1 and L_2 (called a tickler winding) provides an input signal current whose direction and magnitude are set by the physical arrangement of L_1 relative to L_2, and by the direction and magnitude of the current through L_1.

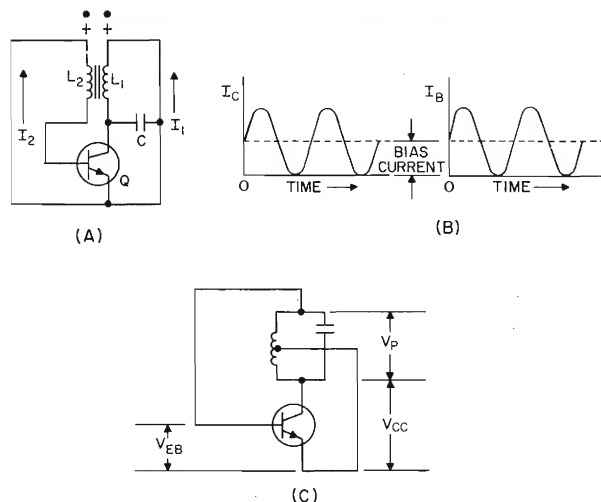
The dots shown on the coils indicate winding start and infer phase coincidence, so that an increase in collector current causes an increase in base current which provides the regenerative, or positive, feedback required to initiate oscillation. The core placed in the transformer is shown to indicate unity coupling between L_1 and L_2 which simplifies the analytical design procedure, but is not necessary for oscillator operation. The collector current and base current waveforms of Figure 8.4(B) both show an offset which comes about from a bias current not shown in this simple ac circuit. This offset, or bias, current insures that the oscillator will start. Reversal of the increasing, or decreasing, base current is limit cycle in nature and comes about because the current gain of a transistor falls at both very high and very low currents. The exact points in I_C where reversal occurs are determined by loop gain and loss, and will

RESONANT FEEDBACK OSCILLATOR

Figure 8.4

always lie between transistor cutoff and saturation. The period of oscillation is very nearly set by the familiar relation between L_2 and C

$$f_r = \frac{1}{2\pi\sqrt{L_2 C}} \quad (8f)$$

This presupposes that the core coupling L_1 and L_2 is operated over a reasonably linear portion of its B-H characteristic. A more nearly exact expression, including the mutual inductance M is

$$f_r = \frac{1}{2\pi\sqrt{C(L_2 + L_1 + 2M)} - (L_2 L_1 - M)^2 h_{ob}/h_{ib}} \quad (8g)$$

In Figure 8.4(C), the ac circuit, an auto transformer can be substituted for the two winding transformer, and the emitter rather than the base may be allowed to float. This preserves the proper feedback polarity, and is the basic circuit of the Hartley oscillator. Further, it is a grounded-base oscillator and stability criteria are appropriately expressed in terms of grounded base hybrid parameters. Analysis of this type of oscillator most frequently concerns itself with limit conditions. First, and fundamental, is the ability of the oscillator to start and continue oscillation. For this purpose small signal hybrid parameters may be used to establish the power gain of the circuit or the equivalent current or voltage gains. The Barkhausen criteria for loop unity gain forms the most convenient analytical approach. In terms of the mutual inductance M and the inductances $L_1 + L_2$ oscillation requires

$$h_{fb} \cong \frac{L_2 + M}{L_1 + M} \quad (8h)$$

In power applications, device ratings become important limit parameters to examine. The first point to consider is the power dissipation of the device compared to the power needed in an attached load. In most cases oscillator efficiency will be somewhat greater than the theoretical class "A" efficiency of 50%. This follows because of the bias needed to guarantee starting and proceeds from the stability criteria. A figure of 50% is pessimistic; it may later be refined by actual circuit

performance measurement. Supposing we desire to furnish 1 watt of power into a stipulated load; and further, that we may, by an additional winding or other means, provide a correct reflected load to the collector of the transistor related to the desired power output as follows

$$R_L = \frac{V_{CC}^2}{2 P_O} \quad (8i)$$

$$\frac{h}{100} = \frac{P_O}{P_I} = \frac{P_O}{P_O + P_D} \text{ (neglecting circuit loss)} \quad (8j)$$

R_L = required load
V_{CC} = collector supply voltage
P_O = output power
P_I = input power
P_D = power dissipated in the transistor
h = efficiency as a percent

In our example, at a worse case efficiency of 50%, $.5 = 1/1 + P_D$ where $P_D = 1 - .5 = .5$ watts.

A device must be chosen which has a half watt capability at the highest environmental temperature to be encountered. The 2N2192 series of silicon devices, described in Chapter 19, will provide ample margin up to their f_α at approximately 100 megacycles.

The next concern is that of collector voltage swing. Having selected a supply voltage, V_{CC}, the maximum swing will be determined by the value of the load resistor R_L. If $R_L = \infty$ then the worst case occurs and the oscillator tank voltage swing is the largest. The *peak* voltage appearing across the tank circuit is

$$V_P \cong \frac{V_{CC}}{R_L} Q\, \omega L \quad (8k)$$

$$Q = \frac{\omega L}{R_L} \text{ (assuming an unloaded } Q > 10) \quad (8l)$$

then

$$V_P \cong \frac{V_{CC}\, \omega^2 L^2}{R_L^2} \quad (8m)$$

the *peak* stress across the transistor then becomes

$$V_{CE} \cong V_{CC}\left(1 + \frac{\omega^2 L^2}{R_L^2}\right). \quad (8n)$$

The *peak* stress across the emitter base junction is related to V_{CE} through the transformer turns ratio. So,

$$V_{EB} = \frac{V_{CC}\, \omega^2 L^2 N}{R_L^2} \text{ where } N = \text{turns ratio} \quad (8o)$$

If the capacitor used to resonate the collector tuned circuit is split and used to form the feedback divider network a Colpitts oscillator results. A simplified ac circuit for this configuration is shown in Figure 8.5(A). Both C_T and C_2 together, set the effective capacity against which **L** resonates.

Figure 8.5(B) is identical to 8.5(A) except that the emitter rather than the base is shown at ground. At higher frequencies one may relate nearly any oscillator to the Hartley or Colpitts types even though part of the capacitive voltage divider is *hidden* as transistor capacity. In this figure, C_1, connected between collector and emitter of the transistor, is termed the *feedback capacity* often seen in high frequency grounded base oscillators.

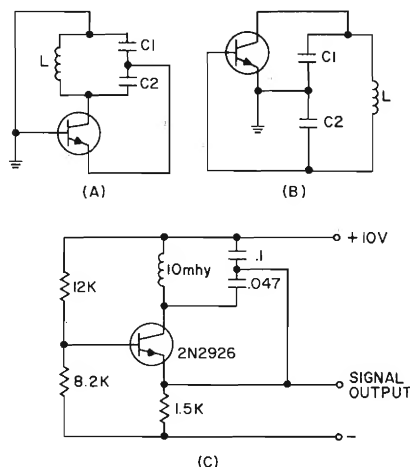
Figure 8.5(C) illustrates a practical 10 Kc Colpitts oscillator having a temperature

COLPITTS OSCILLATOR

Figure 8.5

drift rate of .035%/°C. This is the *total* drift rate and is determined by the temperature rate of incremental permeability of the coil core material. For the purpose of stability analysis, the Thevanin equivalent of the emitter resistor and the bias divider, together with transistor h_{ib} and the loaded voltage divider, are lumped to form the *lossy* feedback loop.

If very high frequency-stability is desired, the frequency determining network should be *buffered* from the amplifier, furnishing its losses, as well as possible. This provision cushions the frequency determining network from the inevitable changes induced from electrical environmental variation, but demands higher losses in coupling networks and a higher amplifier gain to satisfy stability criteria. The alternative to this is a lower loss frequency determining network. The lower loss network is an alternative way of saying that *high Q* is required; where *Q* is defined as the energy stored per radian of angular period divided by the energy lost per radian of angular period. This *Q* definition is the usual figure of merit associated with resonant circuits, but is equally applicable to many other networks having a transcendental solution.

CRYSTAL OSCILLATOR

The quartz crystal is an example of a very low loss resonator which will furnish exceptionally good frequency stability. In Figure 8.6(A,B) the equivalent circuit and impedance vs. frequency characteristic indicate that two modes of operation exist. The lower mode is called the series resonant mode, the upper mode the parallel resonant mode. The series resistance, R_S, of the crystal is a factor of prime importance since it sets, together with the equivalent inductance, the impedance at *mode resonance*. This impedance in turn sets the design of the feedback loop and the frequency stability of the oscillator. In general, the higher the value of R_S, the tighter the coupling to produce sustained oscillation and the poorer the frequency as set by changes in electrical environment. The analysis of oscillator starting criteria directly involves both R_S and L and these should be recognized in writing the expression for loop current gain.

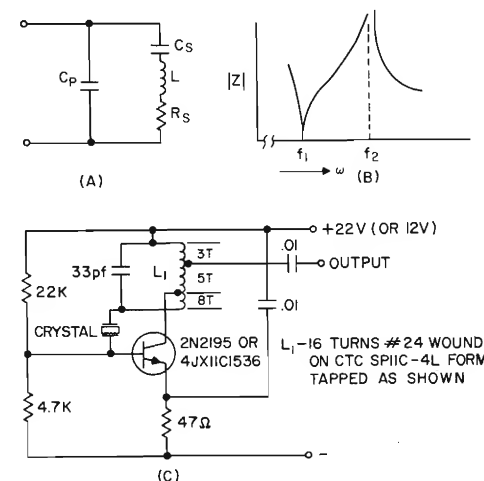
In much of the citizen's band equipment, cost is a constant challenge and higher R_S units must be accommodated. Figure 8.6(C) typifies an oscillator designed to

CRYSTAL OSCILLATOR

Figure 8.6

accept higher R_S crystals (to 30Ω); and provide adequate output to satisfy most MOPA applications. The output tap is arranged to match directly a companion grounded base amplifier (2N2195 – see Experimenter's Chapter). The crystal used is the 3rd overtone type. Operation at lower power is possible, at 12 volts.

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Ware, W. A., Reed, H. R., "*Communication Circuits*," John Wiley & Sons, Inc., New York, New York (1948).

Shea, R. F., et al, "*Transistor Circuit Engineering*," John Wiley & Sons, Inc., New York, New York (1957).

NOTES

FEEDBACK AND SERVO AMPLIFIERS

CHAPTER 9

USE OF FEEDBACK IN TRANSISTOR AMPLIFIERS

NEGATIVE FEEDBACK

Negative feedback is used in transistor amplifiers to fix the amplifier gain, increase the bandwidth (if the number of transistors is less than three),[1] reduce distortion, and change the amplifier input and output impedances. Feedback is used in servo amplifiers to obtain one or more of these characteristics.

Gain is reduced at the midband frequencies as the feedback is increased, and the predictability of the midband gain increases with increasing feedback. Thus, the greater the feedback, the less sensitive will be the amplifier to the gain changes of its transistors with operating point and temperature, and to the replacement of transistors.

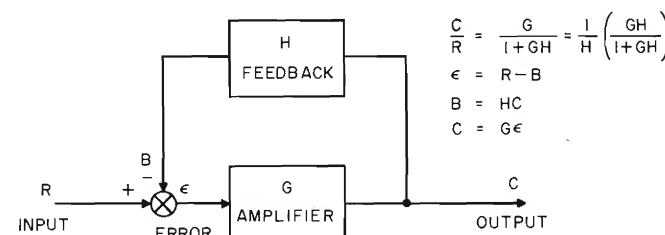
The output and input impedances of the amplifier are dependent upon the type of feedback. If the output voltage is fed back, the output impedance is lowered. In contrast, feedback of the output current raises the output impedance. If the feedback remains a voltage, the input impedance is increased, while if it is a current, the input impedance is decreased.

SERVO-TYPE FEEDBACK SYSTEM

Figure 9.1

A convenient method for evaluating the external gain of an amplifier with feedback is the single loop servo-type system as shown in Figure 9.1. (The internal feedback of transistors can be neglected in most cases.) The forward loop gain of the amplifier without feedback is given by G and it includes the loading effects of the feedback network and the load. H is the feedback function, and is usually a passive network. In using this technique, it is assumed that the error current or voltage does not affect the magnitude of the feedback function. The closed loop gain is then

$$\frac{C}{R} = \frac{G}{1 + GH} = \frac{1}{H}\left(\frac{GH}{1 + GH}\right)$$

where C is the output function and R is the input. If GH is made much larger than one, the closed loop response approaches 1/H and becomes independent of the amplifier gain. Thus, GH determines the sensitivity of the closed loop gain to changes in amplifier gain.

Since GH is a complex quantity whose magnitude and phase are a function of frequency, it also determines the stability of the amplifier. The phase shift of GH for

all frequencies must be less than 180° for a loop gain equal to or greater than one or the amplifier will become unstable and oscillate. Therefore, if the number of transistors in the amplifier is greater than two, the phase shift of GH can exceed 180° at some frequency, and stabilization networks must be added to bring the loop gain to one before the phase shift becomes 180°.

VOLTAGE FEEDBACK AMPLIFIER
Figure 9.2

Figure 9.2 shows a voltage feedback amplifier where both the input and output impedances are lowered. A simplified diagram of the amplifier is shown in Figure 9.2(B), which is useful in calculating the various gains and impedances. Z_1 is the input impedance of the first stage without feedback, and Z_{on} is the output impedance of the last stage without feedback. Ai is the short circuit current gain of the amplifier without feedback (the current in the load branch with $R_L = 0$ for a unit current into the base of the first transistor). Any external resistors such as the collector resistor, which are not part of the load, can be combined with Z_{on}. The gain and impedance equations shown are made assuming that the error voltage ($i_{b1}Z_1$) is zero which is nearly correct in most cases. If this assumption is not made, the loop gain of the amplifier can be derived by breaking the loop at y-y' and terminating the point y with Z_1.[2] The loop gain is then i_f/i_{b1} with the generator voltage set equal to zero. Since the loop is a

numeric, the voltage and current loop gains are identical. The loop gain is then

$$Ai\left(\frac{Z_L'}{Z_L' + Z_F + Z_1'}\right)\left(\frac{Z_g}{Z_g + Z_1}\right) \qquad (9a)$$

where

$$Z_L' = \frac{Z_L Z_{on}}{Z_L + Z_{on}} = Z_L\gamma, \text{ and}$$

$$Z_1' = \frac{Z_g Z_1}{Z_g + Z_1}$$

Notice that if $Z_g >> Z_1$ and $Z_F >> Z_1$, then the loop gain is very nearly equal to GH as given in Figure 9.2.

The input impedance of the amplifier is reduced by 1 + GH, while the output impedance is also decreased.

Figure 9.3 shows a current amplifier where both the output and input impedances are increased. The loop is obtained by breaking the circuit at y-y' and terminating points y-a with Z_1. The loop gain is i_f/i_{b1} and is approximately equal to

$$\frac{\gamma Ai\, Z_F}{Z_g + Z_1} \qquad (9b)$$

CURRENT FEEDBACK AMPLIFIER
Figure 9.3

POSITIVE FEEDBACK

Positive feedback can be used without stability considerations if the loop gain is less than unity. (It can also be used with a loop gain greater than unity if it is used in conjunction with negative feedback, and stability is properly considered.)[4,5] If positive feedback is applied as a current to the transistor base, the input impedance is

increased, while if it is applied as a voltage in series with the emitter, the input impedance is decreased.

A common example of positive feedback with less than unity loop gain is the bootstrapping of the biasing resistors in a transistor amplifier. This is done to minimize the shunting effect these resistors have on the input impedance of the circuit. Figure 9.4(A) shows a transistor amplifier biased in a conventional manner. The transistor's input impedance (Zin_t) seen at the base is

$$Zin_t \approx \frac{h_{fe}\, R_E\, r_C}{h_{fe}\,(R_E + R_L) + r_C} + r_b \qquad (9c)$$

where it is assumed $R_E >> r_e$, and $r_C >> R_L$.

BOOTSTRAPPING THE BIASING RESISTORS AND COLLECTOR

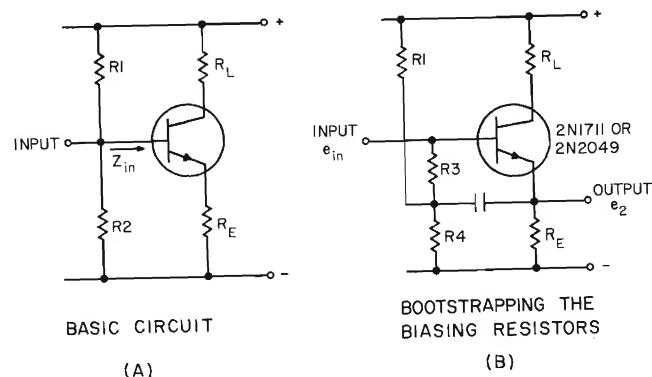
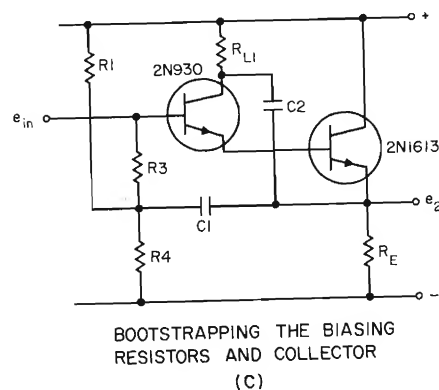
(C)

BOOTSTRAPPING

Figure 9.4

Thus, to increase the transistor's input impedance, it is necessary to increase R_E; however, an upper limit of value r_C is reached when $h_{fe}\, R_E >> r_C$. While this may be in the order of several megohms, the impedance seen at the input terminals is Zin_t in parallel with the parallel combination of R1 and R2. The value of these resistors are determined by the biasing requirements of the circuit, and consequently they reduce the input impedance of the circuit.

Figure 9.4 shows how the bias resistors are bootstrapped in order to reduce their shunting effect on the transistor input impedance. The circuit input impedance (Zin_C) becomes[8]

$$Zin_C = \frac{R3'\, R_E\, h_{fe}}{R3' + R_E\, h_{fe}} \qquad (9d)$$

where $R3' = R3/1 - A$; where it is assumed that the reactance of the capacitor is negligible at the frequencies of interest; and where $h_{fe}\, R1 << r_C$ and $R_L << r_C/h_{fe}$. A is the voltage gain between the base and the emitter or e_2/e_{in}. It is given by

$$A \approx \frac{R_P}{r_b\,(1 - \alpha) + r_e + R_P} \qquad (9e)$$

where

$$\frac{1}{R_P} = \frac{1}{R_E} + \frac{1}{R4} + \frac{1}{R1}, \text{ and } r_e \approx \frac{.026}{I_E}$$

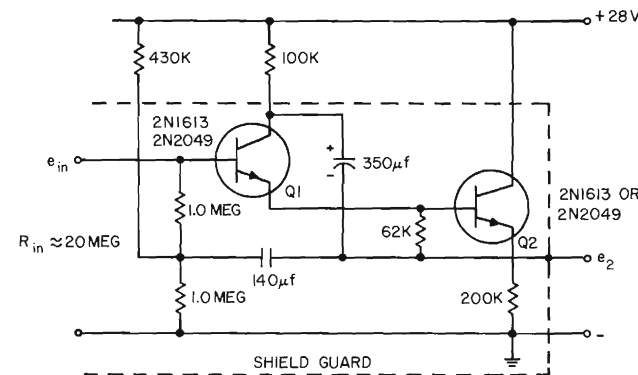
Since the voltage gain can be made near unity, R4' can become very large. For example if R_P is selected to be 3.6K and the transistor is a 2N1711 (biased at 1 ma and 10 volts) with an h_{fe} of 100 and a r_b of 1000 ohms, then $A \approx 0.99$. R3' becomes 100 R3.

BOOTSTRAPPED EMITTER FOLLOWER

Figure 9.5

In some applications the input bootstrapping becomes so effective (through a judicious choice of bias conditions and transistors) that the amplifier input impedance is again limited by r_C. This situation can be remedied by bootstrapping the collector as shown in Figure 9.4(C). Another stage of current gain is provided by Q2, and the voltage e_{O2} is coupled back to the collector of Q1 by C2. Bootstrapping the collector also reduces the effect of the collector to base capacitance, C_{ob}, on the input impedance. Figure 9.5 shows a bootstrapped emitter follower with an input impedance of about 20 megohms and with a band width of 1 cps to 5 kc. The upper frequency is limited by the h_{fe} cutoff frequencies of Q1 and Q2, since they are respectively biased at 10 and 100 μamperes.

SERVO AMPLIFIER FOR TWO-PHASE SERVO MOTORS

PREAMPLIFIERS

Figure 9.6 shows a two stage preamplifier which has a low input impedance, and which is quite stable in bias point and gain over wide temperature ranges. In addition, no selection of transistors is required.

Because only two stages are involved, the amplifier is stable, and frequency stabilization networks are not required. The current gain i_o/i_{in} is approximately R_E/R_F if the generator impedance and R_E are much larger than the grounded emitter input impedance of Q1. R_F should not exceed a few hundred ohms because it contributes to the loss of gain in the interstage coupling network. The loss of gain in the interstage coupling is

$$K = \frac{Z_{o1}'}{Z_{o1}' + h_{ie2} + h_{fe2} R_F} \quad (9f)$$

where Z_{o1}' is the parallel combination of R2 and the output impedance of Q1. The loop gain then is approximately

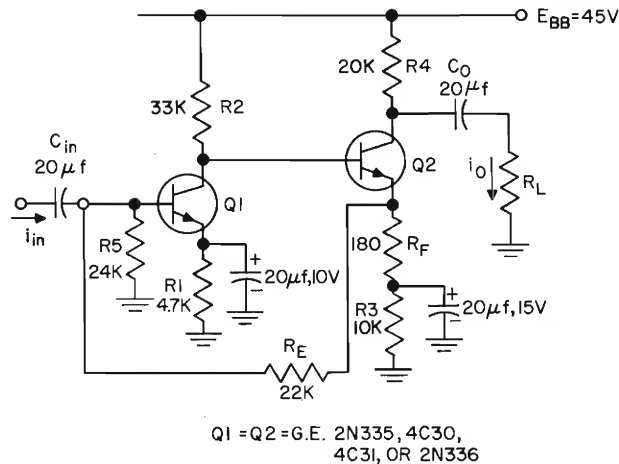
$$\left(\frac{h_{fe1} h_{fe2} K R_F}{R_E}\right) \left(\frac{R_5}{h_{ie1} + R_5}\right) \quad (9g)$$

400 CYCLE PREAMPLIFIER FOR OPERATION IN AMBIENTS OF −55°C TO 125°C

Figure 9.6

Because the feedback remains a current, the input impedance of this circuit is quite low; less than 100 ohms in most cases. This preamplifier will work well where current addition of signals is desired and "cross-talk" is to be kept to a minimum.

Bias Design Procedure for Stage Pair

(Reference Figure 9.7)

1. The values of E_{BB}, I_{E1}, I_{E2}, V_{CE1}, and V_{CE2} are selected by the designer to be compatible with the constraints imposed by the circuit and component specifications. Thus, I_{E2} and E_{BB} must be large enough to prevent clipping at the output under conditions of maximum input. For designs which must operate in wide temperature environment, the bias currents and voltages (I_E and V_{CE}) of Q1 and Q2 should be approximately equal to those used by the manufacturer for specifying the "h" parameters. (For the 2N335, $I_{E1} = I_{E2} = 1$ ma and $V_{CE} = 5$ to 10 volts.)

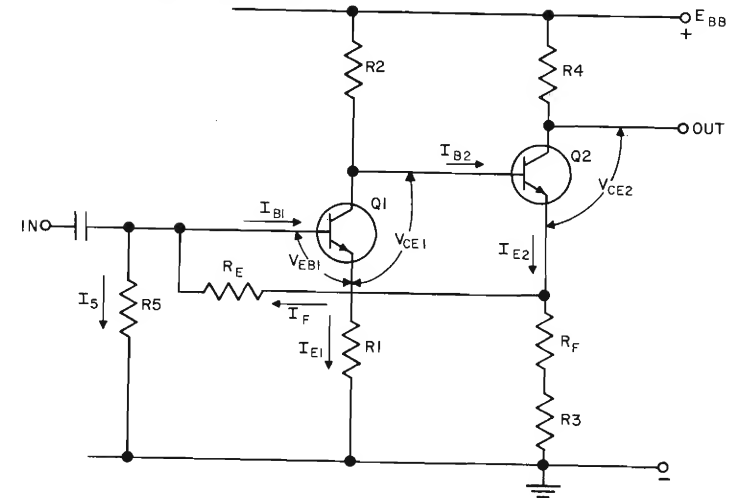



Figure 9.7

2. For good bias stability, I_{E1} R1 should be five to ten times V_{EB1}, i.e., 3 to 5 volts; thus, knowing I_{E1}, R1 can be found. I_5 should also be five to ten times larger than I_{B1}.

3. $$R2 = \frac{E_{bb} - V_{CE1} - I_{E1} R1}{I_{E1} + I_{B1}} \quad (9h)$$

where

$$I_{B2} = \frac{I_{E2}}{h_{FE2}} + I_{CBO2}, \quad I_{B1} = \frac{I_{E1}}{h_{FE1}} + I_{CBO1}, \quad (9i)$$

and where h_{FE1} and h_{FE2} are the typical dc current gains at the particular bias conditions. I_{CBO} is the collector-base leakage current at the temperature and collector-base voltage being used.

4. $$R5 = \frac{I_{E1} R1 + V_{EB1}}{I_5} \quad (9j)$$

where I_5 is selected to be 5 to 10 times larger than I_{B1}.

5. $$R_E = \frac{V_{CE1} - V_{EB1} - V_{EB2}}{I_5 + I_{B1}} \quad (9k)$$

6. $$R3 = \frac{I_{E1} R1 + V_{CE1} - V_{EB2}}{I_{E2} - (I_5 + I_{B1})} \quad (9l)$$

7. $$R4 = \frac{E_{BB} - I_{E2} R3}{2 I_{E2}} \quad (9m)$$

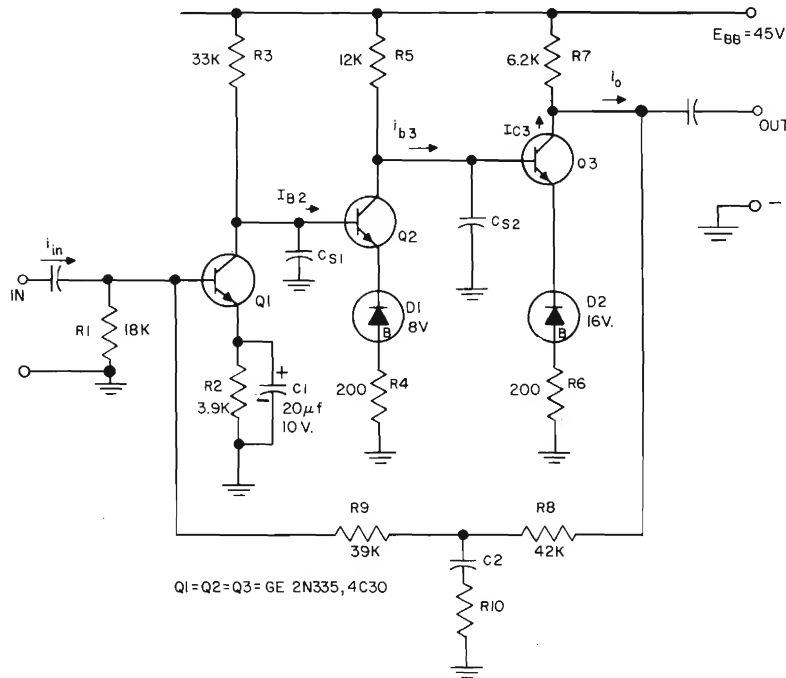
8. $$R_F = \frac{R_E}{G_1} \quad (9n)$$

where G_1 is the desired closed loop ac current gain. (The emitter by-pass capacitors are selected to present essentially a short circuit impedance at the lowest frequency of interest.)

Figure 9.8 shows a three-stage 400 cycle direct-coupled preamplifier with good bias stability from −55°C to 125°C. The dc biasing of the circuit is discussed in Chapter 4, with the collector bias voltage of Q3 being given by equations (4ll) and (4mm).

The various ac gains and impedances can be calculated from the equations of Figure 9.1 with the exception that the ac feedback is now approximately

$$\left(\frac{R_L'}{R8}\right)\left(\frac{R10}{R9}\right) \qquad (9o)$$

where $1/R_L' = 1/R_L + 1/R_{O3} + 1/R7$ and R_{O3} is the output impedance of Q3. This assumes that the input impedance of Q1 is much less than R1 and R9. The value of R10 determines the closed loop gain, while the values of C_{S1}, C_{S2}, R4, and R6 are used to bring the magnitude of the loop gain to unity before the phase shift reaches 180°. The values required for these capacitors and resistors are dependent upon the maximum expected loop gain.

THREE-STAGE 400 CYCLE DIRECT-COUPLED PREAMPLIFIER
Figure 9.8

DRIVER STAGE

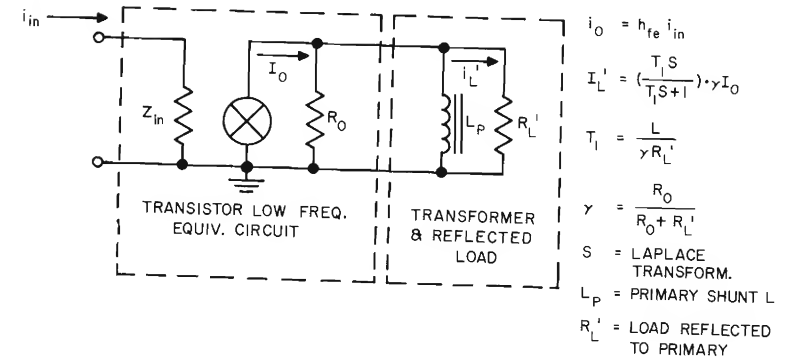
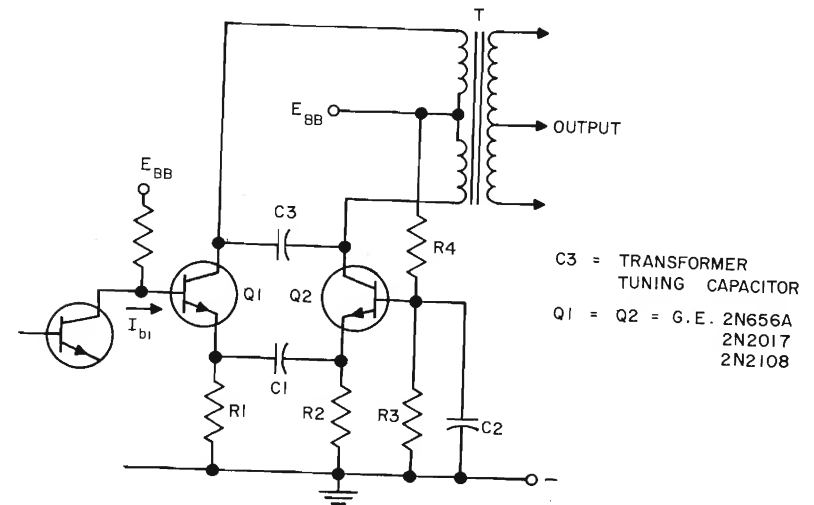
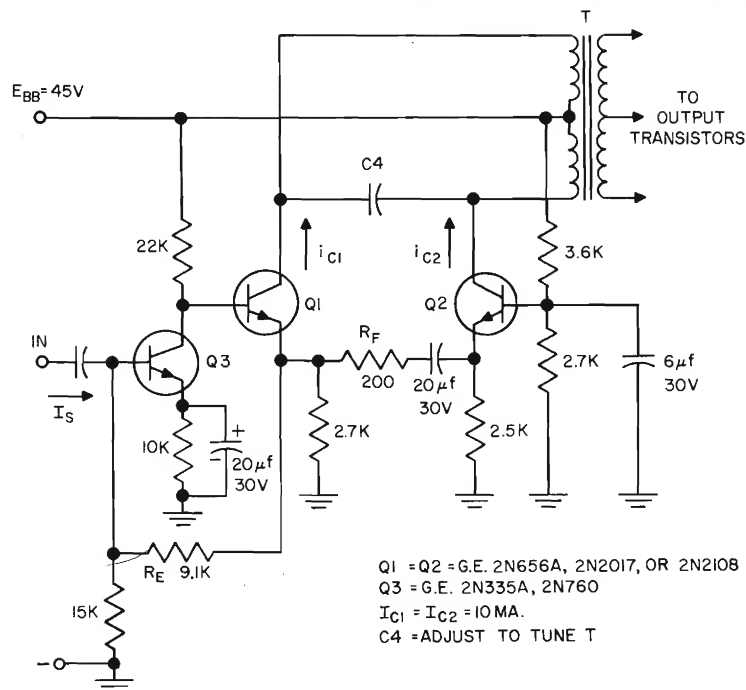
Because the output stages of servo amplifiers are usually operated either Class B or a modified Class B, the driver must provide phase inversion of the signal. In most cases, this is accomplished by transformer coupling the driver to the output stage. The phase shift of the carrier signal in passing through the transformer must be kept small. However, since the output impedance of the transistor can be quite large, the phase shift can be large if the transformer shunt inductance is small, or if the load resistance is large as shown in Figure 9.9. The inductance of most small transformers decreases very rapidly if a dc current flows in the transformer. Therefore in transformer coupling, the phase shift of the carrier is reduced to a minimum if the dc current through the coupling transformer is zero, or feedback is used to lower the output impedance of the driver.

CARRIER PHASE SHIFT DUE TO TRANSFORMER COUPLING
Figure 9.9

Figure 9.10 shows a modified "long tail pair" driver. In this case Q1 and Q2 operate Class A, and the quiescent collector current of Q1 and Q2 cancel magnetically in the transformer. Transistor Q1 operates grounded emitter, while Q2 operates grounded base. Separate emitter resistors R_1 and R_2 are used rather than a common emitter resistor in order to improve the bias stability. The collector current of Q1 is approximately $h_{fe1}\, i_{b1}$, while the emitter current of Q2 is $(h_{fe1} + 1)\, i_{b1}$. Since Q2 operates grounded base, the collector current of Q2 is $-h_{fb2}/(h_{fe1} + 1)\, i_{b1}$ or $-h_{fe}\, i_{b1}$ if the current gain of Q1 and Q2 are equal. Thus push-pull operation is obtained.

In order to stabilize the driver gain for variations in temperature and interchangeability of transistors, another transistor can be added to form a stage pair with Q1 as

TWO-STAGE CLASS "A" PUSH-PULL DRIVER
Figure 9.10

Q1 = Q2 = G.E. 2N656A, 2N2017, OR 2N2108
Q3 = G.E. 2N335A, 2N760
$I_{C1} = I_{C2} = 10$ MA.
C4 = ADJUST TO TUNE T

"STABLE" 400 CYCLE DRIVER
Figure 9.11

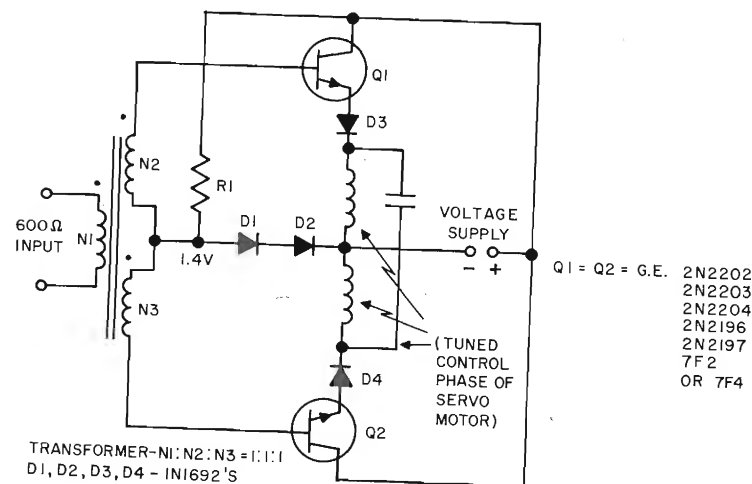
shown in Figure 9.11. The gain of the driver is then very stable and is given approximately by

$$\frac{i_{C1}}{i_S} \cong \frac{-i_{C2}}{i_S} \cong \frac{R_E}{R_F} \qquad (9p)$$

OUTPUT STAGE

The output stages for servo amplifiers can be grounded emitter, grounded collector or grounded base. Output transformers are generally not required because most servo motors can be supplied with split control phase windings. Feedback of the motor control phase voltage to the driver or preamplifier is difficult if transformer coupling is used between the driver and output stages. If a high loop gain is desired, the motor and transformer phase shifts make stabilization of the amplifier very difficult. One technique which can be used to stabilize the output stage gain is to use a grounded emitter configuration where small resistors are added in series with the emitter and the feedback is derived from these resistors. The motor time constants are thus eliminated and stabilization of the amplifier becomes more practical.

A second technique which results in a stable output stage gain and does not require matched transistor characteristics is the emitter follower (common collector) push-pull amplifier as shown in Figure 9.12. Also it offers the advantage of a low impedance drive to the motor. A forward bias voltage of about 1.4 volts is developed across D1 and D2, and this bias on the output transistors gives approximately 20 ma of no signal current. At lower levels of current the cross-over distortion increases and the current gain of the 2N2202 decreases. D3 and D4 protect the 2N2202's from the inductive

load generated voltages that exceed the emitter-base breakdown. The efficiency of this circuit exceeds 60% with a filtered dc voltage supply and can be increased further

SERVO MOTOR DRIVE CIRCUIT
(1 TO 4 WATTS)
Figure 9.12

by using an unfiltered rectified ac supply. This unfiltered supply results in lower operating junction temperatures for the 2N2202's, and in turn permits operation at a higher ambient temperature. The maximum ambient operating temperature varies with the power requirements of the servo motor and the type of heat radiator used with the 2N2202. It is practical to attain operation in ambients to 125°C.

Another technique which results in a stable output amplifier gain over wide ambient temperature extremes and which is compatible with low gain transistors is shown in Figure 9.13. In this case, a grounded base configuration and a split control phase motor winding are used. The driver is coupled to the output stage by means of a step-down transformer, and the current gain occurs in the transformer since the current gain of the transistors is less than one. The current gain is $2\alpha N_{P1}/N_{S1}$ if the drivers are operated Class A such as shown in Figures 9.10 or 9.11. The negative unfiltered dc supply and diode D1 are used to operate the transistor Class AB and eliminate cross-over distortion. As the signal increases, the diode D1 becomes conductive and shunts the bias supply. The operation of the output stage thus goes from Class A to Class B.

An unfiltered dc is used for the collector supply to reduce transistor dissipation. If saturation resistance and leakage currents are neglected, 100% efficiency is possible under full load conditions with an unfiltered supply. The transistor dissipation is given by

$$P \approx \frac{E_{CM}^2}{4\,R_L}\left[a - a^2\left(1 + \frac{R_S}{R_L}\right)\right] + P_L \qquad (9q)$$

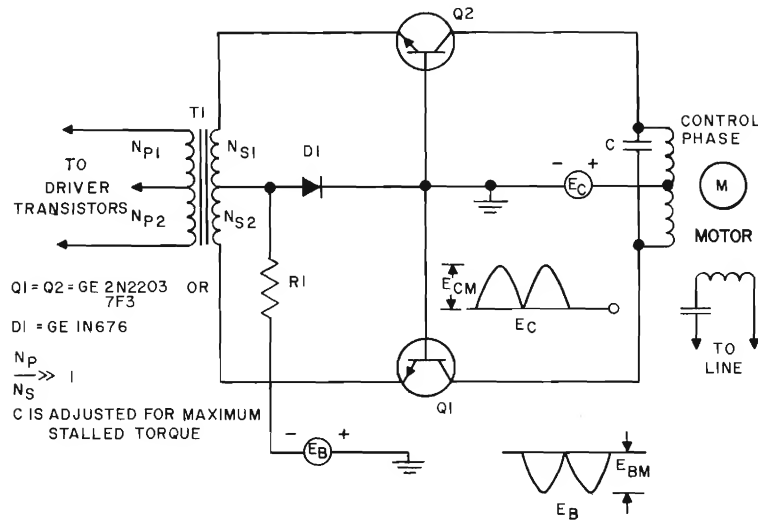
where P_L is the dissipation due to leakage current during the half-cycle when the transistor is turned off, a is the fraction of maximum signal present and varies from 0 to 1, R_S is the saturation resistance, R_L is the load resistance, and E_{CM} is the peak value of the unfiltered collector supply voltage. If P_L is negligible and $R_S/R_L << 1$,

GROUNDED BASE SERVO OUTPUT STAGE

Figure 9.13

then maximum dissipation occurs at a = 1/2 or when the signal is at 50% of its maximum. Thus for amplifiers which are used for position servos, the signal under steady-state conditions is either zero or maximum which are the points of least dissipation.

The peak current which each transistor must supply in Figure 9.13 is given by

$$i_M = \frac{2W}{E_{CM}} \tag{9r}$$

where W is the required control phase power. The transistor dissipation can then be written in terms of the control phase power

$$P = \frac{W}{2}\left[a - a^2\left(1 + \frac{R_S}{R_L}\right)\right] + P_T \tag{9s}$$

The driver must be capable of supplying a peak current of

$$\frac{i_M}{\alpha}\left(\frac{N_{S1}}{N_{P1}}\right) \tag{9t}$$

where α is the grounded base current gain of the output transistor.

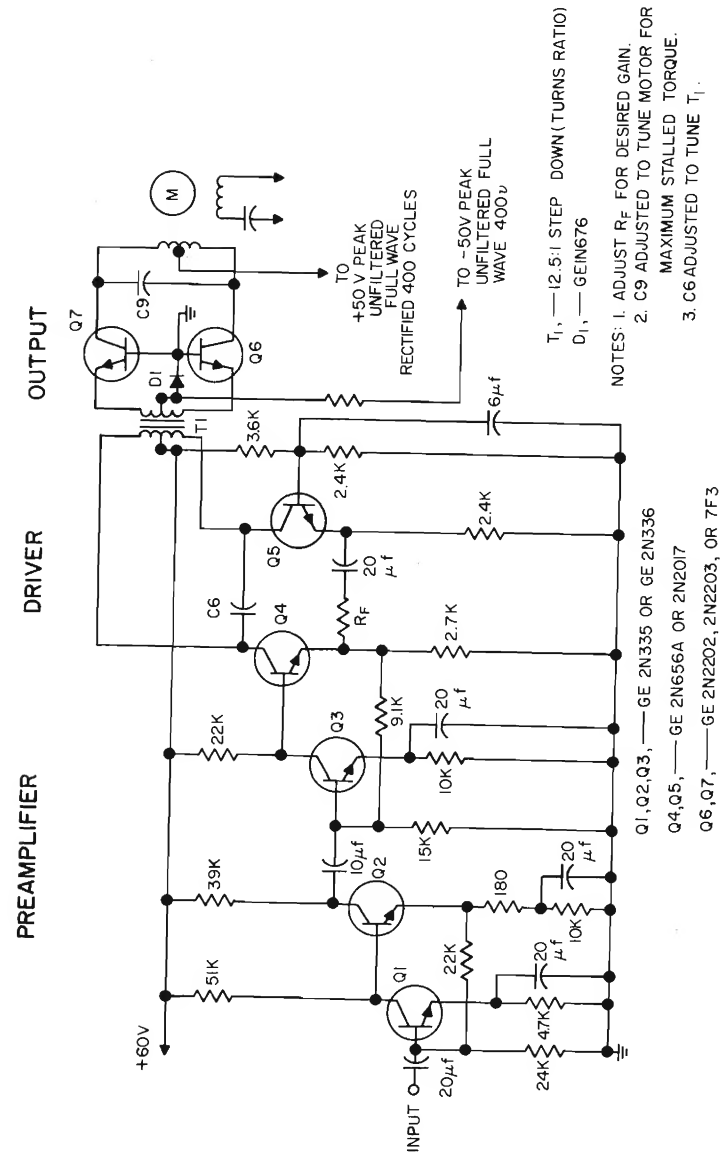
Figure 9.14 shows a complete servo amplifier capable of driving a 3 watt servo motor in an ambient of −55°C to 125°C (if capacitors capable of operation to 125°C are used). The gain can be adjusted from 20,000 to 80,000 amperes/ampere by adjusting R_F in the driver circuit. The variation of gain for typical servo amplifiers of this design is less than 10% from −55°C to 25°C, and the variation in gain from 25°C to 125°C is within measurement error. The variation in gain at low temperature can be reduced if solid tantalum capacitors are used instead of wet tantalum capacitors. The reason is that the effective series resistance of wet tantalum capacitors increases quite rapidly at low temperatures thus changing the amount of preamplifier and driver feedback. The effective series resistance of solid tantalum capacitors is quite constant with temperature. Many 85°C solid tantalum capacitors can be operated at 125°C if they are derated in voltage.

3 WATT 400 CYCLE SERVO AMPLIFIER FOR −55°C TO 125° OPERATION

Figure 9.14

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(2) Hellerman, H., "Some Stability Considerations in the Design of Large Feedback Junction Transistor Amplifiers," *Conference Paper #CP58-87,* presented at the 1958 AIEE Winter General Meeting.

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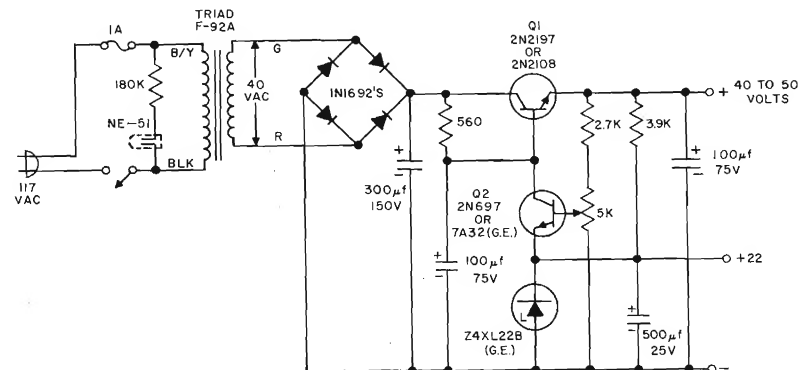
NOTES

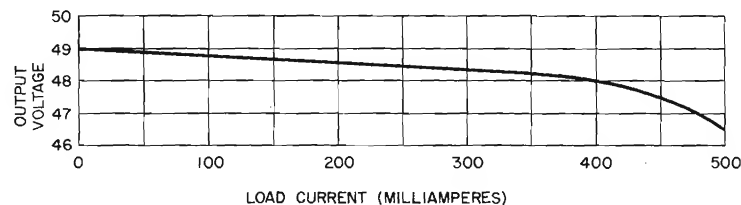
REGULATED DC SUPPLY AND INVERTER CIRCUITS

CHAPTER 10

REGULATED DC SUPPLIES

The regulated supply of Figure 10.1 is a conventional circuit using a series regulating element. With Q1 mounted on a 2½" x 2½" x 3⁄32" aluminum fin the circuit can operate in an ambient temperature up to 55°C. The 2N2108 can be mounted with a washer as shown in Chapter 11.

REGULATED DC VOLTAGE SUPPLY
Figure 10.1

Q1 requires a V_{CER} capability equal to the unregulated output voltage of the bridge. The voltage rating for Q2 must be equal to the difference between the regulated output and the Zener voltage.

Figure 10.2 shows equal regulating ability for all load currents to 350 ma, and 2% voltage regulation at 400 ma. Peak-to-peak output ripple of this circuit is less than 0.3 volt at 400 ma load current, and 0.01 volt at no load; output impedance is less than 2 ohms from dc to 20 cycles and then decreases to less than 1 ohm at 200 ma load current. The output voltage has very little overshoot with step load functions.

OUTPUT VOLTAGE VS. LOAD CURRENT
Figure 10.2

Improved regulation is obtained by using a Darlington connection for the series regulating element (Q1 and Q2) as in Figure 10.3. This regulated dc supply also fea-

tures higher current capability. The supply is designed for output currents up to 2 amps average, or 3.5 amps peak. Output voltage can be adjusted from 45 to 65 volts with R7, but for operation below 60 volts output, the total resistance of R2 and R3 should be increased by a percentage equal to the decrease in output voltage. This will maintain the 22 volt Zener dissipation within its rating.

LOAD CURRENT (D.C.)	REGULATION
1/2 AMP	0.50 %
1 AMP	0.72%
2 AMP	2.1 %

REGULATED DC VOLTAGE SUPPLY

Figure 10.3

Transistors Q2 and Q3 should each be mounted on a heat dissipator capable of dissipating approximately 2 watts; such as an IERC #LP5A1B (135 West Magnolia Blvd., Burbank, California), or a Thermolloy Company #2210 (4417 North Central Expressway, Dallas, Texas). Q1 should be mounted on a heatsink that has a thermal resistance of less than 2.5°C per watt; such as the Delco Radio heatsink #7270725. The 1N3570's can be mounted with insulating hardware to a metal surface of 10 square inches or more.

Output ripple is less than 1 millivolt rms at no load and increases to 60 millivolts peak-to-peak at 2 amps dc load current; output impedance at 0.5 amp dc load current is less than 0.5 ohm down to dc. There is negligible shift in output voltage with step load current from 0 to 1 amp. The output overshoots approximately 5% (decaying in 0.10 sec.) with step load change from 1 amp to zero.

The 6.2 volt Zener diode together with R1 limits the peak output current to approximately 5.5 amps. At higher currents the emitter-base of Q1 will have less than 0.66 volt drive, thus the output voltage will decrease. If 5.5 amps is sustained for about 100 milliseconds, the 3 amp fuse will open.

PRECISION POWER SUPPLIES USING REFERENCE AMPLIFIER[1]

The General Electric types RA-1, RA-2 and RA-3 are Reference Amplifiers (see G.E. Pub. 35.35) designed for applications in regulated voltage or current supplies where they can serve the dual function of a voltage reference element and an error voltage amplier. They are *integrated* devices comprised of a Zener diode and NPN transistor in a single pellet. Cancellation of temperature coefficients between the Zener diode and the transistor result in a transfer characteristic having a very low net

temperature coefficient. Temperature differentials between the Zener diode and the transistor are minimized owing to the integrated structure with a consequent reduction in the transient variation and long term drift of the reference voltage. Reference Amplifiers offer significant advantages in performance, circuit simplicity, and overall cost.

The *temperature coefficient* of the Reference Amplifier is determined by

$$\% \text{ per } ^\circ\text{C} = \frac{V_{ref @ T_1} - V_{ref @ 25^\circ C}}{(V_{ref @ 25^\circ C})\,(T_1 - 25^\circ C)} \times 100\% \qquad (10a)$$

where $V_{ref @ T_1}$ is the reference voltage at temperature T_1 and $V_{ref @ 25^\circ C}$ is the reference voltage at 25°C. The temperature coefficient of the Reference Amplifier as defined above shall not exceed the specified maximum value at any temperature over the entire operating temperature range. This definition is illustrated in Figure 10.4 together with a curve of ΔV_{ref} versus temperature for a typical unit. Note that the curve must lie entirely within the triangular areas to satisfy the specifications for the type RA-2B.

In contrast, the common method of specifying the temperature coefficient of a compensated Zener diode is to determine the voltage variation at each temperature extreme equivalent to the specified temperature coefficient and to guarantee only that this voltage variation will not be exceeded at temperatures between 25°C and the temperature extreme. This definition is illustrated in Figure 10.4(B) together with a curve of ΔV_z versus temperature for a typical unit. Note that although the temperature range and maximum temperature coefficient is the same as for the Reference Amplifier, the voltage variation is considerably higher for the Zener, particularly for temperatures in the vicinity of 25°C.

The temperature coefficient specification applies only when the biasing conditions are identical to those given in the specification. Increasing the collector current or the bias current will tend to make the temperature coefficient more positive.

TEMPERATURE COEFFICIENT

Figure 10.4

A *base source resistance*, R_B, is included in the specification of the reference voltage temperature coefficient to duplicate the effect of the resistance divider which is used in most power supplies to set the output voltage. It is desirable to choose the resistance of the divider as low as possible to maximize the gain of the Reference Amplifier and to reduce the effects of I_{CO} and h_{FE} on the reference voltage. However, considerations such as power dissipation in the divider and current drain will set a lower limit on the resistance which can be used. In consideration of these requirements a compromise value of 1000 ohms has been chosen for R_B.

The transfer characteristic of the Reference Amplifier as shown in Figure 10.5 is of importance in the design of a regulated power supply since it determines the change in collector current resulting from a small change in the reference voltage at the base.

tures higher current capability. The supply is designed for output currents up to 2 amps average, or 3.5 amps peak. Output voltage can be adjusted from 45 to 65 volts with R7, but for operation below 60 volts output, the total resistance of R2 and R3 should be increased by a percentage equal to the decrease in output voltage. This will maintain the 22 volt Zener dissipation within its rating.

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Output ripple is less than 1 millivolt rms at no load and increases to 60 millivolts peak-to-peak at 2 amps dc load current; output impedance at 0.5 amp dc load current is less than 0.5 ohm down to dc. There is negligible shift in output voltage with step load current from 0 to 1 amp. The output overshoots approximately 5% (decaying in 0.10 sec.) with step load change from 1 amp to zero.

The 6.2 volt Zener diode together with R1 limits the peak output current to approximately 5.5 amps. At higher currents the emitter-base of Q1 will have less than 0.66 volt drive, thus the output voltage will decrease. If 5.5 amps is sustained for about 100 milliseconds, the 3 amp fuse will open.

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temperature coefficient. Temperature differentials between the Zener diode and the transistor are minimized owing to the integrated structure with a consequent reduction in the transient variation and long term drift of the reference voltage. Reference Amplifiers offer significant advantages in performance, circuit simplicity, and overall cost.

The *temperature coefficient* of the Reference Amplifier is determined by

$$\% \text{ per } ^\circ C = \frac{V_{ref\,@\,T_1} - V_{ref\,@\,25^\circ C}}{(V_{ref\,@\,25^\circ C})\,(T_1 - 25^\circ C)} \times 100\% \qquad (10a)$$

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TEMPERATURE COEFFICIENT
Figure 10.4

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The transfer characteristic of the Reference Amplifier as shown in Figure 10.5 is of importance in the design of a regulated power supply since it determines the change in collector current resulting from a small change in the reference voltage at the base.

The circuit transconductance, defined as the ratio of collector current change to reference voltage change, is equivalent to the slope of the curve in Figure 10.5.

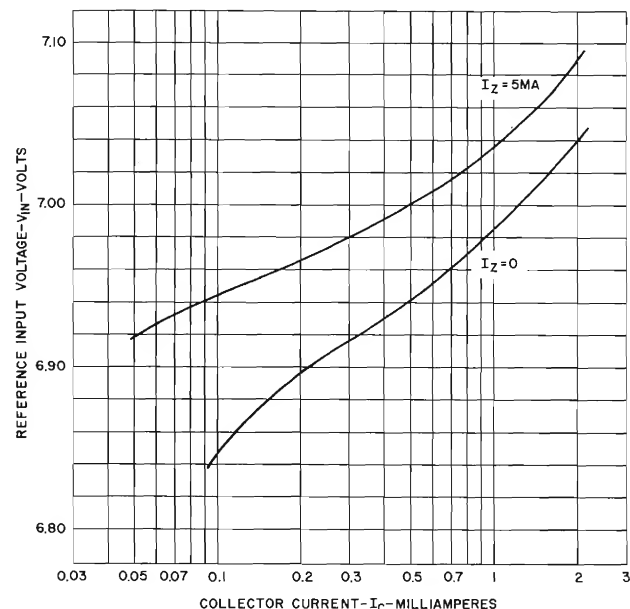
$$g_{mc} = \frac{dI_C}{dV_{ref}} \quad (V_C, I_Z \text{ constant}) \tag{10b}$$

TRANSFER CHARACTERISTICS OF REFERENCE AMPLIFIER

Figure 10.5

The circuit transconductance includes the effects of the base source resistance and the dynamic Zener impedance and hence is lower than the transconductance of a transistor common emitter amplifier stage ($1/h_{ib}$). The circuit transconductance is approximately

$$g_{mc} = \frac{1}{h_{ib} + R_B/(1 + h_{fe}) + r_Z} \tag{10c}$$

where r_Z is the *dynamic resistance* of the Zener diode and all parameters are measured at the specified bias conditions.

The dynamic resistance of the Zener diode in the Reference Amplifier is relatively low as indicated by Figure 10.6 from which it is seen that at low current levels r_Z is lower than the dynamic resistance of a forward biased silicon diode. The low value of r_Z permits the Reference Amplifier to be operated at values of collector current as low as 0.5 ma without additional biasing current for the Zener diode, thus permitting a simplification in the design of regulated power supplies without requiring a compromise in performance.

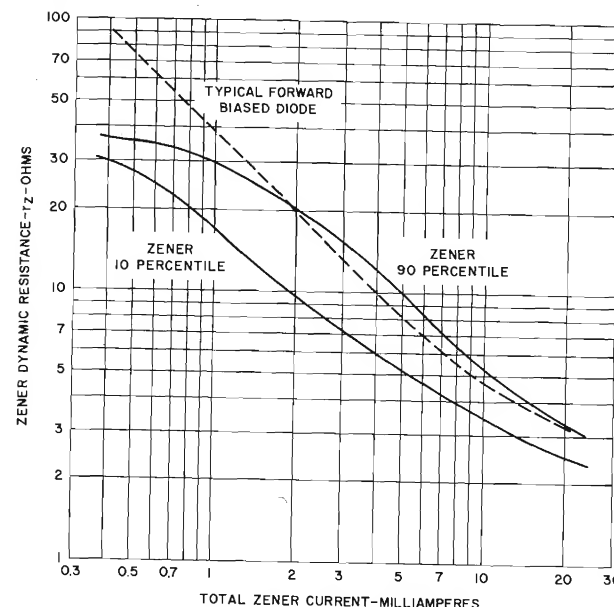
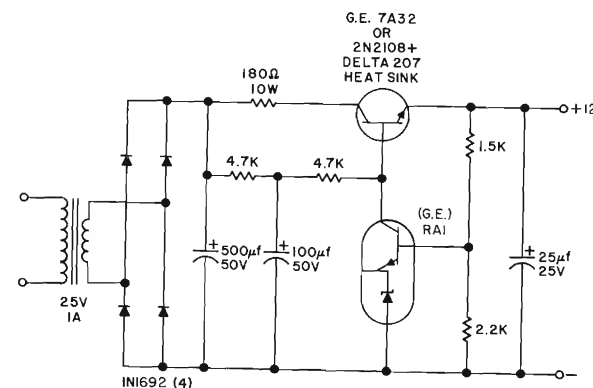
The simplest version of a regulated power supply using the Reference Amplifier is shown in Figure 10.7. This supply is designed for an output of 12 volts at currents up to 100 ma. The 180 ohm resistor provides short circuit protection, limiting the output current to less than 200 ma. The 100 μfd capacitor and the 4.7K resistors provide an effective filter for the base current to the 2N2108 transistor, reducing the

REFERENCE AMPLIFIER ZENER DYNAMIC RESISTANCE

Figure 10.6

REGULATED DC VOLTAGE SUPPLY

Figure 10.7

output ripple to less than 80 microvolts under full load conditions. Output impedance of the supply is approximately 0.65 ohms. For line voltage variations of ±10% the output voltage regulation is better than ±0.3%.

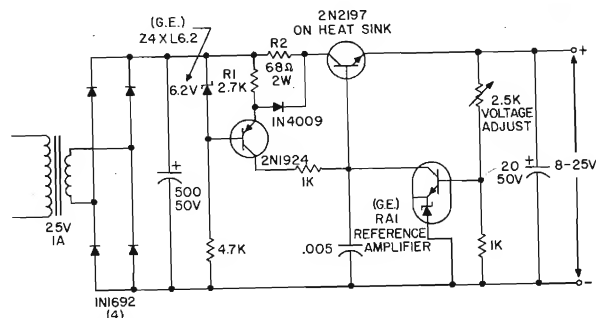
The variable 8 to 25 volts supply in Figure 10.8 limits the current to 100 ma for protection against output shorting. Limiting occurs when the voltage drop across R2 exceeds 6.8 volts and cuts off the current flow in the 2N1924, which is the bias current

GENERAL PURPOSE POWER SUPPLY WITH CURRENT LIMITING

Figure 10.8

source for the 2N2197. In operation the 2N1924 functions as a constant current source and improves regulation with input voltage variations to the regulator circuit. The circuit of Figure 10.8 has 0.02% regulation for line voltages from 105 to 130 volts. The output impedance is 1.0 ohm and the ripple is 200 μv at 20 volts, 100 ma.

Output currents up to 300 ma can be obtained by reducing R1 and R2 and using a suitable heatsink for the 2N2197. The heatsink should be large enough to keep the case temperature below 100°C at minimum output voltage, maximum output current, and maximum line voltage.

PRECISION REGULATED VOLTAGE SUPPLY

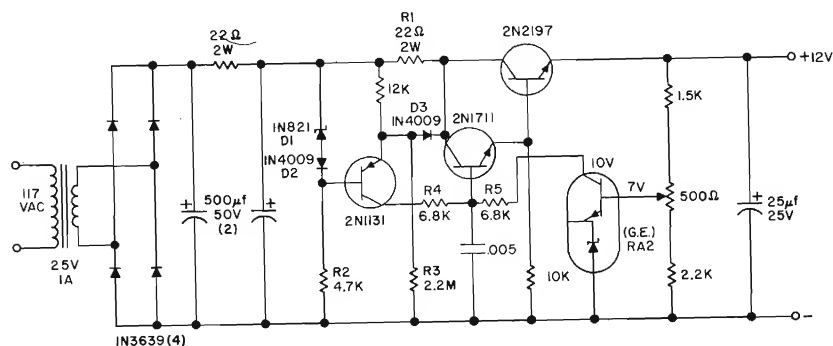
Use of the Reference Amplifier in a precision 12 volt, 200 ma regulated voltage supply is shown in Figure 10.9. In this supply the 2N1131 PNP silicon transistor is used to regulate the collector current of the Reference Amplifier. The output current of the 2N1131 will vary with line voltage due to the finite output resistance of the transistor and the voltage divider action between R2 and the dynamic resistance of D1 and D2. Resistor R3, added to compensate for these effects, makes the output current of the 2N1131 almost completely independent of changes in line voltage. For a ±10% change in line voltage, the variation in output voltage is typically less than ±0.001% and by adjustment of R3 can be reduced to less than ±0.0001%. Diode D2 provides temperature compensation for the base-emitter diode of the 2N1131.

PRECISION REGULATED VOLTAGE SUPPLY

Figure 10.9

This compensation is not critical since, owing to the gain of the Reference Amplifier, a 1% change in the collector current of the 2N1131 has only the effect of a 0.01% change in the reference voltage.

A Darlington transistor connection is used for the series regulator. The current gain of the Darlington is typically 10,000 at 100 ma so the normal variation of collector current of the Reference Amplifier over the full range of output current will be 10 microamperes, or only 2% of the nominal collector current.

In a constant-voltage power supply, regulation of the collector current in the Reference Amplifier allows the collector-to-base voltage to be adjusted to the 3 volt nominal operating value by adding resistor R5 between the base of the series regulator and the collector of the Reference Amplifier. R4 limits any surge current via the base-collector path in the 2N1131.

Sharp current limiting is provided in this circuit at 300 ma by R1 and D3. When the IR drop across R1 exceeds 6 volts, diode D3 will conduct decreasing the emitter current to the 2N1131 and thus reducing the base current to the 2N1711. The output impedance of the power supply is approximately .012 ohm; output ripple and noise at full load is less than 300 microvolts peak-to-peak. Voltage regulation for 100 ma load change is 0.01%. Temperature stability of the supply is mainly dependent on the temperature coefficient of the reference amplifier. An overall temperature coefficient of ±0.002%/°C can easily be achieved using the RA-2B.

PRECISION CONSTANT CURRENT SUPPLY

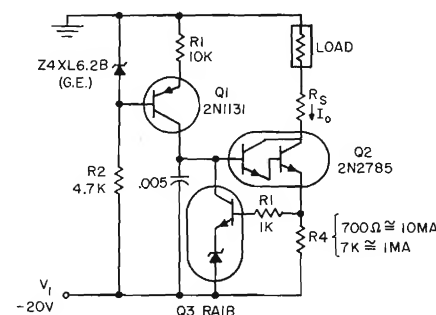
In many applications requiring precise measurements of dc parameters, it is more convenient to use a current reference rather than a voltage reference. However, there is a popular misconception that precision current sources are more difficult to achieve than precision voltage sources.

PRECISION CONSTANT CURRENT SUPPLY

Figure 10.10

It will be noted that the current reference supply is similar to the voltage reference supply shown in Figure 10.9, but is somewhat simpler. The Reference Amplifier in Figure 10.10 acts together with transistor Q2 to maintain the voltage constant across R4 at V_{ref}. The current through R4 equals the current through the load except for the relatively small base currents of Q2 and Q3.

$$I_{LOAD} = \frac{V_{ref}}{R4} - I_{B2} + I_{B3} \qquad (10d)$$

where I_{B2} is the base current to Q2 and I_{B3} is the base current to Q3. Since these currents have opposite signs in the above expression, they can be made to compensate for

each other for changes in ambient temperature by proper selection of transistors and bias points. However, since the base currents have only a second order effect on the temperature coefficient of the output current, it is generally more practical to include the base current changes in the overall temperature compensation.

Transistors with typical values of h_{fe} and h_{oe} were used to evaluate the circuit. The Reference Amplifier had a temperature coefficient of +0.002%/°C. Resistor R4 is a Precision Resistor Corporation wire wound type having specified temperature coefficient of ±20 ppm per °C. All other resistors, being much less critical than R4, are standard composition types. During performance evaluation, output current was measured across a precision resistor, in place of load, using a Keithley 660 differential voltmeter; output impedance was measured by inserting a resistor in series with the load with a value chosen to give a 10 volt drop and noting the resultant change in voltage across the load. The entire circuit was inserted in a temperature chamber.

TEST CONDITION NO. 1: $I_O = 10$ ma (R4 = 700 ohms)

Change in current for 10 volts change in V_1
$\Delta I_O < 100$ na (0.001% or 1 ppm per volt)

Output impedance
> 100 megohms

Change in current with temperature (25°C to 55°C)
$\Delta I_O = +5.0\ \mu a$ (+0.0013% per °C)

TEST CONDITION NO. 2: $I_O = 1.0$ ma (R4 = 7K)

Output impedance
> 1300 megohms

Change in current with temperature (25°C to 55°C)
$\Delta I_O = -0.2\ \mu a$ (−0.0008% per °C)

Drift (15 hours)
$< 0.01\%$ (limited by measuring resistor)

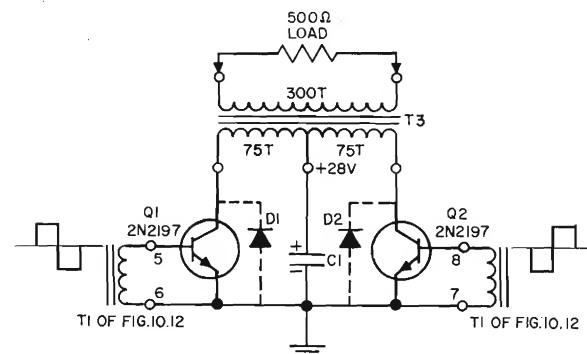
No attempt was made to minimize the temperature coefficient by trimming the circuit values. This could easily be done by adjusting the bias current to the collector of the Reference Amplifier by changing the value of R1. The specification sheet for RA-1 shows change in reference voltage vs. temperature for different collector currents.

PARALLEL INVERTERS

The parallel inverter configuration shown in Figure 10.11 provides an output that is essentially a square wave. An ac input can be rectified to provide the primary power for the inverter, in which case it will function as a frequency changer. A square wave drive to this inverter causes Q1 to conduct half the time while Q2 is blocking, and vice-versa. In this manner, the current from the supply will flow alternately through the two sides of the transformer primary and produce an ac voltage at the load.

It may be desirable to incorporate the feedback diodes D1 and D2 if the circuit is to be lightly loaded or operated under open circuit conditions. For reactive loads these diodes can conduct to supply the out-of-phase portion of the load current. When the inverter switches from Q1 to Q2 an inductive load prevents the main load current from reversing instantaneously, so transformed load current must flow through D2 and back into the dc supply until the load current reverses. The feedback diodes prevent the voltage across either half of the primary winding from exceeding the supply voltage. These diodes not only maintain a square wave output under all load conditions, but also decrease the voltage requirements for Q1 and Q2.

DC TO AC (SQUARE WAVE) INVERTER

Figure 10.11

The dc source should have a low transient impedance, and a capacitor on the output of the dc supply is usually required so it can accept power as well as supply power. It is often important to have this capacitor (C1) right at the inverter itself as shown in Figure 10.11 since the inductance of the supply leads of a few feet in length represents an undesirable impedance during the μsec switching intervals.

For a driven transistor inverter, it is desirable to select a transformer and core with a volt-second saturation capability that is at least two times the actual circuit requirements. The leakage inductance should be held to a minimum since the transformer will be subjected to rapidly changing currents during the switching interval. Bifilar transformer winding is usually used to obtain tight coupling between the two primary windings. Since the inverter output transformer (T3) cannot be allowed to saturate, its design must either incorporate an air gap, have a high ratio of saturation to residual flux density, or be used with predictable reset circuitry.

The inverter circuit of Figure 10.11 was operated using two stacked AJ-H12 (Arnold) C-cores (4 mil), in transformer T3. The core gap spacing was .02 inch. This gives about a 2:1 volt-second capability at 400 cycles.

The square wave inverter drive is easily obtained with a transistor multivibrator that uses a unijunction transistor to stabilize and control the frequency as in Figure 10.12. This circuit provides a symmetrical square wave drive which avoids second harmonics in the output and also a dc component in the inverter, tending to saturate the transformer. With this drive circuit, the inverter output voltage waveform across the load is shown in Figure 10.13. The efficiency of the square wave inverter (Figure 10.11) is 80 to 85% in the 400 to 3200 cycle frequency range at 16 watts output. General Electric transistor type 11C10B1 can be used for Q1 and Q2 of Figure 10.11 with both improved efficiency and waveform at 3200 cycles. The efficiency is 92% at 20 watts output. Type 11C10B1 has lower saturation voltage because of epitaxial construction and also higher switching speeds. Q1 and Q2 should each be mounted on a heatsink capable of dissipating 1.75 watts.

The circuit of Figure 10.12 is a slightly modified "hybrid-multivibrator," described in more detail in Chapter 13. The unijunction transistor provides a source of short, precisely timed negative pulses with the period between pulses depending on the C1R2 time constant. These pulses are coupled to the common emitter resistor of a conventional transistor flip-flop (Q3 and Q4). Each pulse from the unijunction transistor will turn off the transistor which is on in the flip-flop and the resulting square wave of voltage at the collectors is coupled to the inverter by a small transformer. D3 and D4 are used to prevent the emitter-base voltage of Q3 and Q4 from exceeding ratings when a transistor is turned off.

The multivibrator free-runs at about 100 cps, but is synchronized and controlled

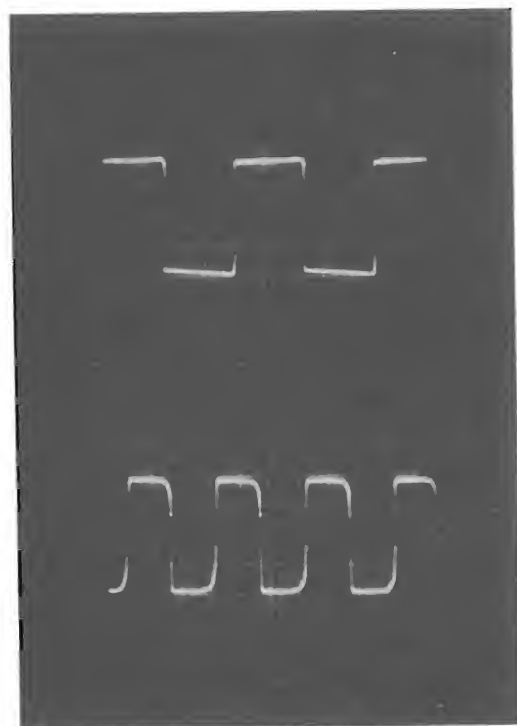
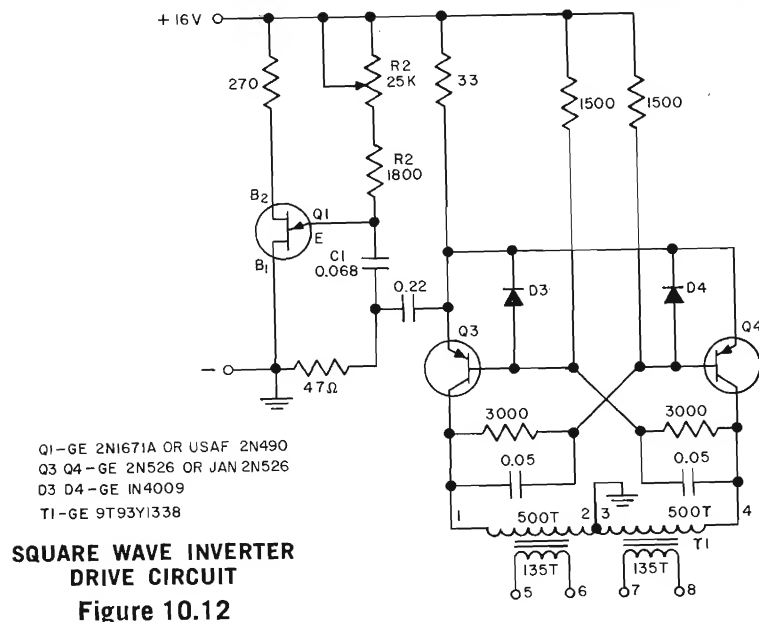
SQUARE WAVE INVERTER DRIVE CIRCUIT

Figure 10.12

400 cycles

3200 cycles

INVERTER OUTPUT VOLTAGE
(VERTICAL SCALE 50 VOLTS/CM)

Figure 10.13

by the unijunction at the higher operating frequencies at which it is designed to operate. This circuit has good frequency stability with variations in supply voltage and ambient temperature, due to the inherent stability of the unijunction. The circuit has an operating frequency range of 400 to 3200 cps in an ambient temperature up to 70°C. The output impedance of this square wave generator is about 8 ohms and the open circuit voltage is about 4 volts peak.

DC TO DC CONVERTERS

A simple and efficient saturating core inverter is shown in Figure 10.14. The load can be shorted without any harm to the circuit and operation automatically resumes after removal of the short. The operating frequency is approximately 8.5 kc with an efficiency of 80% at 10 watts output. Each transistor should be mounted on a heatsink that can dissipate about 1.5 watts; such as IERC #LP5A1B (135 West Magnolia Blvd., Burbank, California), or Thermolloy Company, #2210 (4417 North Central Expressway, Dallas, Texas).

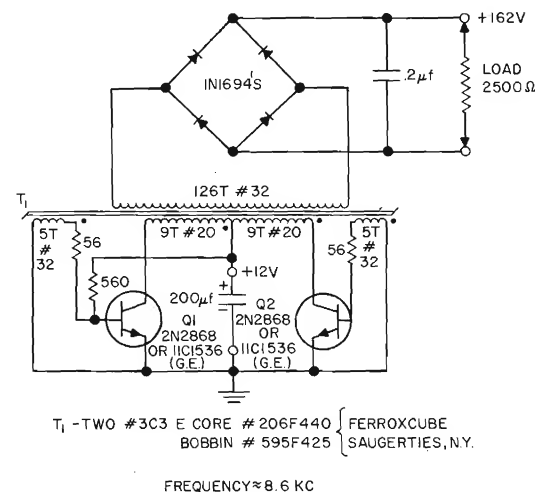
FREQUENCY≈8.6 KC

DC TO DC CONVERTER
(12 VOLT SUPPLY)

Figure 10.14

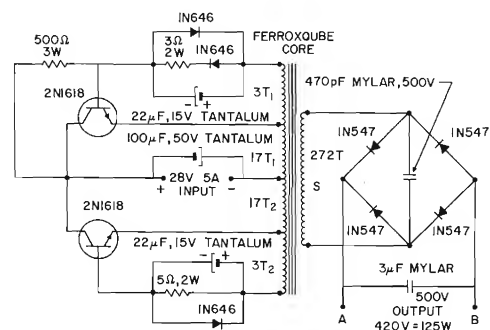
The 560 ohm resistor assures start-up with Q1 conduction initially. The 56 ohm resistor in series with the base, limits the drive and hence the transistor current during the switching interval at core saturation. The operating frequency is determined by

$$t_1 = \frac{2N\phi}{V_s} \qquad (10e)$$

where

t_1 = 1/2 the operating period
N = 9 turns in Figure 10.14
ϕ = total flux = BA
B = flux density
A = core cross sectional area
V_s = about 11.5 volts in Figure 10.14

The higher power dc to dc converter in Figure 10.15 has the following characteristics:

Output	–	125 watts
Input voltage	–	28 volts
Input current	–	5.1 amps
Operating frequency	–	10 kc
Output voltage	–	420 volts
Output current	–	0.3 amps
Output voltage ripple	–	0.7 volts $_{P-P}$
Efficiency	–	87%
Ambient temperature range	–	−50°C to +125°C

1/2 SECONDARY WINDING 136 TURNS — CASING — $17T_2$ — $3T_1$ — $3T_2$ — $17T_1$ — CORE — 1/2 SECONDARY WINDING 136 TURNS

NOMENCLATURE

TRANSFORMER T

A. MAGNETIC CIRCUIT
FERROXCUBE ---------- { U CORE PT # IF2 / I CORE PT # IF28I
(SAUGERTIES, N.Y.)
MAINTAIN 1/2 MM GAP

B. WINDING DIMENSIONS (SEE FIGURE AT LEFT) ALL WINDINGS WOUND IN SAME DIRECTION.
$3T_1$ - 3 TURNS ENAMEL COPPER WIRE, #23
$17T_1$ - 17 TURNS ENAMEL COPPER WIRE, #18
$17T_2$ - 17 TURNS ENAMEL COPPER WIRE, #18
$3T_2$ - 3 TURNS ENAMEL COPPER WIRE, #23
SECONDARY WINDING 136 + 136 TURNS ENAMEL COPPER WIRE, #26

C. STACKING OF THE WINDINGS ON THE CORE.
THE WINDINGS ARE STACKED ON THE CORE AS SHOWN. THIS WILL MINIMIZE CORE LOSSES AND DECREASE THE HIGH VOLTAGES THAT WILL OCCUR AS A RESULT OF THE SWITCHING OF THE TRANSISTORS.

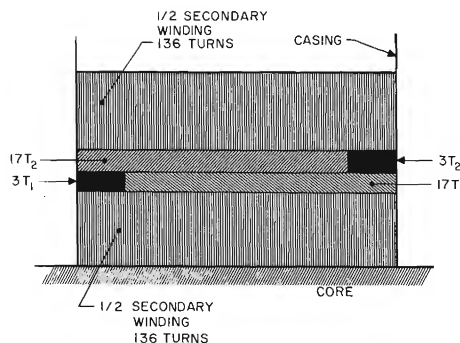
D. INSULATION
APPLY PAPER INSULATION BETWEEN LAYERS
APPLY DOUBLE PAPER INSULATION BETWEEN WINDINGS.

125 WATT DC TO DC CONVERTER

Figure 10.15

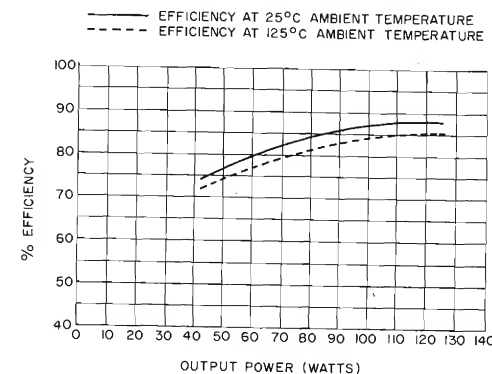
Additional information on circuit performance is shown in Figures 10.16 and 10.17. The power transistors can be mounted on a common heatsink.

EFFICIENCY VS. OUTPUT POWER
(VARIABLE LOAD BETWEEN A AND B)

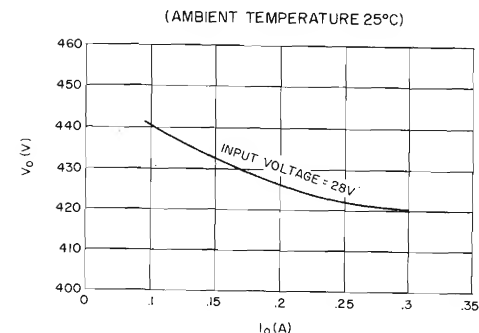
Figure 10.16

OUTPUT VOLTAGE VS. OUTPUT CURRENT FOR CONSTANT INPUT VOLTAGE

Figure 10.17

REFERENCES

(1) Sylvan, T. P., "An Integrated Reference Amplifier for Precision Power Supplies," General Electric Application Note 90.15, Semiconductor Products Department, Syracuse, New York.

NOTES

AUDIO AND HIGH FIDELITY AMPLIFIER CIRCUITS

CHAPTER 11

Part 1 — Audio Amplifier Circuits

BASIC AMPLIFIERS

In this chapter on audio amplifiers a few basic circuit concepts are given in a simplified approach. Approximate circuit design techniques are used, but in most cases the accuracy attained is *practical* because of the production variation in a given transistor parameter for a particular transistor type. Chapter 2 discusses some of the more exact formulas.

SINGLE STAGE AUDIO AMPLIFIER

Figure 11.1 shows a typical single stage audio amplifier using a 2N1414 PNP transistor. With the resistance values shown, the bias conditions on the transistor are 1 ma of collector current and six volts from collector to emitter. At frequencies at which C2 provides good by-passing, the input resistance is given by the formula

$$R_{in} = (1 + h_{fe})\, h_{ib}$$

For the 2N1414, at a *design center* of 1 ma, the input resistance would be 45 × 29, or about 1300 ohms.

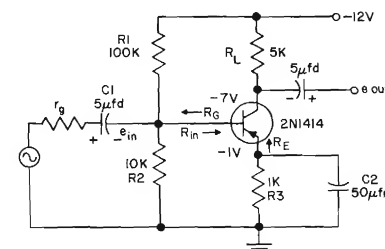



Figure 11.1 SINGLE STAGE AUDIO AMPLIFIER

The ac voltage gain e_{out}/e_{in} is approximately equal to R_L/h_{ib}. For the circuit shown, this would be 5000/29, or approximately 172 (44 db). The low frequency gain will drop 3 db when the reactance of C1 equals $R_{in} + r_g$. This assumes the bias network, R1 and R2, are high impedance compared to R_{in}. Also, the low frequency gain will drop 3 db when the reactance of C2 equals the parallel impedance of R3 and R_E. Where

$$R_E \cong \frac{R_G + h_{ib}}{h_{fe} + 1}$$

and R_G is the parallel impedance of the bias network and generator, r_g. Where the low frequency gain loss is mostly circuit dependant, the high frequency gain loss can be due to transistor characteristics (see Chapter 2).

TWO STAGE RC COUPLED AUDIO AMPLIFIER

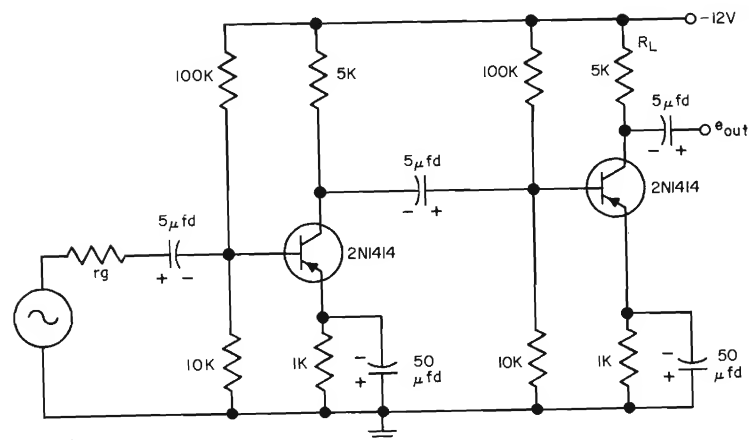
The circuit of a two stage RC coupled amplifier is shown by Figure 11.2. The input impedance is the same as the single stage amplifier and would be approximately 1300 ohms.

TWO STAGE RC COUPLED AUDIO AMPLIFIER

Figure 11.2

The load resistance for the first stage is now the input impedance of the second stage. The voltage gain for the two stage circuit is given approximately by the formula

$$A_v \approx h_{fe} \frac{R_L}{h_{ib}}$$

CLASS B PUSH-PULL OUTPUT STAGES

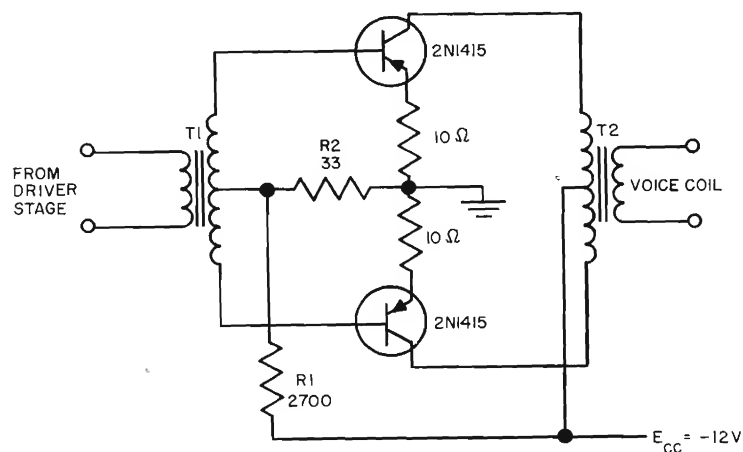
In the majority of applications the output power is specified so a design will usually begin at this point. The circuit of a typical push-pull Class B output stage is shown in Figure 11.3.

CLASS B PUSH-PULL OUTPUT STAGE

Figure 11.3

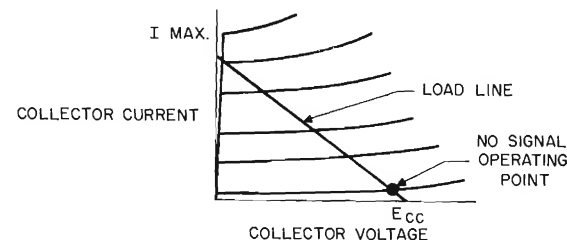
The voltage divider consisting of R1 and R2 gives a slight forward bias of about 0.14 volts on the transistors to prevent cross-over distortion. The 10 ohm resistors in the emitter leads stabilize the transistors so they will not go into thermal runaway when the ambient temperature is less than 55°C. Typical collector characteristics with a load line are shown below.

TYPICAL COLLECTOR CHARACTERISTICS AND LOAD LINE

Figure 11.4

It can be shown that the maximum ac output power without clipping using a push-pull stage is given by the formula

$$P_{out} = \frac{I_{max} \quad V_{CE}}{2}$$

where V_{CE} = collector to emitter voltage at no signal. Since the load resistance is equal to

$$R_L = \frac{V_{CE}}{I_{max}}$$

and the collector-to-collector impedance is four times the load resistance per collector, the output power is given by the formula

$$P_o = \frac{2 V_{CE}^2}{R_{c-c}} \tag{11a}$$

Thus, for a specified output power and collector voltage the collector to collector load resistance can be determined. For output powers in the order of 50 mw to 850 mw the load impedance is so low that it is essentially a short circuit compared to the output impedance of the transistors. Thus, unlike small signal amplifiers, no attempt is made to match the output impedance of transistors in power output stages. The power gain is given by the formula

$$\text{Power Gain} = \frac{P_{out}}{P_{in}} = \frac{I_o^2 \quad R_L}{I_{in}^2 \quad R_{in}}$$

Since I_o/I_{in} is equal to the current gain, beta, for small load resistance, the power gain formula can be written as

$$P.\,G. = \beta^2 \frac{R_{c-c}}{R_{b-b}} \tag{11b}$$

where

R_{c-c} is the collector-to-collector load resistance,

R_{b-b} is the base to base input resistance, and

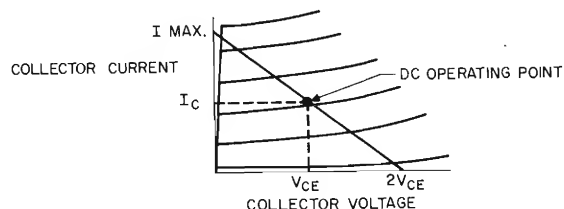
β is the grounded emitter current gain.

Since the load resistance is determined by the required maximum undistorted output power, the power gain can be written in terms of the maximum output power by com-

bining equations (11a) and (11b) to give

$$P.G. = \frac{2\beta^2 V_{CE}^2}{R_{b-b} P_{out}} \qquad (11c)$$

CLASS A OUTPUT STAGES

The Class A output stage is biased as shown on the collector characteristics below

DC OPERATING POINT OF CLASS A AUDIO AMPLIFIER
Figure 11.5

The dc operating point is chosen so that the output signal can swing equally in the positive and negative direction. The maximum output power without clipping is equal to

$$P_{out} = \frac{V_{CE}\ I_c}{2}$$

The load resistance is then given by

$$R_L = \frac{V_{CE}}{I_c}$$

Combining these two equations, the load resistance can be expressed in terms of the collector voltage and power output by

$$R_L = \frac{V_{CE}^2}{2\,P_o} \qquad (11d)$$

For output powers of 20 mw and above the load resistance is very small compared to the transistor output impedance and the current gain of the transistor is essentially the short circuit current gain beta. Thus for a Class A output stage the power gain is given by the formula

$$PG = \frac{\beta^2 R_L}{R_{in}} = \frac{\beta^2 V_{CE}^2}{2\,R_{in} P_o} \qquad (11e)$$

CLASS A DRIVER STAGES

For a required output power of 500 mw the typical gain for a 12 volt push-pull output stage would be in the order of 27 db. Thus the input power to the output stage would be about 1 to 2 mw. The load resistance of a Class A driver stage is then determined by the power that must be furnished to the output stage and this load resistance is given by equation (11d). For output powers in the order of a few milliwatts, the load resistance is not negligible in comparison to the output impedance of the transistors, therefore, more exact equations must be used to determine the power gain of a Class A driver stage. From four-terminal network theory, after making appropriate approximations, it can be shown that the voltage gain is given by

$$A_V = \frac{R_L}{h_{ib} + Z_e} \qquad (11f)$$

where

h_{ib} is the grounded base input impedance, and

Z_e is the external circuit impedance in series with the emitter.

The current gain is given by

$$A_I = \frac{\alpha}{1 - \alpha + R_L h_{ob}} \qquad (11g)$$

where

h_{ob} is the grounded base output conductance

The power gain is the product of the current gain and the voltage gain. Unlike the formula for high power output stages, there is no simple relationship between required output power and power gain for a Class A driver amplifier. Thus the following design charts simplify a circuit design.

DESIGN CHARTS

Figures 11.7 through 11.16 are design charts for determination of transformer impedances and typical power gains for Class A driver stages, Class A output stages, and Class B push-pull stages. The transformer power output charts take into account a transformer efficiency of 75% and therefore may be read directly in terms of power delivered to the loudspeaker. Power gain charts show the ratio of output power in the collector circuit to input power in the base circuit and therefore do not include transformer losses. Since the output transformer loss is included in the one chart, and the design procedure that follows includes the driver transformer loss, it can be seen that the major losses are accounted for.

The charts can best be understood by working through a typical example. Assume a 500 mw output is desired from a 12 volt amplifier consisting of a driver and push-pull output pair. To obtain 500 mw in the loudspeaker, the output pair must develop 500 mw plus the transformer loss.

$$P_{collector\text{-}to\text{-}collector} = \frac{P_{out}}{\text{transformer eff.}} = \frac{500\text{ mw}}{.75} = 666\text{ mw}$$

From Figure 11.11, a pair of 2N1415's in Class B push-pull produce a power gain of approximately 27 db at 666 mw. This is a numerical gain of 500, so the input power required by the output stage is

$$P_{in} = \frac{P_{out}}{\text{Gain}} = \frac{666\text{ mw}}{500} = 1.33\text{ mw}$$

If the driver transformer is 75% efficient, the driver must produce

$$P_{driver} = \frac{\text{P into output stage}}{75\%} = \frac{1.33\text{ mw}}{.75} = 1.8\text{ mw}$$

From Figure 11.16 the 2N322 has a power gain of 42 db at a power output of 1.8 mw.

The output transformer primary impedance is obtained from Figure 11.12 on the 12 volt supply line at 666 mw output, and is 340 ohms maximum collector to collector load resistance. Therefore, a more standard 300 ohm center tap (CT) output transformer may be used with secondary impedance to match the load. From Figure 11.13 the driver transformer primary impedance is 20,000 ohms. The secondary must be center tapped with a total impedance of 800 to 5000 ohms. When this procedure is used for commercial designs, it must be remembered that it represents full battery voltage, typical power gain and input impedance, and therefore does not account for end-limit points. Figure 11.6 is a circuit that uses the above design calculations. The input sensitivity is between 10 and 20 millivolts for ½ watt output.

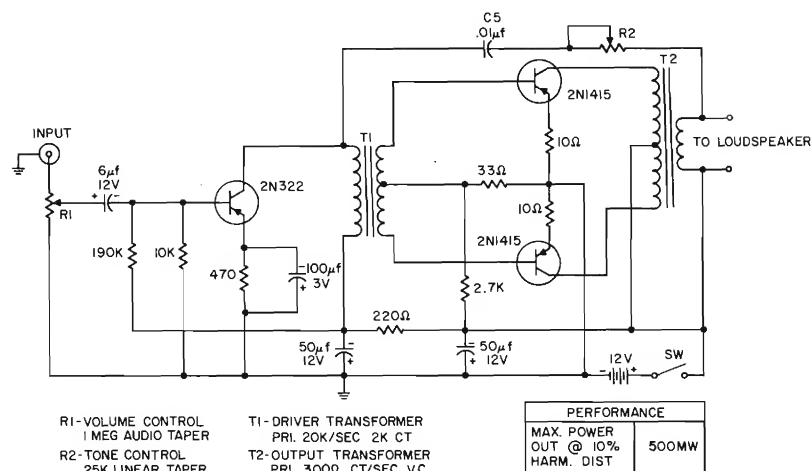
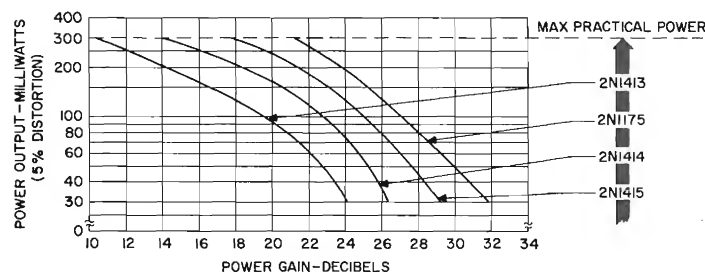
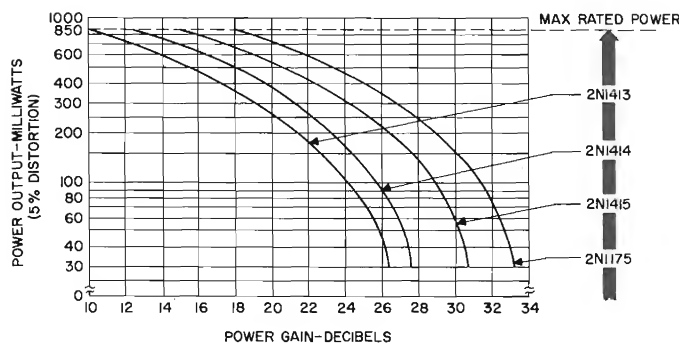
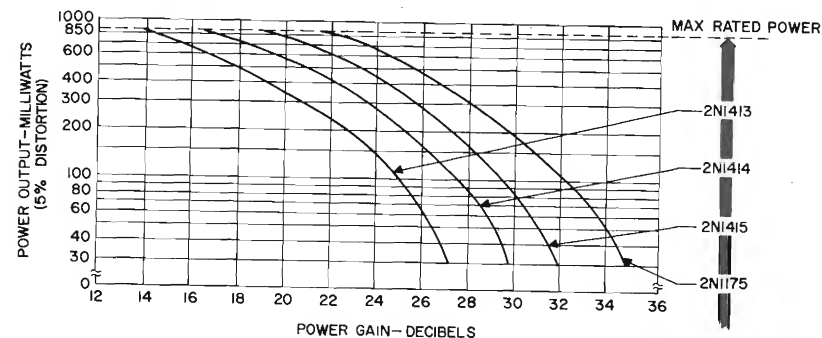
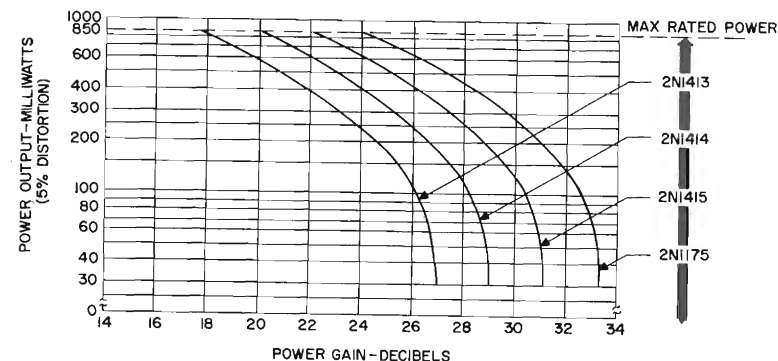
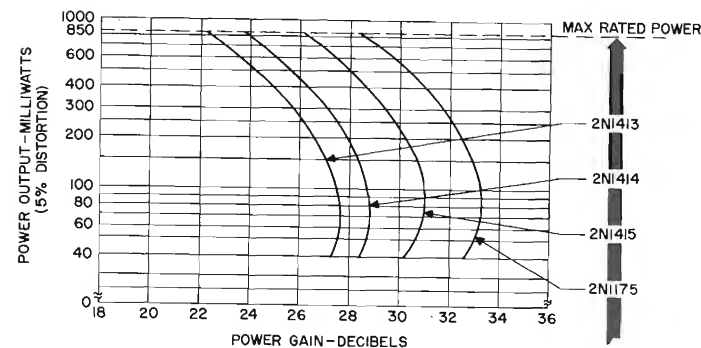
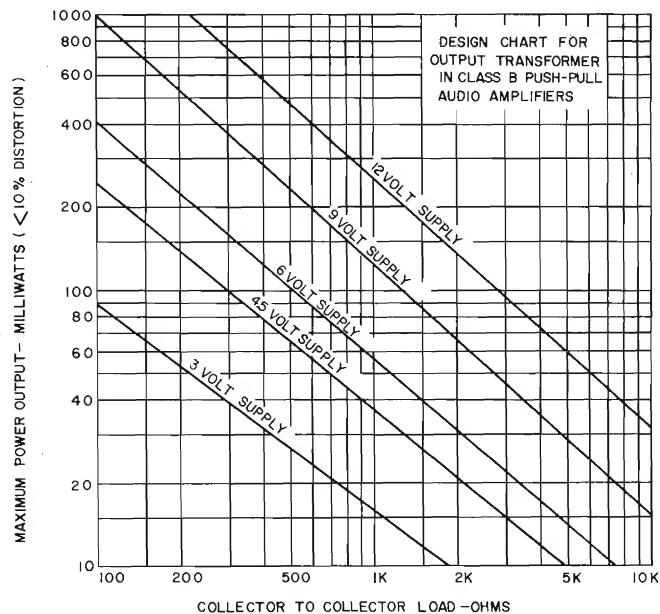
PERFORMANCE	
MAX. POWER OUT @ 10% HARM. DIST	500MW

12 VOLT AUDIO AMPLIFIER **Figure 11.6**

TYPICAL POWER GAIN FOR CLASS B PUSH-PULL AMPLIFIERS, 3.0 VOLT SUPPLY
Figure 11.7

TYPICAL POWER GAIN FOR CLASS B PUSH-PULL AMPLIFIERS, 4.5 VOLT SUPPLY
Figure 11.8

TYPICAL POWER GAIN FOR CLASS B PUSH-PULL AMPLIFIERS, 6 VOLT SUPPLY
Figure 11.9

TYPICAL POWER GAIN FOR CLASS B PUSH-PULL AMPLIFIERS, 9 VOLT SUPPLY
Figure 11.10

TYPICAL POWER GAIN FOR CLASS B PUSH-PULL AMPLIFIERS, 12 VOLT SUPPLY
Figure 11.11

DESIGN CHART FOR OUTPUT TRANSFORMER IN CLASS B PUSH-PULL AUDIO AMPLIFIERS

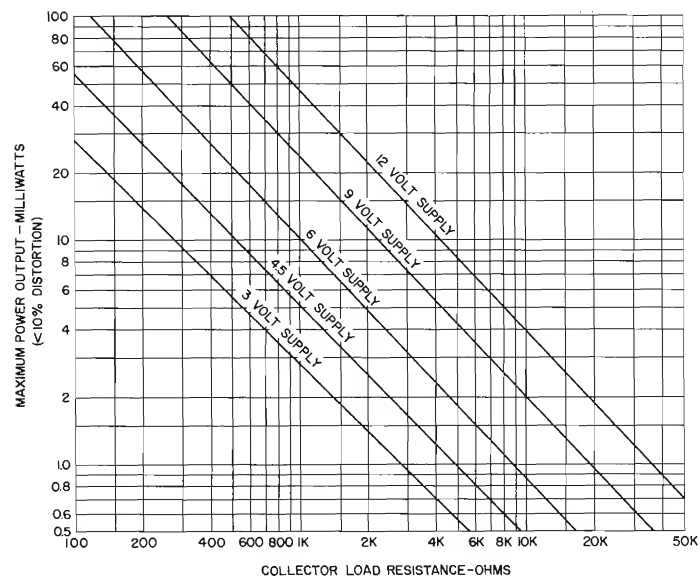
Figure 11.12

DESIGN CHART FOR OUTPUT TRANSFORMER IN CLASS A SINGLE-ENDED AMPLIFIER

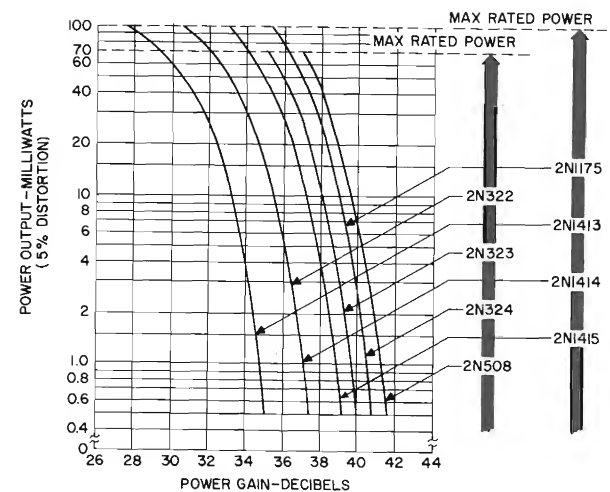
Figure 11.13

TYPICAL POWER GAIN FOR CLASS A SINGLE-ENDED AMPLIFIERS, 6 VOLT SUPPLY

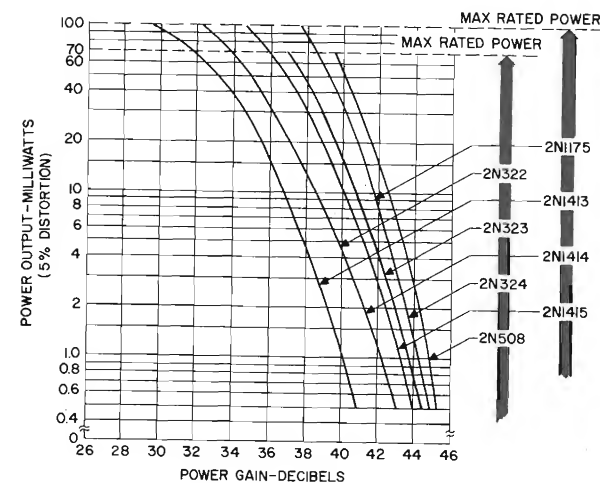
Figure 11.14

TYPICAL POWER GAIN FOR CLASS A SINGLE-ENDED AMPLIFIERS, 9 VOLT SUPPLY

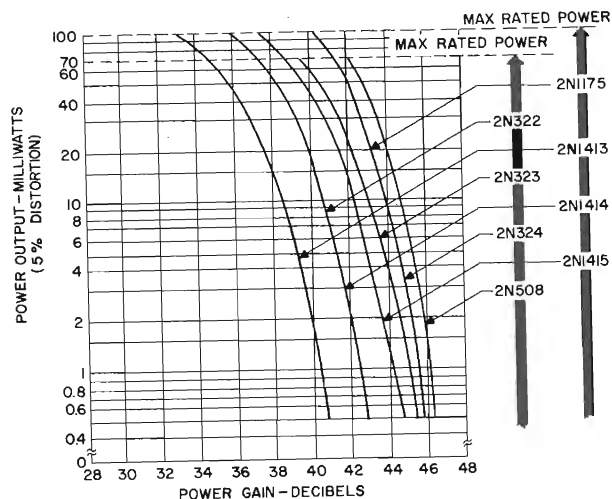
Figure 11.15

TYPICAL POWER GAIN FOR CLASS A SINGLE-ENDED AMPLIFIERS, 12 VOLT SUPPLY

Figure 11.16

TRANSISTORS LISTED IN THE TOP ROW ARE PREFERRED TYPES. THEY CAN BE SUBSTITUTED FOR TYPES LISTED BELOW THEM IN THE SAME COLUMN. BRACKETED TYPES ARE NOT RECOMMENDED FOR NEW DESIGNS.

* 2N322	* 2N323	* 2N324	* 2N508	2N1413	2N1414	2N1415	2N1175
(2N190)	(2N191)	(2N192)	(2N265)	(2N187A) (2N189) 2N319	(2N188A) (2N190) 2N320 2N322	(2N241A) (2N191) 2N321 2N323	(2N192) 2N324

* THESE TYPES CAN NOT BE SUBSTITUTED IF APPLICATION REQUIRES $V_{CER} > 16$ VOLTS

PREFERRED TYPES AND SUBSTITUTION CHART

Figure 11.17

Part 2 – High Fidelity Circuits

INTRODUCTION

Transistors are ideally suited for high fidelity amplifiers since there is no problem with microphonics or hum pick-up from filaments as there is with tubes. Transistors are inherently low impedance devices and thus offer better matching to magnetic pick-ups and loudspeakers for more efficient power transfer.

Transistor circuits with negative feedback can give the wide frequency response and low distortion required for high fidelity equipment. In general, the distortion reduction is about equal to the gain reduction for the circuit to which negative feedback is applied. The input and output impedances of amplifiers with feedback are either increased or decreased, depending on the form of feedback used. Voltage feedback

from the collector, over one or several transistor stages, decreases the output impedance of that stage; whereas current feedback from the emitter increases the output impedance of the stage. If either of these networks are fed back to the base of a transistor the input impedance is decreased, but if the feedback is to the emitter then the impedance is increased. The feedback can be applied to the emitter for effective operation with a low generator impedance, whereas the feedback to the base is effective with a high impedance (constant current) source. If the source impedance is low in the latter case then most of the feedback current would flow into the source and not into the feedback amplifier. The feedback connections must be chosen to give a feedback signal that is out-of-phase with the input signal if applied to the base, or in-phase if it is applied to the emitter of a common-emitter stage.

Care must be used in applying feedback around more than two transistor stages to prevent high frequency instability. This instability results when the phase shift through the transistor amplifiers is sufficient to change the feedback from negative to positive. The frequency response of the feedback loop is sometimes limited to stabilize the circuit. At the present time the amount of feedback that can be applied to some audio power transistors is limited because of the poor frequency response in the common-emitter and common-collector connections. The common-collector connection offers the advantage of local voltage feedback that is inherent with this connection. *Local* feedback (one stage only) can be used on high phase shift amplifiers to increase the frequency response and decrease distortion.

PREAMPLIFIERS

Preamplifiers have two major functions: increasing the signal level from a pickup device to about 1 volt rms; and providing compensation, if required, to equalize the input signal for a constant output with frequency.

The circuit of Figure 11.18 meets these requirements when the pickup device is a magnetic microphone, phono cartridge (monaural or stereo), or a tape head. The total harmonic or IM (intermodulation) distortion of the preamp is less than 0.3% at reference level output (1 volt).

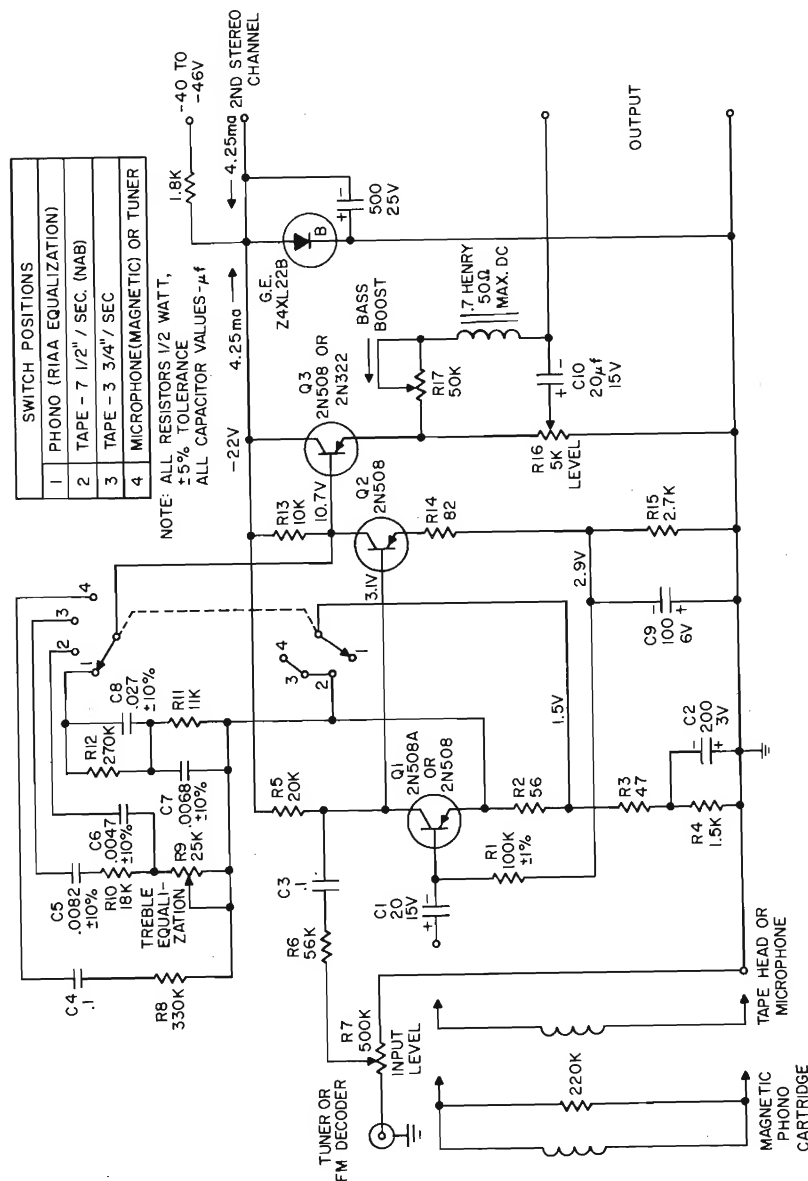
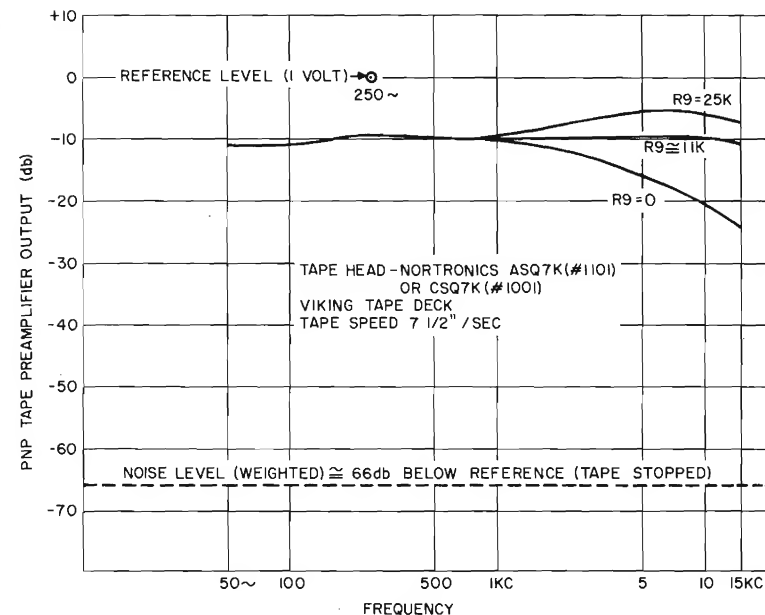
This preamp will accommodate most magnetic pickup impedances. Input impedance to the preamp increases with frequency (except in switch pos. #4) because of the frequency selective negative feedback to the emitter of Q1. The impedance of the magnetic pickups will also increase with frequency but are below that of the preamp.

The first two stages of this circuit have a feedback bias arrangement with R1 feeding bias current to the base of Q1 that is directly proportional to the emitter current of Q2. This stabilizes the voltage and current bias points in the circuit for variations in both h_{FE} of the 2N508 and ambient temperatures up to 55°C (131°F). The output stage is well stabilized with a 5K emitter resistance.

The ac negative feedback from the collector of Q2 to the emitter of Q1 is frequency selective to compensate for the standard NAB recording characteristic for tape or the standard RIAA for phonograph records. The flat response from a standard NAB recorded tape occurs with the treble control (R9) near mid-position (see Figure 11.19). There is about 5 db of treble boost with the control at 25K and approximately 12 db of treble cut with R9 = 0. Mid-position of the treble control also gives flat response from a 3¾"/second tape. This treble equalization permits adjustment for variations in program material, tap heads, and loudspeakers.

The 0.36 henry tape head gives an equalized response within ±1 db variation from 50 cycles to 15 kc (see Figure 11.19). Noise level is 66 db below reference level output with a weighted measurement. The unweighted noise level is 57 db below reference. Measurement of unweighted noise even in the audio range (16 cps to 20 kc)

SWITCH POSITIONS	
1	PHONO (RIAA EQUALIZATION)
2	TAPE - 7 1/2" / SEC. (NAB)
3	TAPE - 3 3/4"/ SEC
4	MICROPHONE(MAGNETIC) OR TUNER

NOTE: ALL RESISTORS 1/2 WATT, ±5% TOLERANCE
ALL CAPACITOR VALUES-μf

PHONO, TAPE, MICROPHONE PREAMPLIFIER
Figure 11.18

TAPE PREAMPLIFIER RESPONSE FROM NAB RECORDING
Figure 11.19

does not give results that correlate with the low level audible noise as heard from a speaker. For measurement of low level noise, a filter can be used with a response that follows the Fletcher-Munson curve of equal loudness at a level of 40 db above the threshold of hearing at 1 kc. This response falls within the ASA standard "A" weighting curve.(1)

A good signal-to-noise ratio (S/N) can be realized with a tape head inductance between 0.2 and 0.5 henry. One has to be careful of the physical position of the tape head or the noise output will increase considerably due to pick-up of stray fields. For good S/N it is important that the tape head have good shielding and hum bucking. The S/N and dynamic range is improved by R14 in the emitter of Q2 which reflects a higher input impedance for this stage and thus increases the gain of Q1. The preamp performance with a Nortronics B2Q7K, or F, head will be similar to Figure 11.19 with the preamp output level increased about 2 db.

The preamp in the #2 (Tape 7½"/sec.) position requires about 1.5 mv input signal at 1 kc for 1 volt output. Therefore a tape head with a 1 kc reference level output of 1.2 to 2 mv is desirable. Maximum output of the preamp before clipping is over 14 db above the 1 volt reference output level.

In switch position #3 (Tape 3¾"/sec.) with $R9 + R10 = 30K$, the equalized response is within ±1 db from 50 cycles to 7½ kc with Ampex Standard Alignment Tape #6000-A4 and Nortronics ASQ7K tape head. The preamp reference level output is 0.55 volts and the noise (weighted) is 56 db below this level.

The voltage feedback from the collector of Q2 decreases at lower frequencies because of the increasing reactance of the feedback capacitor in series with the treble control. In switch position #4 the capacitor C4 is large enough with R8 to make the voltage feedback, and thus the gain, constant across the audio spectrum. This flat

preamp response can be used with a tuner, FM decoder or microphone. The input impedance to the preamp in #4 switch position is about 4.5K ohms, and 350 microvolts input level gives 1 volt output (69 db gain). This sensitivity and input impedance gives excellent performance with low and medium impedance magnetic microphones. The noise (weighted) is 64 db below the 1 volt output level. A magnetic pickup should be left connected at the preamp input while using the tuner or FM decoder. This tuner input has a sensitivity down to 250 millivolts.

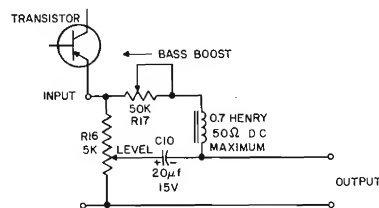
The RIAA feedback network (switch position #1) has a capacitor C7 for decreasing the amplifier gain at the higher frequencies. This eliminates the need to load a magnetic cartridge with the proper resistance for high frequency compensation. An input level of 8 millivolts gives 1 volt output, and the preamp output noise (unweighted) is 78 db below this level. The equalized output is within ±1 db variation from 40 cycles to 12 kc using the London PS-131 stereophonic frequency test record and a Shure M77 Stereo Dynetic pickup cartridge.

Generally, the manufacturer of a piezoelectric pickup often has a recommended network for converting his pickup to a velocity device, so that it may be fed into an input jack intended for a magnetic pickup.

The emitter-follower output stage of the preamp gives a low impedance output for a cable run to a power amplifier (transistor or tube), and acts as a buffer so that any loading on the preamp will not affect the equalization characteristic. The preamp output should not be loaded with less than 3K ohms and preferably about 10K or greater.

Since this is a high gain circuit care should be used in the physical layout to prevent regenerative feedback to the input. Also, a switching circuit at the input will increase the possibilities for hum pickup and thus decrease the S/N. All connections to the base of Q1 should be very short, or shielded. A 22½ volt battery can be used to power this preamp circuit with good battery life since total load current is only 4.25 ma. The treble control should have a linear taper and the level control an audio taper.

BASS BOOST OR LOUDNESS CONTROL CIRCUIT

The bass boost circuit of Figure 11.20 operates on the output of the preamp (Figures 11.18, 11.22). With this addition, the operator has the necessary treble and bass control to compensate for listening levels, or deficiencies in program material, pickup, speakers, etc. This bass boost circuit gives the operator independent control of the level, or amount of bass boost desired, or the level control can be used as a loudness control.

BASS BOOST OR LOUDNESS CONTROL CIRCUIT
Figure 11.20

It is usually desirable to have some method of boosting the level of the lower portion of the audio spectrum as the overall sound level is decreased. This is to compensate for the non-linear response of the human ear as shown in the Fletcher-Munson curves that are often referred to in the audio industry. The ear requires a higher level for the low frequency sound to be audible as the frequency is decreased and also as the overall spectrum level is decreased.

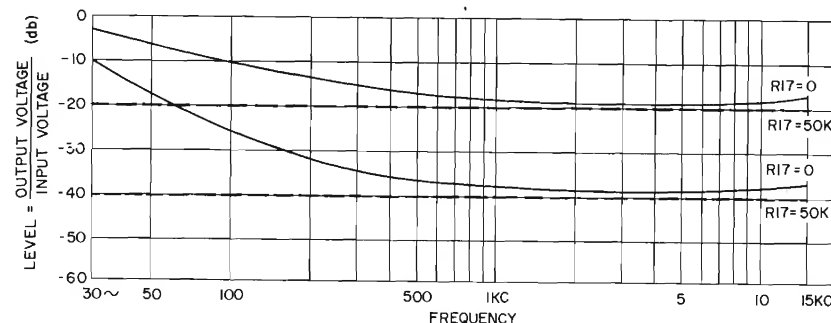
Figure 11.21 shows the frequency characteristics of this bass boost circuit. With the level control set for zero attenuation at the output there is no bass boost available, but as the output level is attenuated the available bass boost increases.

FREQUENCY RESPONSE OF BASS BOOST CIRCUIT
Figure 11.21

Figure 11.21 shows the frequency response (lower dashed curve) when the output is attenuated 40 db and the bass boost control is set for minimum (50K ohms). The solid curve immediately above represents the frequency response when the bass boost control is set at maximum (zero ohms). Thus, a frequency of 30 cycles can have anything from zero to 27 db of boost with respect to 1 kc, depending on the adjustment of the bass boost control.

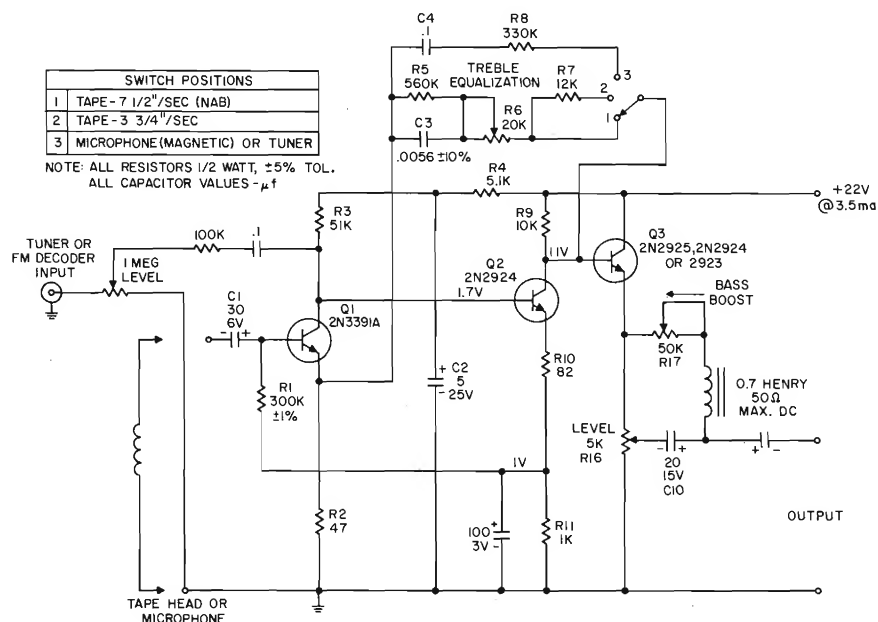
The Fletcher-Munson contours of equal loudness level show most of the contour changes involve a considerable boost of the bass frequencies at the lower levels of intensity. Therefore, this circuit combination fulfills the requirements of level control, bass boost, and loudness control.

When using R17 as a loudness control, set it at 50K and adjust the level control, R16, so that the program material sounds as loud as the original and adjust the treble equalization (Figure 11.18 and 11.22) for proper tone balance. Now the program level can be reduced to the desired listening level and R17 adjusted for the same acoustical bass response. With R17 set for maximum bass boost and the level control at −40 db output, the frequency response as shown in Figure 11.21 is within about 2 db of the 55 phon curve of equal loudness as given by Fletcher and Munson below 1 kc. Forty decibals higher intensity level at 1 kc would be at the 95 phon curve of equal loudness. This is near the maximum level of very loud music peaks while a 55 phon level is representative of background music level.

The bass boost control may be a standard 50K potentiometer with a linear taper. The desired inductance may be obtained by using the green and yellow leads on the secondary of an Argonne transistor transformer #AR-128 (Lafayette Radio Catalog).

NPN-TAPE AND MICROPHONE PREAMPLIFIER

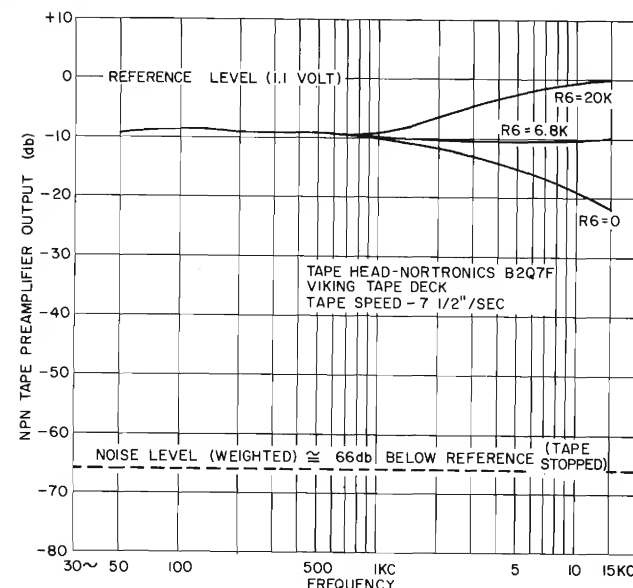
The basic preamplifier of Figure 11.22 is similar to that of Figure 11.18 except silicon planar NPN transistors are used and thus the first stage does not require a temperature compensating resistor in the emitter circuit. Since Q1 is a planar passivated transistor which has very low leakage current (I_{CBO}), the bias current can be

reduced. Approximately 0.35 ma of collector current for Q1 gives the best signal-to-noise ratio (S/N). R4 and C2 provide ripple reduction in the supply to the first stage. This preamp has higher open loop gain than the preamp in Figure 11.18 and thus R5 is required for NAB equalization at 50 cycles.

TAPE-MICROPHONE PREAMPLIFIER
Figure 11.22

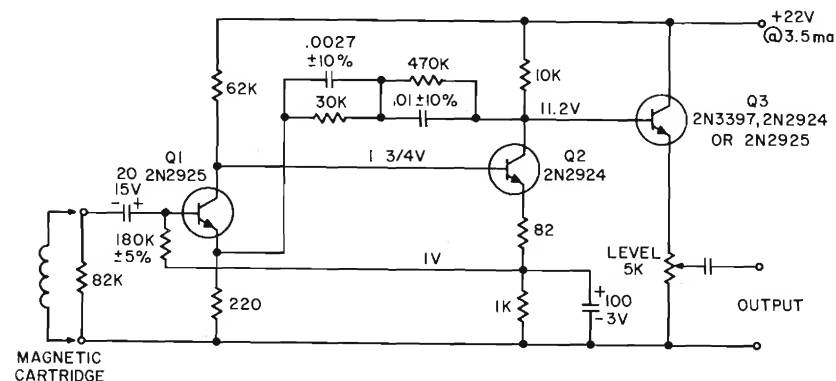
The 0.4 henry tape head gives an equalized response within ±1 db variation from 50 cycles to 15 kc (see Figure 11.23). Noise level is approximately 66 db below reference level output with a weighted measurement, and 57 db unweighted. The equalized response is equally good with a Nortronics B2Q7K or ASQ7K tape head.

The preamp in switch position #1 (Tape 7½"/sec.) requires 1.8 mv input signal at 1 kc for 1.1 volts output. This level is about 14 db below maximum output. The IM distortion is less than 0.25% at 1.1 volts output (reference level). The input impedance at 1 kc is over 100K and approximately 43K at 15 kc. This high input impedance along with the treble equalization adjustment accommodates tape head impedances to 0.8 henry. The optimum output level of the tape head for best dynamic range and S/N is a 1 kc reference level of 1.8 mv ±3 db.

In switch position #2 (Tape 3¾"/sec.) with R6 + R7 = 22K, the equalized response is within ±1.25 db from 50 cycles to 7½ kc with Ampex standard alignment tape #6000-A4 and Nortronics B2Q7F tape head. The preamp reference level output is 1.18 volts which is 57 db above the weighted noise level.

In switch position #3, the flat preamp response can be used with a tuner, FM decoder, or magnetic microphone. The microphone preamp input impedance is 43K, and a 400 microvolts input signal gives 1.2 volts output (70 db gain). This output level is 14 db below maximum, and is 62 db above the weighted noise level. The

TAPE PREAMPLIFIER RESPONSE FROM NAB RECORDING
Figure 11.23

frequency response is flat within 0.25 db from 30 cycles to 15 kc and the total harmonic distortion is 0.01% at 1.2 volts output. The tape head or a 200 ohm resistor should be connected at the preamp input while using the tuner or FM decoder. This tuner input has a sensitivity down to 260 millivolts.

A large capacitor value for C1 is desirable to keep the impedance low at the base of Q1 for best S/N performance. All connections to the base of Q1 should be very short, or shielded. Since this basic preamp is quite similar to the circuit in Figure 11.18, the previous detailed discussion applies also to this NPN preamp.

PHONO (RIAA) PREAMPLIFIER
Figure 11.24

NPN-PHONO PREAMPLIFIERS

The circuit of Figure 11.24 is designed for a magnetic phono cartridge and is quite similar to the basic circuit of Figure 11.22. An input signal of 6 millivolts at 1 kc gives 1 volt output which is 15 db below the clipping level and 72 db above the unweighted noise level. The RIAA equalized output is within ±1 db variation from 40 cycles to 12 kc using the London PS 131 stereophonic frequency test record and a Shure M77 Stereo Dynetic cartridge. The input impedance at 1 kc is 43K. The total harmonic distortion at 1 kc is 0.15% at 1 volt output.

The circuit of Figure 11.25 gives an RIAA equalized output when used with ceramic cartridges that have 5,000 to 10,000 pf capacitance. The input impedance is approximately 620K at 50 cycles. With the Astatic Model 137 cartridge the output reference level of 1 volt is 13 db below maximum output and 69 db above the unweighted noise level. The total harmonic distortion is less than 0.6% at the 1 volt output level. R3 and R4 with the .01 capacitor give the 500 and 2,122 cycle turnover points for RIAA equalization.

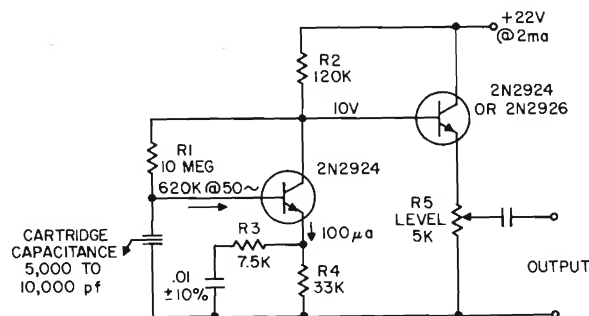
The circuit of Figure 11.26 gives an RIAA equalized output when used with ceramic cartridges that have 1,000 to 10,000 pf capacitance. Here the feedback

PHONO PREAMPLIFIER FOR CERAMIC CARTRIDGE
(AMPLITUDE RESPONSE — RIAA EQUALIZATION)

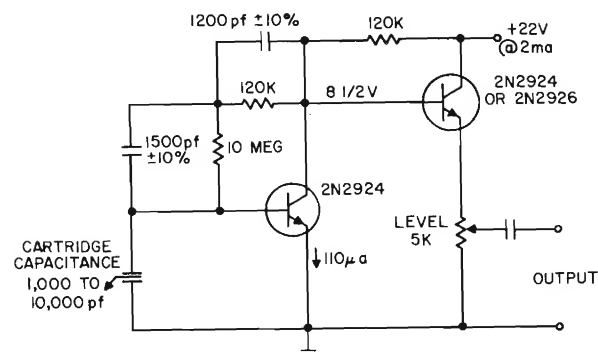
Figure 11.25

PHONO PREAMPLIFIER FOR CERAMIC CARTRIDGE
(VELOCITY RESPONSE — RIAA EQUALIZATION)

Figure 11.26

equalization is from collector to base which lowers the input impedance. This has the advantage of accepting a wide range of cartridge capacitance. It is also less susceptible to cable capacitance and noise pickup. The input impedance, which is about 30K at 40 cycles, decreases with increasing frequency. This results in a velocity response from the cartridge and thus the preamp frequency response is like that required for a magnetic cartridge.

Using the Astatic 137 cartridge (7,800 pf) and the London PS 131 stereophonic frequency test record the output is equalized within ±1.6 db from 40 cycles to 12 kc. The output reference level is 1¼ volts which is 14 db below clipping, and 70 db above the unweighted noise level. The 1 kc total harmonic distortion is less than 0.1% at 1¼ volts output.

Using the Astatic 17 cartridge (1,000 pf), the preamp output is equalized within ±1.6 db also, but at about 10 db lower level.

POWER AMPLIFIERS

It is difficult to attain faithful reproduction of a square wave signal with a transformer amplifier. A high quality transformer is required and it must be physically large to have a good response at the low frequencies. Thus, a great deal of effort has gone into developing transformerless push-pull amplifiers using vacuum tubes. Practical circuits, however, use many power tubes in parallel to provide the high currents necessary for direct-coupling to a low impedance load such as loudspeakers.

The advent of power transistors has sparked new interest in the development of transformerless circuits since the transistors are basically low voltage, high current devices. The emitter-follower stage, in particular, offers the most interesting possibilities since it has low inherent distortion and low output impedance.

Figure 11.27 is a direct-coupled power amplifier with excellent low frequency response, and also has the advantage of dc feedback for temperature stabilization of all stages. This feedback system stabilizes the voltage division across the power output transistors Q4 and Q5 which operate in a single-ended Class B push-pull arrangement. Q2 and Q3 also operate Class B in the Darlington connection to increase the current gain. Using an NPN for Q3 gives the required phase inversion for driving Q5 and also has the advantage of push-pull emitter-follower operation from the output of Q1 to the load. Emitter-follower operation has lower inherent distortion and low output impedance because of the 100% voltage feedback.

Q4 and Q5 have a small forward bias of 10 to 20 ma to minimize cross-over distortion and it also operates the output transistors in a more favorable beta range. This bias is set by the voltage drop across the 390 ohm resistors that shunt the input to Q4 and Q5. Q2 and Q3 are biased at about 1 ma (to minimize cross-over distortion) with the voltage drop across the silicon diode (D1). Junction diodes have a temperature characteristic similar to the emitter-base junction of a transistor. Therefore, this diode also gives compensation for the temperature variation of the emitter-base resistance of Q2, Q4 and Q3. These resistances decrease with increasing temperature, thus the decrease in forward voltage drop of approximately 2 millivolts/degree centigrade of the diode provides some temperature compensation.

Q1 is a Class A driver with an emitter current of about 3 ma. Negative feedback to the base of Q1 lowers the input impedance of this stage and thus requires a source impedance that is higher so the feedback current will flow into the amplifier rather than into the source. Resistor R1 limits the minimum value of source impedance. The value of R3 permits about one-half the supply voltage across Q5.

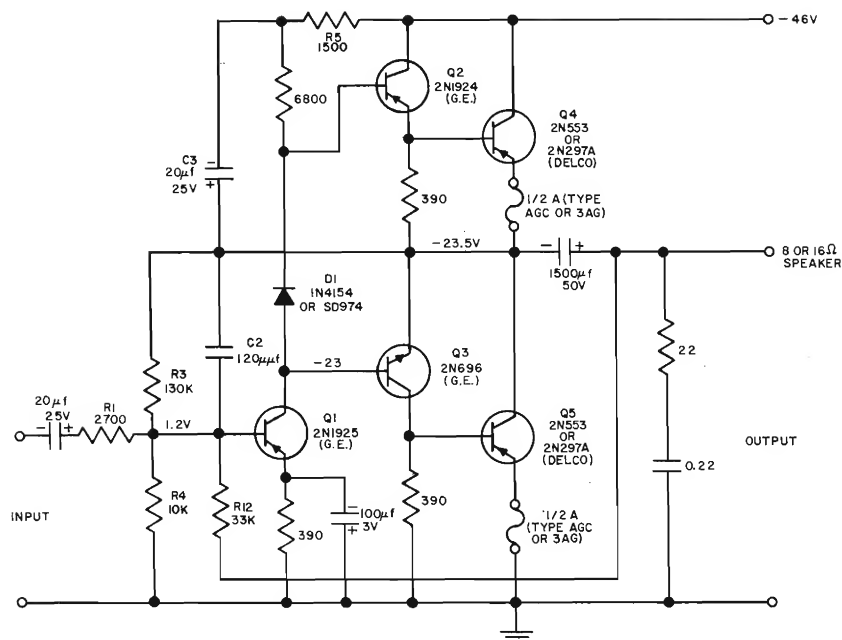
About 11 db of positive feedback is applied by way of C3 across R5. This bootstrapping action helps to compensate for the unsymmetrical output circuit and permits the positive peak signal swing to approach the amplitude of the negative peak. This

10 WATT AMPLIFIER

Figure 11.27

positive feedback is offset by about the same magnitude of negative feedback via R3 to the base of Q1. The net amount of negative feedback is approximately 14 db resulting from R12 connecting the output to the input. In addition, there is the local feedback inherent in the emitter-follower stages. The value for the C2 feedback capacitor was chosen for optimum square wave response (i.e., maximum rise-time and minimum overshoot).

A ½ ampere fuse is used in the emitter of each output transistor for protective fusing of Q4 and Q5, and also to provide local feedback since the ½ ampere type AGC or 3AG fuse has about 1 ohm dc resistance. This local feedback increases the bias stability of the circuit and also improves the declining frequency response of Q4 and Q5 at the upper end of the audio spectrum. Because of the lower transistor efficiency above 10 kc, care should be used when checking the amplifier for maximum continuous sinewave output at these frequencies. If continuous power is applied for more than a short duration, sufficient heating may result to raise the transistor current enough to blow the ½ ampere fuses. Since there is not sufficient sustained high frequency power in regular program material to raise the current to this level, actual performance of the amplifier does not suffer since the power level in music and speech declines as the frequency increases beyond about 1 to 2 kc.

The speaker system is shunted by 22 ohms in series with 0.22 μfd to prevent the continued rise of the amplifier load impedance and its accompanying phase shift beyond the audio spectrum.

The overall result, from using direct-coupling, no transformers, and ample degeneration, is an amplifier with output impedance of about 1 ohm for good speaker damping, low distortion, and good bandwidth. The power response at 1 watt is flat

from 30 cycles to 15 kc and is down 3 db at 50 kc. At this level the total harmonic and IM distortion are both less than 1%. At 7 watts the IM distortion is less than 2½% and the total harmonic distortion is less than 1% measured at 50 cycles, 1 kc, and 10 kc. The performance of the amplifier of Figure 11.27 is about equal for both 8 and 16 ohm loads.

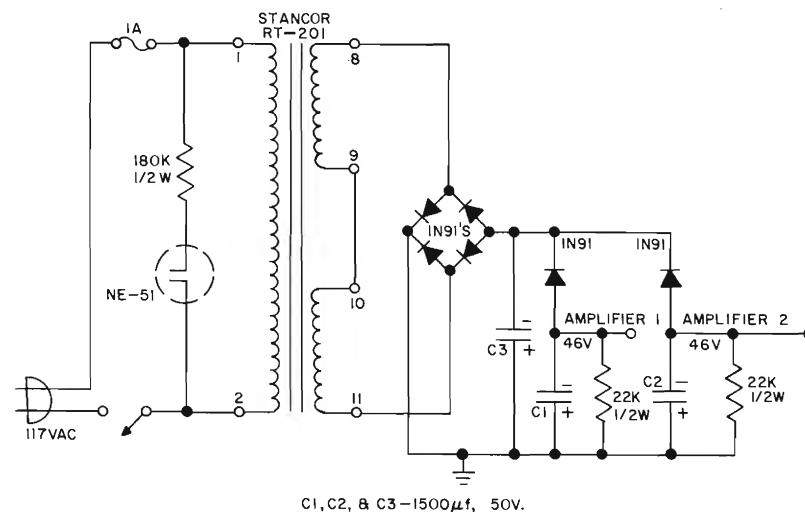
This amplifier is capable of about 8 watts of continuous output power with 1 volt rms input, or 10 watts of music power into 8 or 16 ohms when used with the power supply of Figure 11.28. This power supply has diode decoupling which provides excellent separation (80 db) between the two stereo amplifier channels.

POWER SUPPLY FOR STEREO SYSTEM

Figure 11.28

The power transistors Q4 and Q5 should each be mounted on an adequate heat radiator such as used for transistor output in an automobile radio, or mounted on a 3" x 3" x 3/32" aluminum plate that is insulated from the chassis.

SILICON POWER AMPLIFIERS

Some of the transistor power amplifiers to date have been lacking in their high frequency performance and their temperature stability. The diffused silicon transistors permit good circuit performance at high frequency. Silicon transistors are desirable for power output stages because of their ability to perform at much higher junction temperatures than germanium. This means smaller heat radiating fins can be used for the same power dissipation. On the negative side, silicon often has higher saturation resistance which gives decreased operating efficiency that becomes appreciable when operating from low voltage supplies.

The power handling capability of a transistor is limited by both its electrical and thermal ratings. The electrical rating limit is a function of the transistor's voltage capability, and its maximum current at which the current gain is still usable. The thermal rating is limited by the transistor's maximum junction temperature. Therefore, it is desirable to provide the lowest thermal impedance path that is practical from junction to air. The thermal impedance from junction to case is fixed by the design

of the transistor; thus it is advantageous to achieve a low thermal impedance from case to the ambient air.

The GE 7A31, 2N2107, and 2N2196 are NPN diffused silicon transistors. They will be limited in their maximum power handling ability by the thermal considerations for many applications unless an efficient thermal path is provided from case to air.

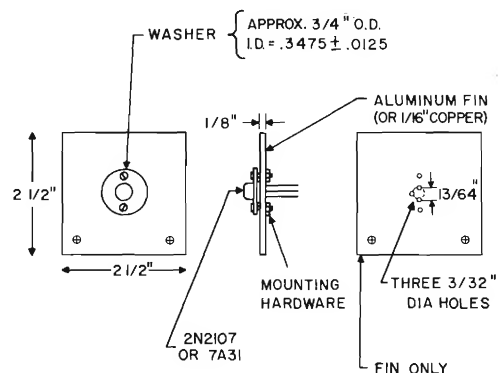
These transistors are constructed with the silicon pellet mounted directly on the metal header, and it is therefore more efficient to have an external heat radiator in direct contact with this header than to make contact with the cap of the transistor package.

TRANSISTOR HEAT RADIATOR

Figure 11.29

Figure 11.29 shows a practical method for achieving a maximum area of direct contact between the metal header and an aluminum fin for efficient heat transfer to the surrounding air. A plain washer with two holes drilled for the mounting hardware is simple but quite adequate for securing the transistor header to the fin. Since air is a relatively poor thermal conductor, the thermal transfer can be improved by applying a thin layer of GE Silicone Dielectric Grease #SS-4005 or equivalent between the transistor and the radiating fin before assembly. The fin may be anodized or flat paint may be used to cover all the surface except for the area of direct contact with the transistor header. An anodized finish would provide the insulation needed between the base and emitter leads and the sides of the feed-through holes in the aluminum fin. Figure 11.30 shows a thermal rating for the 2N2107 and 7A31 as assembled on the radiating fin. An efficient commercial version of the heat radiator shown in Figure 11.30 is available in the IERC #LP5C1B (IERC, 135 W. Magnolia Blvd., Burbank, California).

8 Watt Transformerless Amplifier

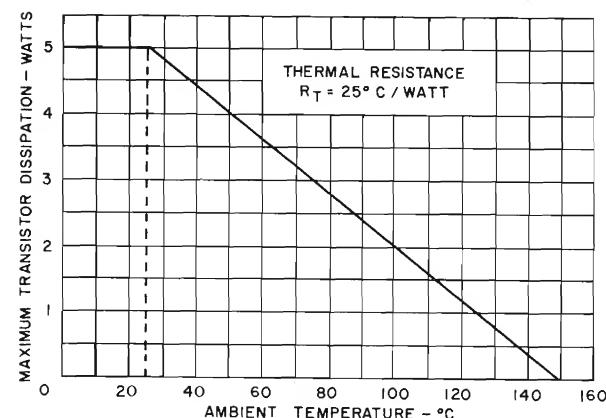
The circuit of Figure 11.31 is very much like that described for Figure 11.27. Opposite polarity is used for transistors, capacitors, and supply voltage. The 1N91 in the emitter circuit of Q4 stabilizes the push-pull output stage for variations in transistor beta and temperature. The fuse, F1, in the emitter circuit of Q4 gives protective fusing for Q4 and Q5, and also its 1 ohm dc resistance gives increased circuit stability. The voltage drop across forward biased diodes, D1 and D2, sets the quiescent current level for the circuit and also adds to the temperature stability as mentioned for Figure 11.27.

THERMAL CHARACTERISTIC

Figure 11.30

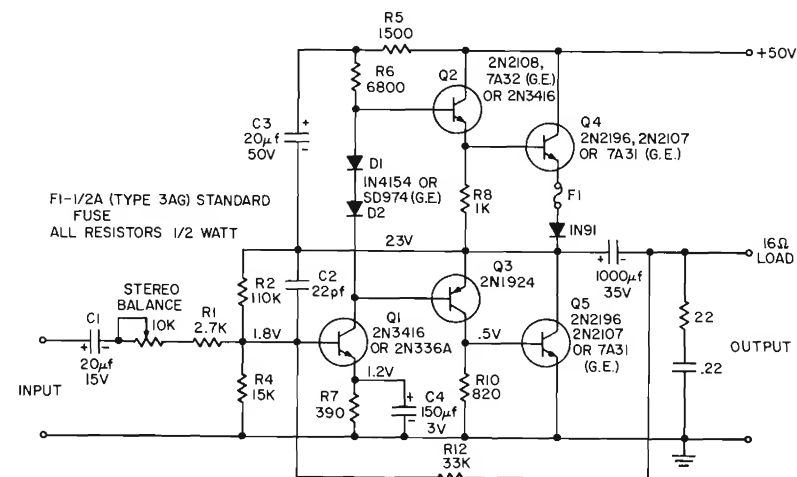
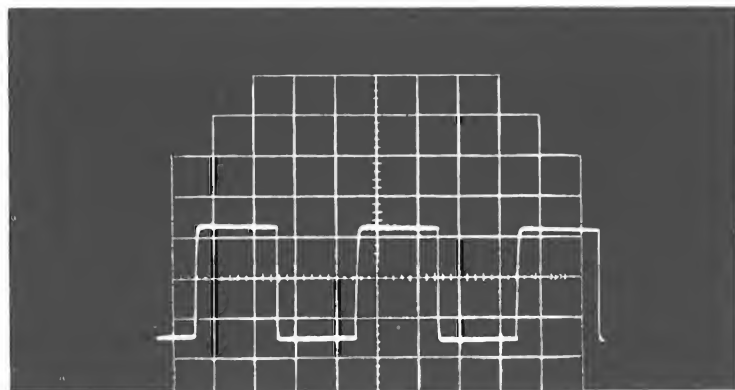
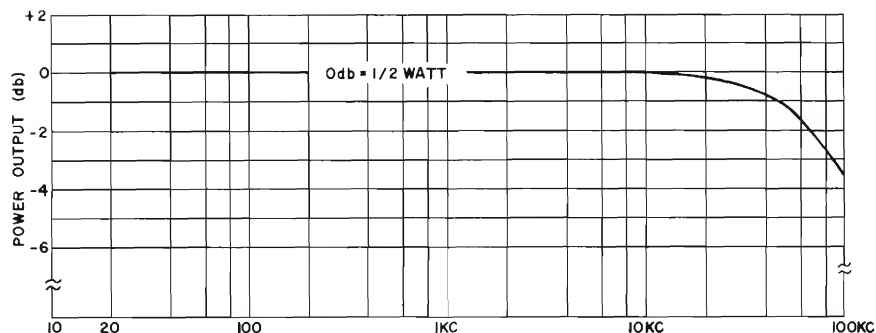
The silicon power amplifier of Figure 11.31 has an output impedance of 0.5 ohm for good speaker damping. There is about 20 db of overall negative feedback with R12 connecting the output to the input. The rise-time and fall-time for a square pulse is less than 2 microseconds. The square wave response shown in Figure 11.32 is indicative of an amplifier with good transient response as well as good bandwidth. The bandwidth is confirmed by the response curve of Figure 11.33 where it is —3 db at 86 kc. Power response at 6 watts output is flat within ⅓ db from 30 cycles to 15 kc. The amplifier exhibits good recovery from overload, and the square wave peak power output without distorting the waveform is 12 watts.

8 WATT AMPLIFIER

Figure 11.31

2 KC SQUARE WAVE RESPONSE
Figure 11.32

FREQUENCY RESPONSE
Figure 11.33

The output transistors, Q4 and Q5, were mounted on heat dissipating fins as shown in Figure 11.29 and the amplifier operated successfully delivering 1 watt rms 400 cycles continuous power to the load with no increase in total harmonic distortion from room ambient of 75°F to 175°F (approx. 80°C). At 175°F the dc voltage across Q5 had decreased less than 15% from its room ambient value. Operation at higher temperatures was not attempted because of Q3 being a germanium transistor which has a maximum operating junction temperature of 85°C.

When operated with the heat radiator assembly, this amplifier can safely deliver up to 10 watts rms of continuous power to the load at room temperature. When driving a loudspeaker with program material at a level where peak power may reach 10 watts, the rms power would generally be less than 1 watt. This amplifier, when operated with 2N2196's in the outputs, can be mounted on a smaller 2" x 2" fin because of its increased power capabilities. The 2N2196 has a case that simplifies mounting on a heat radiator and has electrical characteristics that equal or excel the 2N2107 or 7A31 for this application.

IM and total harmonic distortion is less than ½% at power levels under 3½ watts. The total harmonic distortion measured at 50 cycles, 400 cycles, and 10 kc is still

under 1% at 6 watts output, and the IM distortion under 2%. An rms input signal of 1¼ volts is required for 8 watts continuous output with a supply furnishing 350 ma at 48 volts. The amplifier operates with an efficiency of 47% to 60%, and has a signal-to-noise ratio of better than 98 db.

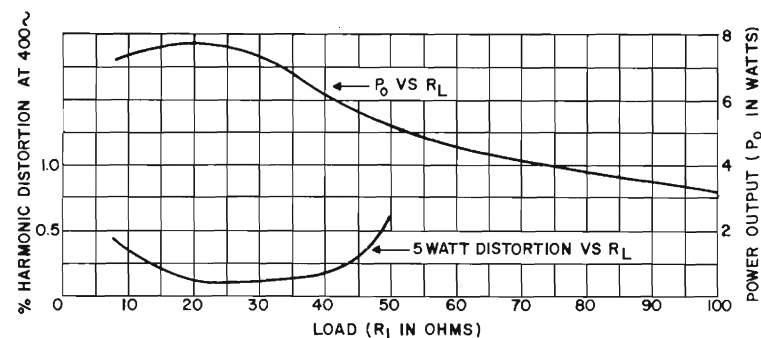
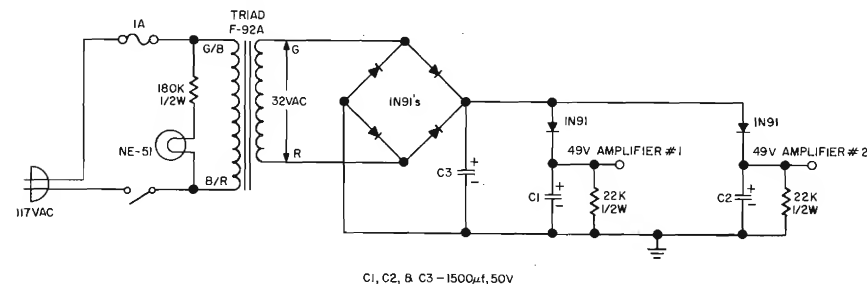
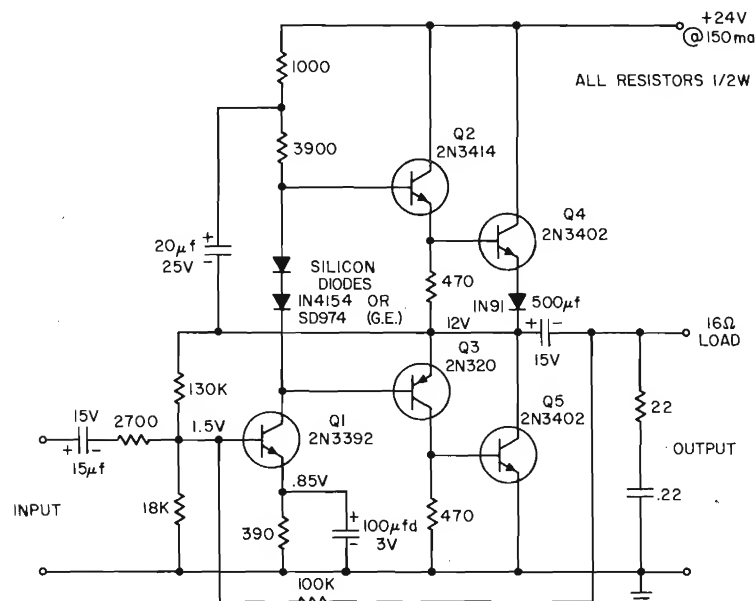
The performance tests were made with a 16 ohm resistive load. Performance near maximum power output will vary slightly with transistors of different beta values. Also, varying values of saturation resistance for the output transistors Q4 and Q5 affect the maximum power output.

AMPLIFIER PERFORMANCE VS. LOAD
Figure 11.34

Figure 11.34 shows the load range for maximum performance. It indicates that for a varying load impedance, such as a loudspeaker, the most desirable range is 16 to 40 ohms. A 16 ohm speaker system is in this range. A 20 to 600 ohm auto-transformer should be used for driving a 600 ohm line.

This amplifier can be used with either the power supply shown in Figure 11.35 or Figure 10.1 of Chapter 10.

POWER SUPPLY FOR STEREO SYSTEM
Figure 11.35

2½ Watt Transformerless Amplifier

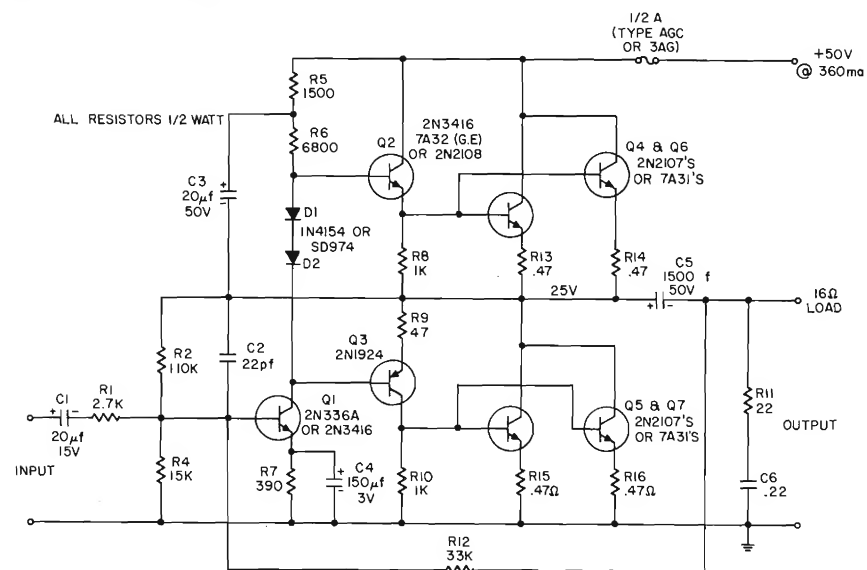
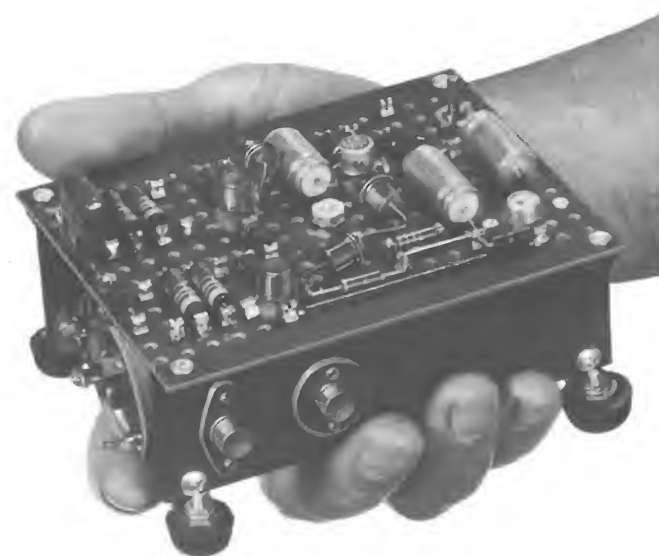
Figure 11.36 is a lower power version of the circuit shown in Figure 11.31. This 2½ watt amplifier uses economical semiconductors, and the output transistors, Q4

and Q5, can be fastened with their strap directly to the printed circuit board for adequate heat dissipation. This circuit requires about 330 millivolts input for 2½ watts power output. At this power level the total harmonic distortion at 1 kc is less than 1% and the IM distortion less than 2%.

2½ WATT AMPLIFIER
Figure 11.36

12 Watt Transformerless Amplifier

The amplifier shown in Figure 11.31 is limited in maximum power output by supply voltage and the increasing saturation resistance of the output transistors, Q4 and Q5, as the current increases. The supply voltage can not be increased much beyond 50 volts at maximum amplifier signal swing without making the V_{CE} rating for Q1 marginal. Under these conditions the saturation resistance becomes the limiting factor for obtaining increased power output.

The circuit of Figure 11.37 uses two transistors in parallel for each of the outputs. This enables the saturation resistance to be reduced in half and gives 12 watts output. The 0.47 ohm resistor used in the emitter of the paralleled transistors gives a more uniform input characteristic for sharing of the input currents. These emitter resistors, in addition, aid the bias stabilization. R9 in the emitter of Q3 improves the performance of this germanium transistor stage through local feedback. The rest of the circuit is the same as in Figure 11.31.

Performance of the 12 watt circuit is like that given previously for the circuit of Figure 11.31 except for the distortion vs. power output. Figure 11.39 indicates the increased power output and also the lower distortion which is a second advantage of parallel operation of the outputs. Lower distortion results from parallel operation since the signal current swing in each transistor is approximately halved and thus confined to the more linear portion of the transfer characteristic.

12 WATT AMPLIFIER
Figure 11.37

12 WATT AMPLIFIER
Figure 11.38

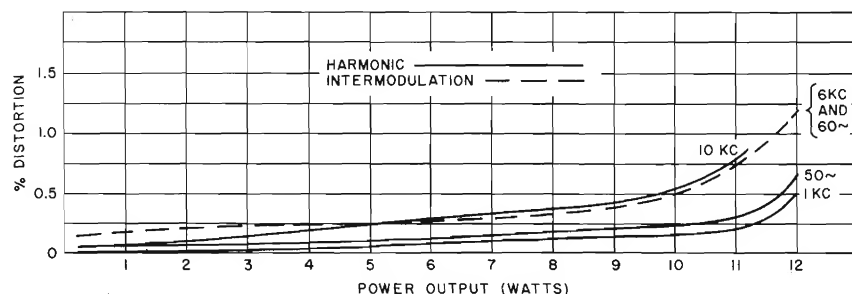
The 12 watt amplifier operates at maximum power output with an efficiency of 67%. This circuit can be packaged with minimum volume and weight without component crowding (see Figure 11.38). One of the paralleled output transistors uses the technique described in Figure 11.29 and the other makes for simplified mounting using the 2N2196 as previously discussed. All four of the output transistors could be 7A31's, 2N2107's, or all 2N2196's. Each mounting fin is 3/32" x 1½" x 4½" aluminum. If the amplifier is powered by the supply of Figure 11.35. It will provide 10 watts of continuous power output or 12 watts at Music Power Rating.

DISTORTION VS. POWER OUTPUT FOR 12 WATT AMPLIFIER

Figure 11.39

15 Watt Transformerless Amplifier

The amplifier in Figure 11.40 has an input stage added to increase the input impedance from about 3K ohms, as in the previous power amplifiers, to over 200K ohms. This stage also increases the amplifier sensitivity so that slightly less than 1 volt rms signal is required for full output.

The power frequency response is flat within ½ db from 20 cycles to 20 kc. Output impedance is less than 0.3 ohm for good speaker damping. At 15 watts the total harmonic distortion is less than ¼% across the band, 20 cycles to 20 kc. IM distortion (60 and 6000 cps mixed 4:1) is about 1% at 15 watts.

The output transistors should be mounted on a heat dissipator such as IERC #LP 5C3B (IERC, 135 W. Magnolia Blvd., Burbank, California).

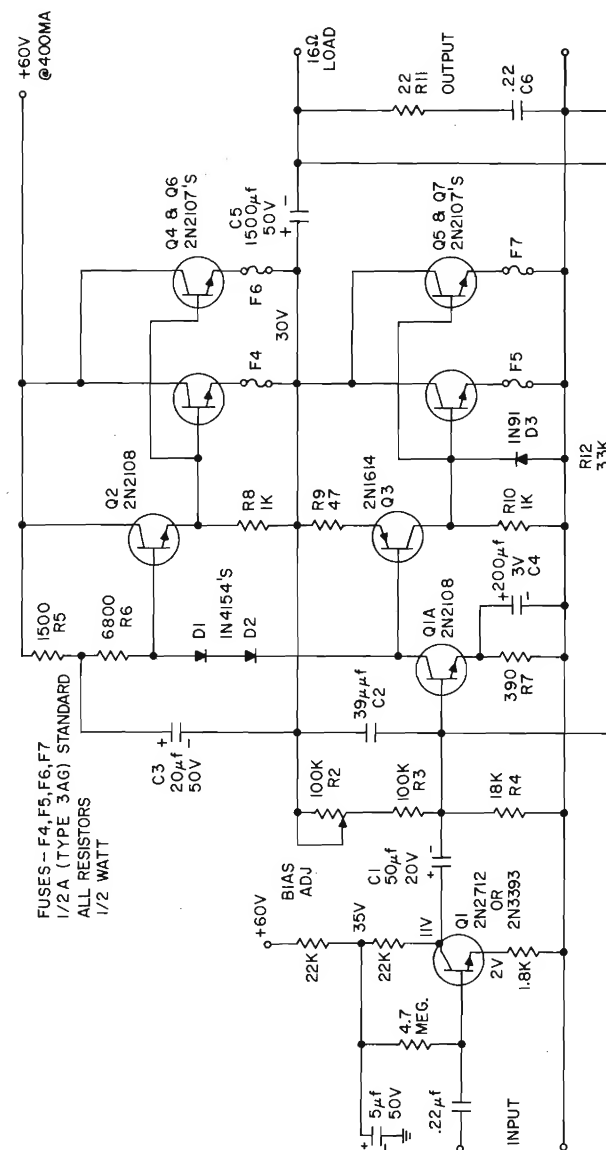
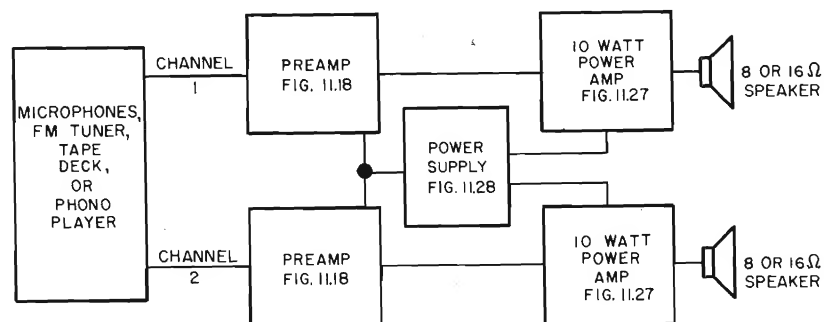
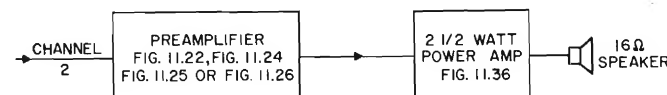
Diode D3 has a leakage current which increases with temperature in a manner similar to the I_{co} of Q3. D3 can thus shunt this temperature sensitive current to ground, whereas, if it were to flow into the base of Q5 and Q7, it would be amplified in the output stages. The standard ½ ampere fuse (Littlefuse type 3AG) has a dc resistance of about 1 ohm and is used in the emitter circuit of each output transistor for bias stabilization, equalization of the input characteristic for parallel operation, and protective fusing of the transistors. Bias adjust, R2, is set for one-half the supply voltage across Q5 and Q7. The power supply in Figure 10.3 is more than adequate to power two of these 15 watt amplifiers for 30 watts of continuous stereo power. This will give superb performance in a stereo system when used to drive 16 ohm speakers that have at least moderate sensitivity.

15 WATT AMPLIFIER

Figure 11.40

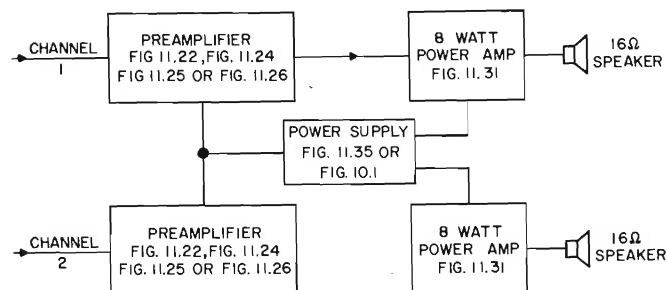
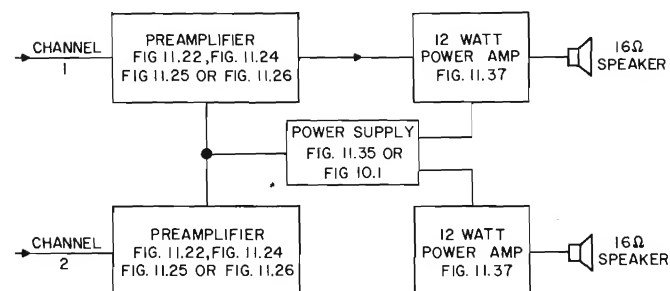
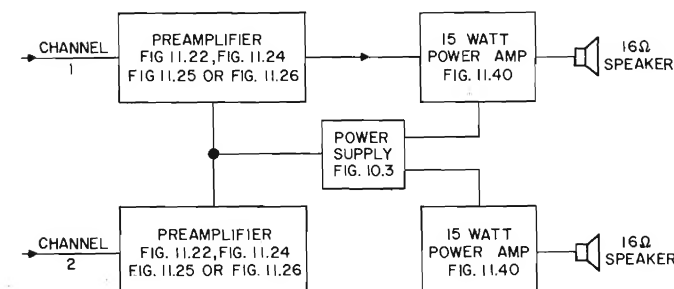
STEREOPHONIC SYSTEMS

Complete semiconductor, stereophonic playback systems may be assembled by using combinations of previous circuits as indicated in the block diagrams that follow.

20 WATT STEREO WITH 8 OR 16 OHM SPEAKERS

BLOCK DIAGRAM OF 20 WATT STEREOPHONIC SYSTEM
Figure 11.41

STEREOPHONIC SYSTEMS USING SILICON TRANSISTORS

5 WATT STEREOPHONIC SYSTEM
Figure 11.42

16 WATT STEREOPHONIC SYSTEM
Figure 11.43

CHANNEL 1
PREAMPLIFIER FIG 11.22, FIG. 11.24 FIG 11.25 OR FIG. 11.26
12 WATT POWER AMP FIG. 11.37
16Ω SPEAKER
POWER SUPPLY FIG. 11.35 OR FIG 10.1
CHANNEL 2
PREAMPLIFIER FIG. 11.22, FIG. 11.24 FIG. 11.25 OR FIG. 11.26
12 WATT POWER AMP FIG. 11.37
16Ω SPEAKER

24 WATT STEREOPHONIC SYSTEM
Figure 11.44

30 WATT STEREOPHONIC SYSTEM
Figure 11.45

STEREO HEADPHONE AMPLIFIER

The stereo headphone amplifier shown in Figure 11.46 will drive dynamic headphones of 75 to 400 ohms impedance to a power level of 45 to 60 milliwatts. Program source may be from a tuner or from records using a ceramic cartridge. This amplifier may also be used as a low level 600 ohm line driver.

Typical performance of the amplifier with a 200 ohm load, such as the AKG Model K50 dynamic headphones, has less than 1% IM distortion for 10 milliwatts output. At 1 milliwatt level or less (usual listening level with the K50) the distortion level is below the measuring capability of most test equipment. Frequency response is flat within ±⅓ db from 20 cycles to 20 kc. The input impedance is 1 megohm from 30 cycles to 2.5 kc and gradually decreases to 400K ohms at 15 kc. An input signal level of 110 millivolts will give 10 milliwatts output, and 250 millivolts input gives the maximum output of 60 milliwatts into a 200 ohm load.

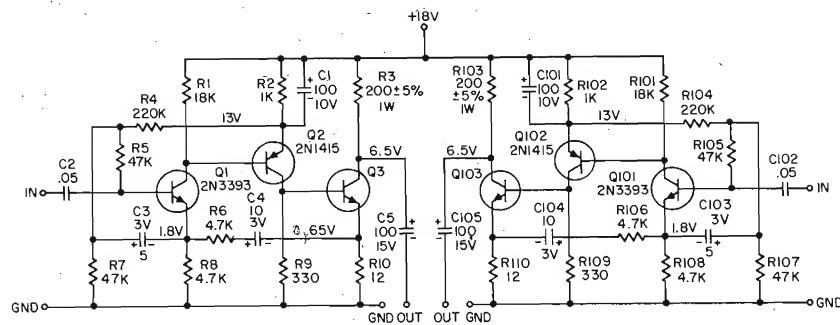
The high input impedance is attained by using a "bootstrapped" bias network for Q1 and also with the negative feedback via C4 and R6. This high impedance will not load the output of a tuner and can be readily adapted to many of the standard ceramic cartridges. Figure 11.47 shows a practical equalization and level control circuit for a cartridge capacitance of 1000 pf.

NOTE: SELECT R4 AND R104 TO GIVE 13 VOLTS AT EMITTER OF Q2 AND Q102.
Q3 AND Q103-2N2868 OR 11C1536(G.E.)
ALL RESISTORS 1/2 WATT, UNLESS NOTED.
ALL CAPACITORS IN μfd

Figure 11.46 STEREO HEADPHONE AMPLIFIER

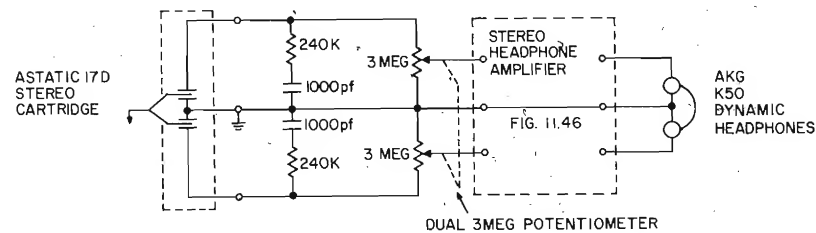



Figure 11.47 PHONO-HEADPHONE STEREO SYSTEM

A printed circuit board is shown in actual size in Figure 11.49. The component assembly of the Figure 11.46 circuit is shown in Figure 11.48.

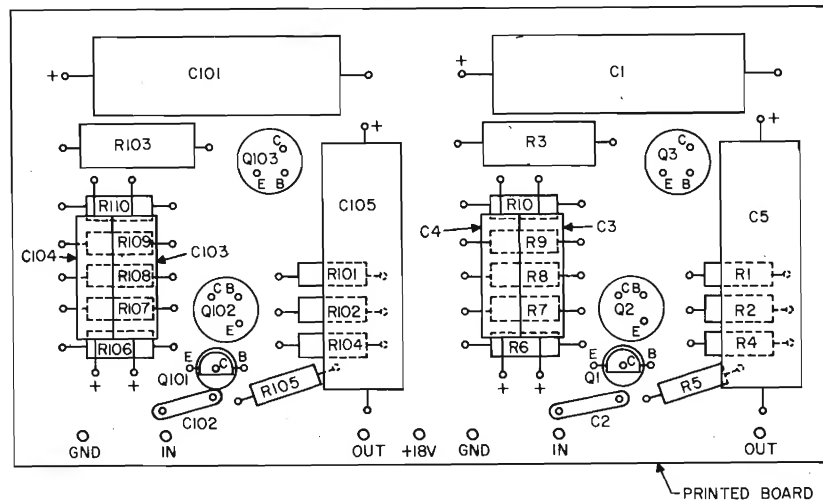
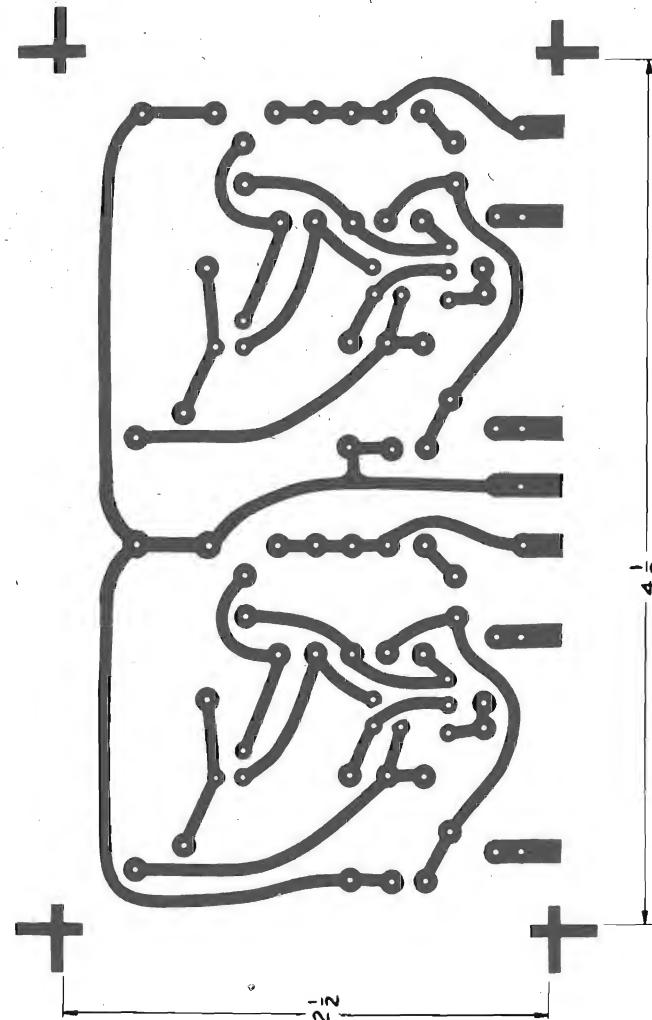



Figure 11.48 STEREO AMPLIFIER COMPONENT ASSEMBLY

PRINTED CIRCUIT BOARD
Figure 11.49

TAPE RECORDING AMPLIFIER WITH BIAS AND ERASE OSCILLATOR

The design of a magnetic recording amplifier will be discussed with equalization to produce a flat final system response with a Nortronics low impedance recording head when the playback preamplifier is adjusted for NAB equalization at 7½"/second tape speed. This design has sufficient input impedance to permit the use of a medium high impedance magnetic microphone and the circuit is capable of providing audio current at least 15 db above reference recording level at 1 kc.

The recording amplifier must perform several functions to properly impress a magnetic recording on tape. The microphone, or high level, signal must be amplified, pre-equalized, and presented as a recording current signal to the head. At the same time an oscillator, operating in this case between 70 kc and 80 kc, provides a bias current which is electrically added to the audio current supplied to the head. Figure 11.50 illustrates a block diagram for one channel only of the amplifier that will be described.

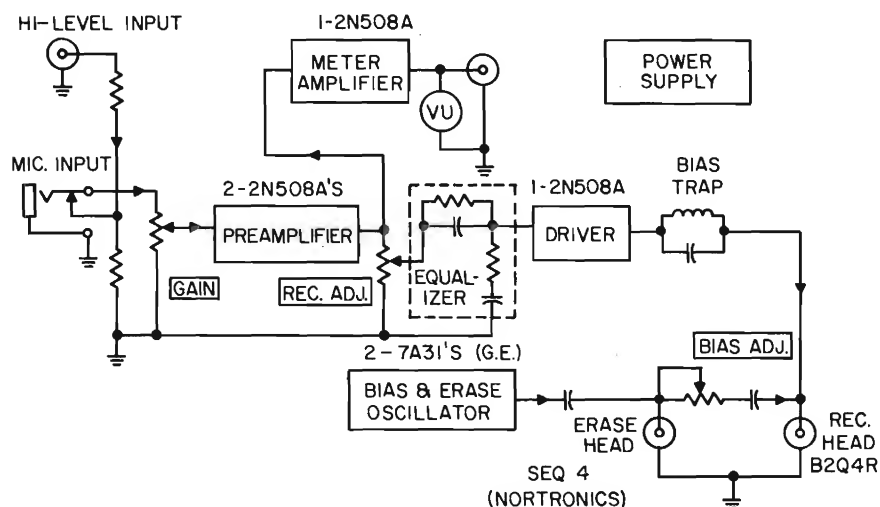



DIAGRAM OF RECORDING SYSTEM
(ONE CHANNEL)
Figure 11.50

RECORDING AMPLIFIER*

Record equalization for 7.5 ips is arrived at by extrapolating back to the NAB playback curve, the basic Nortronics constant current head response curve, and assuming that flat system response from 50 to 20 kc is desired. The NAB playback curve is shown in Figure 11.51. It represents what the output voltage of the amplifier will look like when the input is energized with a constant voltage signal in series with the playback head impedance over the audible range.

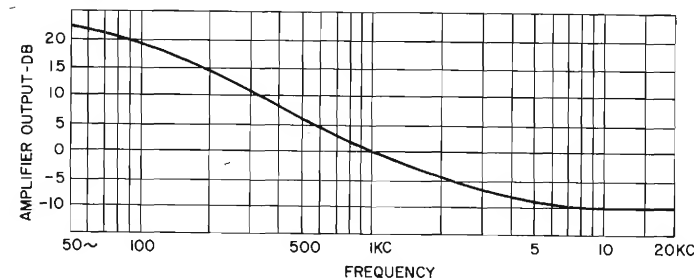
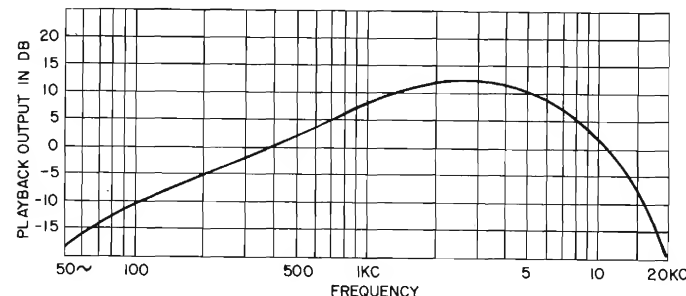
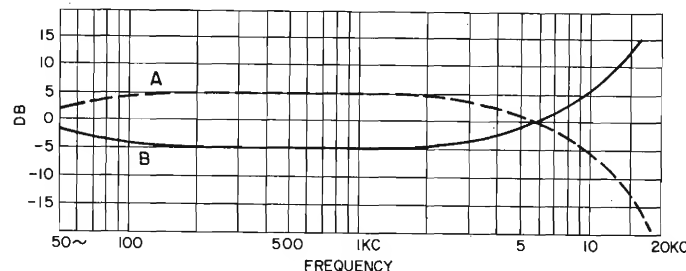
*Courtesy of Nortronics Co., 8101 West 10th Avenue, N., Minneapolis 27, Minn. Customer Engineering Bulletin No. 8.

PLAYBACK AMPLIFIER RESPONSE WITH CONSTANT VOLTAGE INPUT SIGNAL IN SERIES WITH HEAD IMPEDANCE
Figure 11.51

TYPICAL PLAYBACK HEAD RESPONSE FROM A TAPE RECORDED WITH CONSTANT CURRENT AT PEAK BIAS AT 7.5 IPS
Figure 11.52

Figure 11.52 is a plot of the constant current characteristic of a typical Nortronics head. This curve would result when taking the unequalized, open circuit voltage from the terminals of a playback head, where the recorded signal was with a constant recording current and bias current adjusted to peak at 1 kc response. When the curve in Figure 11.52 is subtracted from the curve in Figure 11.51 the resultant curve is shown by A in Figure 11.53. It is the inverse of this curve that is required during the recording process to give an overall flat system response. The inverted curve represents the desired audio current for the recording head.

RECORD EQUALIZATION CHARACTERISTICS AT 7½"/SEC.
Figure 11.53

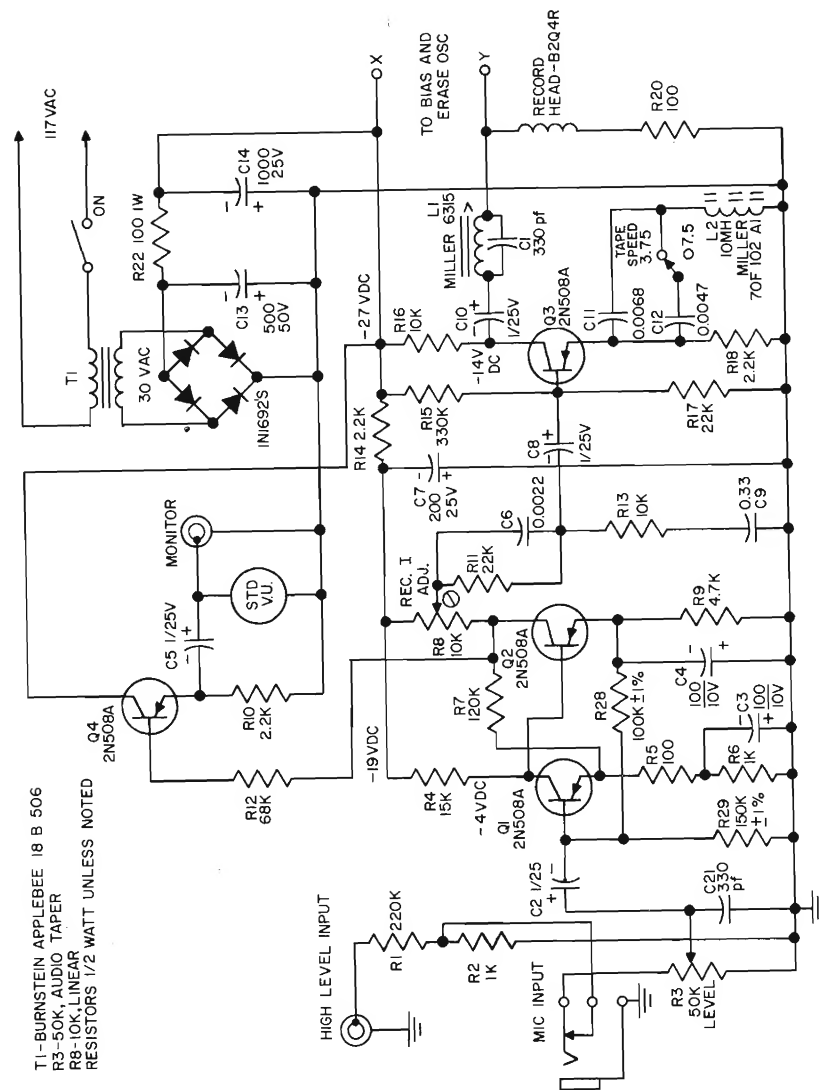



Figure 11.54 RECORDING AMPLIFIER

The first two stages of the recording amplifier in Figure 11.54 have a small amount of negative feedback through R7 to stabilize gain, increase input impedance, and generally provide amplification with low distortion.

The equalizing components in the amplifier include R11, C6, R13, C9, C11, C12, and L2. With frequencies between 200 cycles and 1500 cycles, R11 and R13 act as a straight voltage divider between the output of the *Record Current Adjust* and the base input of the last stage. At frequencies below 200 cycles the capacitive reactance of C9 becomes increasingly higher as the frequency goes down. This produces the slightly rising characteristic which is called for in Figure 11.53 at the low end.

At frequencies above 1500 cycles capacitor C6 begins to shunt resistor R11 producing an increasing amplitude of signal at the base of the driver transistor as the frequency goes up. The series resonant action of C11 and L2 provides a further assist to the high end boost, up to a peak of approximately 20 kc. This LC peaking circuit offers a further advantage of suppressing noise above 20 kc. The resulting curve is shown in Figure 11.55. Note that this curve is nearly the same as is called for in Figure 11.53. 0 db is 0 VU at 1 kc with a head current of 0.05 ma (50 microamperes). Note that the amplifier overload point is above tape saturation at 1 kc. With a quality playback system such as Figure 11.18 or Figure 11.22 a flat system response between 50 cycles and 15 kc is easily attained at 7.5 ips. It must be remembered that full frequency response at 7.5 ips must be checked at least 15 db below reference recording level, and at least —20 db at 3.75 ips.

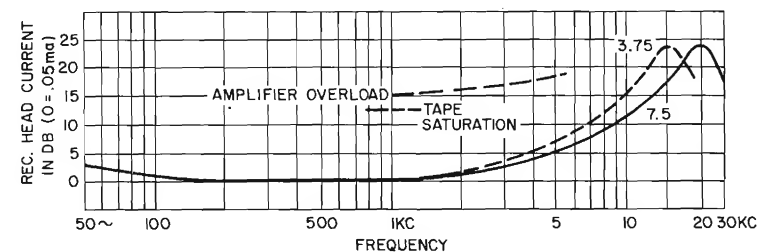



Figure 11.55 RECORD AMPLIFIER WITH B2Q4R

Record equalization for 3.75 ips is shown also in Figure 11.55 and is obtained by simply switching the additional capacitor (C12) into the circuit.

A bias trap consisting of L1 and C1 provides a high impedance to the bias frequency and thus reduces bias intermodulation at the collector of the driver stage. Adjust L1 for minimum bias signal at the collector of Q3. C21 is a bypass filter for the bias or higher rf frequencies.

The use of the gain control before the first stage will not be a source of noise if a good quality control is used. There are several good reasons for placing the control in this position, they include: the amplifier cannot be over-loaded under any conditions; and feedback can be applied between the first and second stage which will help to make the gain independent of transistor beta variations. The philosophy of design in this amplifier tends to promote operation at the highest signal-to-noise ratios under all conditions. The standard VU-meter which is driven by the emitter-follower is, in turn, directly connected to the output of the first two stages. Therefore, when a recording is being made sufficiently high in level to give proper reading on the VU-meter (peaks from 0 to +2) the operator is making full and proper use of signal level in the first two stages.

Construction of the amplifier should follow good standard practice and excessive heat should be avoided when soldering transistors and components. The power trans-

former should be located away from the input transistor and, if possible, it should be shielded with an external steel case. For stereo recording all of the Figure 11.54 circuit would be duplicated for the second channel except for the power supply. R22 can be reduced to maintain a 27 volt supply for a stereo system.

TAPE ERASE AND BIAS OSCILLATOR

As previously mentioned it is necessary to add a supersonic "bias current" to the audio current during the recording process; the amplitude (or magnitude) of this current is approximately ten times the amplitude of the average audio current. If it is too high it will result in unwanted degeneration of the higher audio frequencies, and if it is too low, recording stability, distortion, and dynamic range will all be adversely affected. At the so called "peak bias" operating mode, the 1 kc signal recorded on the tape will be at its maximum value; in practice this is a good point to operate a recording system.

In this application diffused silicon transistors are used since they offer the advantage of efficient operation with no external heat sink required. This silicon transistor is the 2N2106 or 7A30, and it has the standard T0-5 package.

The circuit of Figure 11.56 provides ample power to give a minimum of 60 db erasure of saturated tape (at 400 cycles) with a stereo erase head. This is accomplished with at least 10 ma of 70 to 80 kc signal in the Nortronics SEQ4 erase head. The total power output of this circuit is approximately 1½ watts with an efficiency of 60%. This erase signal increases the noise level only about 1 db on bulk erased tape. The balanced push-pull oscillator circuit of Figure 11.56 has negligible dc or even harmonic distortion in the output waveform which is a requirement for minimum increase in tape noise during playback. Total harmonic distortion is less than ½%.

SWITCH S1	
1	UPPER TRACK ONLY
2	STEREO
3	LOWER TRACK ONLY

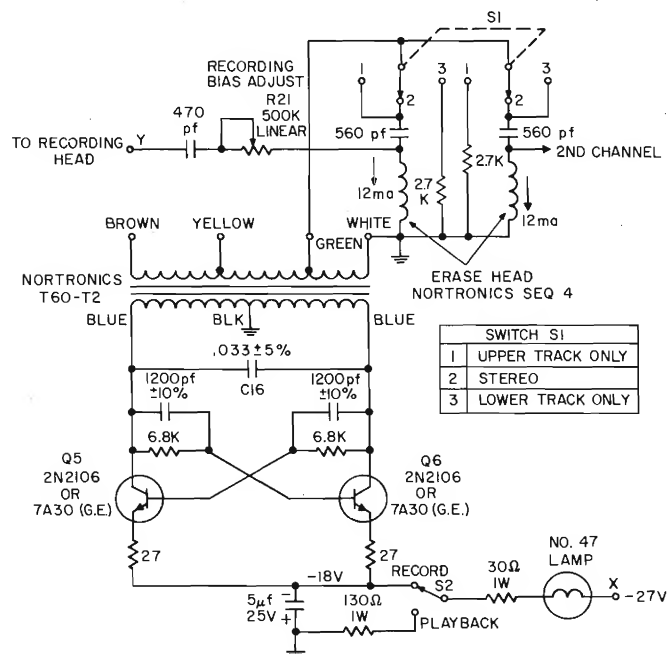



Figure 11.56 TAPE ERASE AND BIAS OSCILLATOR

C16 in the resonant tank circuit determines the frequency of the oscillator. Since the efficiency of the erase head decreases above approximately 76 kc, this was chosen as the operating frequency for the oscillator. Also, higher frequencies will be more difficult to handle in equipment with cable capacitance losses, circuit switching, etc.

The 27 ohm resistors provide negative feedback which help to compensate for component variations in the circuit. The transistor interchangeability vs circuit performance is very good.

This circuit is a cross-coupled multivibrator with a tuned load. The erase head winding is coupled to the transformer tap with 560 pf which series resonates with the erase head winding. Thus, the load appears largely resistive on the transformer secondary winding. This permits switching a 2.7K resistor in place of the series tuned erase head load without changing the loading or the frequency of the oscillator. This permits erasing and recording on only one channel of the tape. The series resonant circuit of the erase head winding and the 560 pf capacitor has a low Q of about 1½; variations in either the L or the C, therefore, will not alter appreciably the value of erase current in the head.

The 76 kc bias current for the recording head is adjusted with R21. Bias current can be measured by measuring the voltage across the 100 ohm resistor in series with the record head in Figure 11.54. A VTVM, such as a Ballantine 310A, is used for this measurement. The audio signal record current can also be measured at R20, but switch S2 in Figure 11.56 must be in the playback position to stop the oscillator bias current. The approximate reference level 1 kc record signal current for the Nortronics B2Q4R is 0.05 ma and the bias current is 0.70 ma. Accurate determination of bias and record currents can best be achieved by using a deck with an independent playback head and amplifier. Under these conditions the bias current is adjusted until the 1 kc response is maximum and the record current is adjusted until "0—VU" on the meter is one-fourth (—12 db) of saturation level.

REFERENCES

(1) McKnight, J.G., "Signal-to-Noise Problems and a New Equalization For Magnetic Recording of Music." Audio Engineering Society Preprint #58, presented October 1958.
(2) Jones, D.V., "Class B Power Amplifier Performance with Silicon Transistors," Audio Engineering Society Convention Paper, presented October 1960.
(3) Geiser, D.T., "Using Diodes as Power Supply Filter Elements," *Electronic Design*, June 10, 1959.
(4) Jones, D.V., "All Transistor Stereo Tape System," *Electronics World*, July 1959.

NOTES

NOTES

RADIO RECEIVER CIRCUITS

CHAPTER 12

Transistorized radio receiver circuits are of two main categories; *portable and line operated.* The transistors used may be germanium or silicon or a combination of the two. Practical working circuits representing some of the more popular radios are offered at the end of this Chapter.

SILICON TRANSISTORS

Silicon transistors in low cost *epoxy* housings have recently been introduced by General Electric for use in FM, AM, and TV receivers. Figure 12.1 shows the size and shape of the new transistor as compared to the conventional TO-18 and TO-5 packages. Figure 12.2 presents an internal view of the construction.

SIZE COMPARISON OF LOW COST EPOXY HOUSING TO TO-18 AND TO-5

Figure 12.1

The transistors are manufactured by the planar passivated process, which is the very latest technique employed on high reliability military transistors. Low costs are achieved by an entirely new concept of highly mechanized manufacture, the use of the epoxy package, and high speed automatic testing.

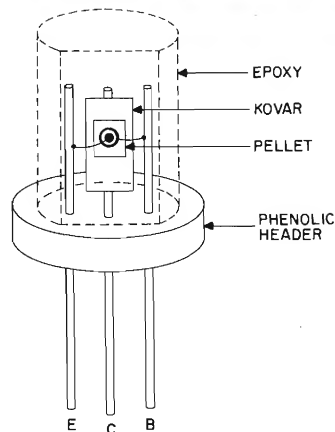
When designing radio circuits with silicon transistors there is very little difference in technique as compared to germanium transistors, with the major exception of the dc biasing circuits. Silicon transistors will exhibit a larger change in quiescent collector current when the supply voltage is varied than will germanium transistors if conventional biasing circuits are used. In portable radios, where operation is required at half the original battery voltage, a special biasing technique is required. This has been discussed on page 101 of Chapter 4. Other more obvious methods would be the use of a Zener diode to regulate the supply voltage at a value below the original battery voltage, or the use of a single, separate battery to supply only the base circuits. Since current drain would be very low, the life of the battery would be essentially its shelf life.

ADVANTAGES

Some of the advantages to be gained by the use of silicon transistors are

1. *Low I_{CO}* permits simpler circuit design and improved high temperature operation.
2. *Stable characteristics* are guaranteed by the passivated surface.
3. *Consistent characteristics* are inherently produced by the planar process

INTERNAL VIEW OF 2N2711 AND 2N2921 SERIES

Figure 12.2

which simplifies bias circuits, makes possible fixed neutralization of collector feedback capacity, and assures constant power gain.

4. *Small solid package* is practically immune to shock and vibration.
5. *High cut-off frequency* in excess of 100 Mc assures a constant, high power gain across the frequency band.
6. *High betas* of 500 and higher are perfectly practical and useable with silicon transistors. This permits high gain AVC systems and high gain audio systems.

LINE OPERATED RECEIVERS

Subsequent sections are devoted to a stage by stage discussion of portable receivers and with few exceptions they are applicable to line operated receivers. The main differences to consider are the derivation of a suitable supply voltage from the line voltage, the higher audio output generally required, and the feasibility of using Class A output stages since power consumption is not very important.

The most economical design, the *Four Transistor Line Set*, is shown in Figure 12.21. Incorporation of a Class A output stage, with its constant current drain, permits the use of a simple half wave rectifier and dropping resistance. The resistance may consist of a light bulb, a high resistance line cord, or an actual resistor. Even with an inefficient power supply of this nature, power consumption of the transistor set is only one third that of a tube set. Sensitivity, selectivity, and audio output of the transistor receiver are all equal or superior to an equivalent 5 tube AC-DC radio.

A more deluxe radio for those who prefer push-pull output is the *Six Transistor Line Set* shown in Figure 12.22. The varying load current drawn by the output necessitates a low impedance power supply in order to maintain the B+ voltage nearly constant as the load power is increased. A "filament" step down transformer and half-wave rectifier is sufficient to allow close to one watt audio output power.

RADIO FREQUENCY CIRCUITS

A tuned RF stage at the input of a radio receiver will greatly enhance performance in several important respects. Improved signal to noise ratio, sensitivity, selectivity, and AVC are all benefits to be expected from the use of a tuned RF stage.

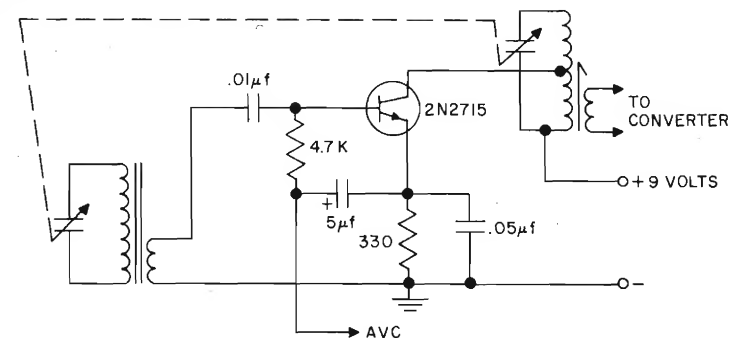
In establishing the maximum useable sensitivity of a receiver (or the minimum signal that can be satisfactorily received) the predominating factor is the noise con-

TUNED RF STAGE

Figure 12.3

tribution of the first stage. If the first stage has a high equivalent noise input, then a large signal will be required to overcome the noise and produce an intelligible output. Once the signal and noise have been inter-mixed, it is practically impossible to separate them. The effect of noise added by succeeding stages is of secondary importance because it is reduced by the gain of the first stage according to the relation

$$NF = NF_1 + \frac{NF_2}{G_1}$$

where

NF is the overall receiver noise figure

NF_1 is the RF stage noise figure

NF_2 is the converter stage noise figure, and

G_1 is the RF stage gain.

A transistor used as a linear RF amplifier will inherently be several db quieter than the same transistor used as a converter because the mixing action of a converter produces additional noise components not present in the RF stage. For the ultimate in sensitivity therefore, an RF stage is required.

An alternative method to describe noise performance, which in practice is simpler to measure, is signal to noise ratio, S/N. The end result, however, is identical; a *figure of merit* which describes a receiver's ability to perform on weak signals. ENSI ratio or *equivalent noise sideband input* is still another method. For a complete description of these procedures see the Radiotron Designer's Handbook by Langford-Smith, or appropriate IEEE standards.

Improved selectivity results directly from the extra tuned circuit in the collector of the RF stage. By narrowing the bandwidth, unwanted signals close to the desired signal will be rejected. Image frequencies (desired RF signal frequency plus twice the intermediate frequency, IF) will also be greatly attenuated.

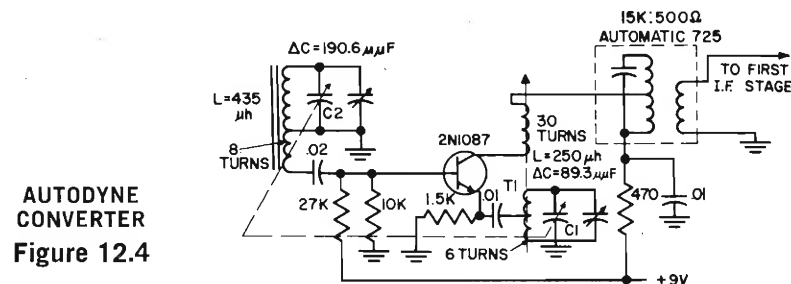
Automatic volume control, AVC, is improved by an RF stage for several reasons. In the ordinary converter input radio, AVC power is taken from the detector and applied to the first IF stage. There is only one stage of gain between the controlled stage and the detector, which is the second IF. In a receiver with an RF stage there will be at least two stages of gain between the controlled stage and the detector, the converter and IF. There will therefore be more *loop gain* within the AVC closure, and better AVC action. A small amount of AVC may also be placed on the IF for additional control.

A converter is *not* usually AVC'd, as the bias change would cause an appreciable

shift in oscillator frequency. When the converter is the input stage it must be operated at maximum gain for best performance on weak signals. Under strong signal conditions, it still will be high gain and will deliver a large signal to the IF, tending to cause overload. With an RF stage, control is applied to the very first amplifier, which is the most effective place. *Blocking* of the converter on strong signals is greatly reduced by AVC on the RF stage, as the signal to the converter can be less than the incoming signal.

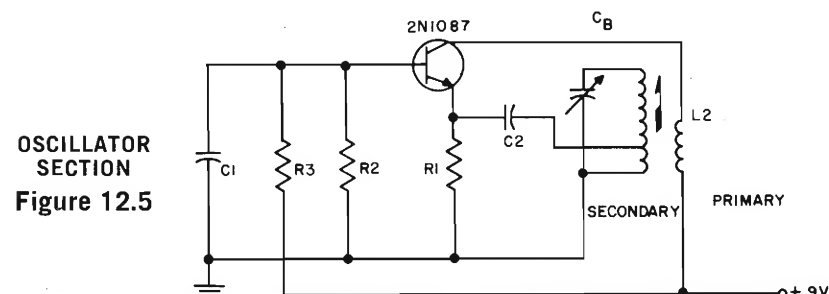
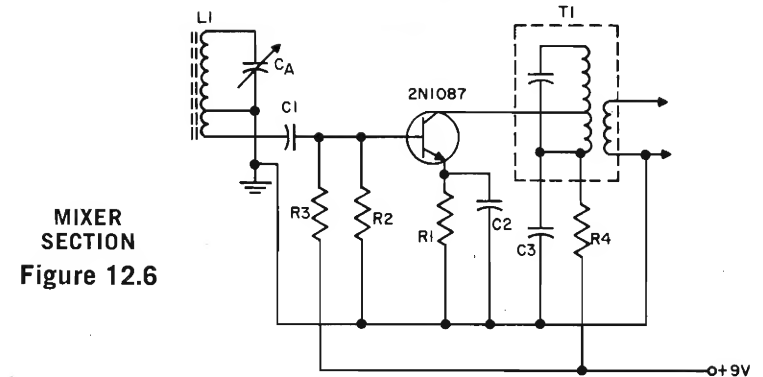
However, there are a few disadvantages in using an RF stage: a three-gang tuning condenser is required which occupies more space and is more expensive; and, due to the extra tuned circuit the receiver is more difficult to align and *track*.

AUTODYNE CONVERTER CIRCUITS

The converter stage of a transistor radio is a combination of a local oscillator, a mixer, and an IF amplifier. A typical circuit for this stage is shown in Figure 12.4.

AUTODYNE CONVERTER
Figure 12.4

FOR ADDITIONAL INFORMATION SEE PAGE 299

Redrawing the circuit to illustrate the oscillator and mixer sections separately, we obtain Figures 12.5 and 12.6.

The operation of the oscillator section in Figure 12.5 is as follows: random noise produces a slight variation in base current which is subsequently amplified to a larger variation of collector current. This ac signal in the primary of L_2 induces an ac current into the secondary of L_2 tuned by C_B to the desired oscillator frequency. C_2 then couples the resonant frequency signal back into the emitter circuit. If the feedback (tickler) winding of L_2 is properly phased the feedback will be positive (regenerative) and of proper magnitude to cause sustained oscillations. The secondary of L_2 is an auto-transformer to achieve proper impedance match between the high impedance tank circuit of L_2 and the relatively low impedance of the emitter circuit.

OSCILLATOR SECTION
Figure 12.5

MIXER SECTION
Figure 12.6

C_1 effectively bypasses the biasing resistors R_2 and R_3 to ground, thus the base is ac grounded. In other words, the oscillator section operates essentially in the *grounded base* configuration.

The operation of the mixer section in Figure 12.6 is as follows: the ferrite rod antenna L_1 exposed to the radiation field of the entire frequency spectrum is tuned by C_A to the desired frequency (broadcast station).

The transistor is biased in a relatively low current region, thus exhibiting quite non-linear characteristics. This enables the incoming signal to mix with the oscillator signal present, creating signals of the following four frequencies

1. *Local oscillator signal*
2. *Received incoming signal*
3. *Sum of the above two*
4. *Difference between the above two.*

The IF load impedance T_1 is tuned here to the difference between the oscillator and incoming signal frequencies. This frequency is called the intermediate frequency (IF) and is conventionally 455 KC. This frequency will be maintained fixed since C_A and C_B are mechanically geared (ganged) together. R_4 and C_3 make up a filter to prevent undesirable currents flowing through the collector circuit. C_2 essentially bypasses the biasing and stabilizing resistor R_1 to ground. Since the emitter is grounded and the incoming signal injected into the base, the mixer section operates in the *grounded emitter* configuration.

IF AMPLIFIERS AND AVC SYSTEMS

A typical circuit for a transistor IF amplifier is shown by Figure 12.7.

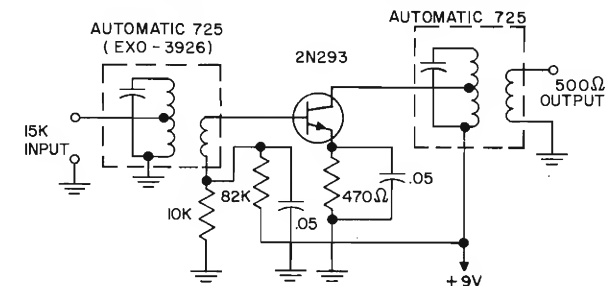



Figure 12.7 IF AMPLIFIER

The collector current is determined by a voltage divider on the base and a large resistance in the emitter. The input and output are coupled by means of tuned IF transformers. The .05 capacitors are used to prevent degeneration by the resistance in the emitter. The collector of the transistor is connected to a tap on the output transformer to provide proper matching for the transistor and also to make the performance of the stage relatively independent of variations between transistors of the same type. With a rate-grown NPN transistor such as the 2N293, it is unnecessary to use neutralization to obtain a stable IF amplifier. With PNP alloy transistors, it is necessary to use neutralization to obtain a stable amplifier and the neutralization capacitor depends on the collector capacitance of the transistor. The gain of a transistor IF amplifier will decrease if the emitter current is decreased. This property of the transistor can be used to control the gain of the IF amplifier so that weak stations and strong stations will produce the same audio output from a radio. Typical circuits for changing the gain of an IF amplifier in accordance with the strength of the received signal are explained in the AVC section of this chapter.

AVC is a system which automatically varies the total amplification of the signal in a radio receiver with changing strength of the received signal carrier wave. From the definition given, it would be correctly inferred that a more exact term to describe the system would be automatic gain control (AGC).

Since broadcast stations are at different distances from a receiver and there is a great deal of variation in transmitted power from station-to-station, the field strength around a receiver can vary by several orders of magnitude. Thus, without some sort of automatic control circuit, the output power of the receiver would vary considerably when tuning through the frequency band. It is the purpose of the AVC, or AGC, circuit to maintain the output power of the receiver constant for large variations of signal strengths.

Another important purpose of this circuit is its so-called "anti-fading" properties. The received signal strength from a distant station depends on the phase and amplitude relationship of the ground wave and the sky wave. With atmospheric changes this relationship can change, yielding a net variation in signal strength. Since these changes may be of periodic and/or temporary nature, the AVC system will maintain the average output power constant without constantly adjusting the volume control.

The AVC system consists of taking, at the detector, a voltage proportional to the incoming carrier amplitude and applying it as a negative bias to the controlled amplifier thereby reducing its gain.

In tube circuits the control voltage is a negative going dc grid voltage creating a loss in transconductance (Gm).

In transistor circuits various types of AVC schemes can be used.

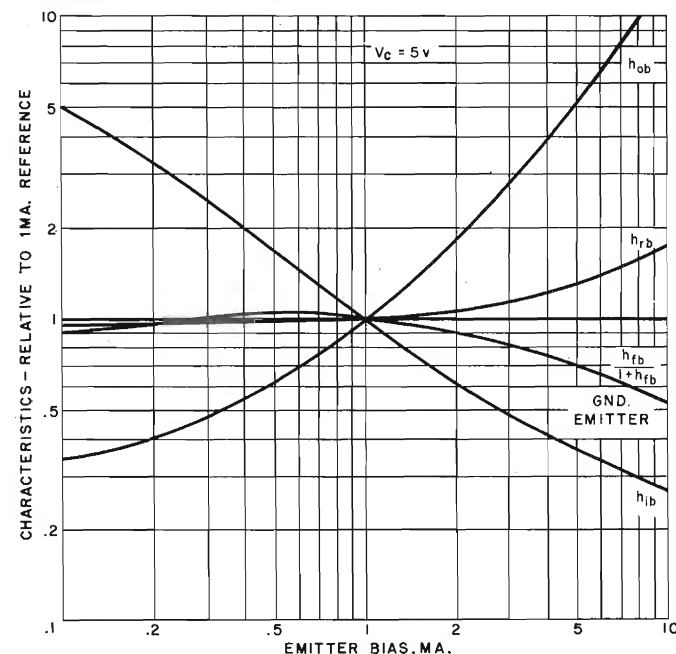
EMITTER CURRENT CONTROL

As the emitter current of a transistor is reduced (from 1.0 ma to .1 ma for instance) various parameters change considerably (see Figure 12.8).

The effect of these changes will be twofold

1. *A change in maximum available gain, and*
2. *A change in impedance matching since it can be seen that both h_{ob} and h_{ib} vary radically.*

Therefore, a considerable change in power gain can be obtained as shown by Figure 12.9.

On the other hand, as a result of I_{CO} (collector leakage current) some current always flows, thus a transistor can be controlled only up to a point and cannot be "cut-off" completely. This system yields generally fair control and is, therefore, used more than others. For performance data see Figure 12.10.

CHARACTERISTICS VS. EMITTER CURRENT

h PARAMETERS VS. EMITTER BIAS CURRENT

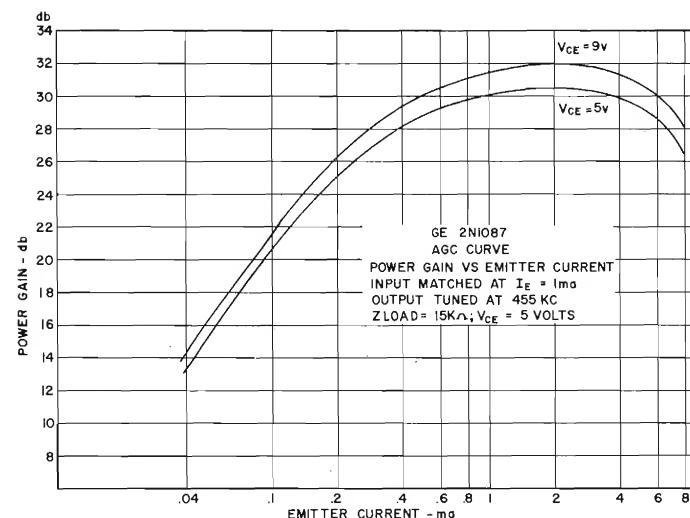
Figure 12.8

POWER GAIN VS. EMITTER CURRENT

Figure 12.9

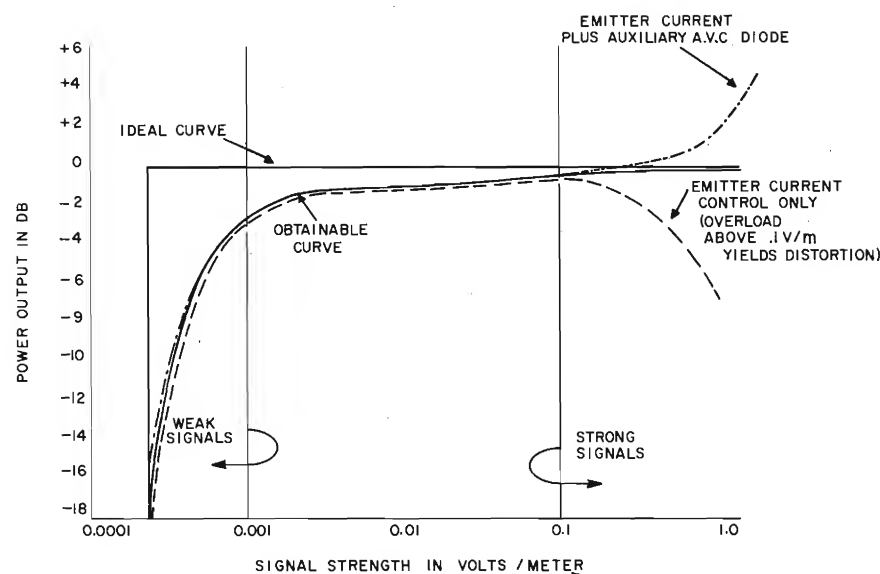



Figure 12.10 IDEAL VS. TYPICAL AVC PERFORMANCE

AUXILIARY AVC SYSTEMS

Since most AVC systems are somewhat limited in performance, to obtain improved control, auxiliary diode AVC is sometimes used. The technique used is to shunt some of the signal to ground when operating at high signal levels, as shown by Figure 12.11.

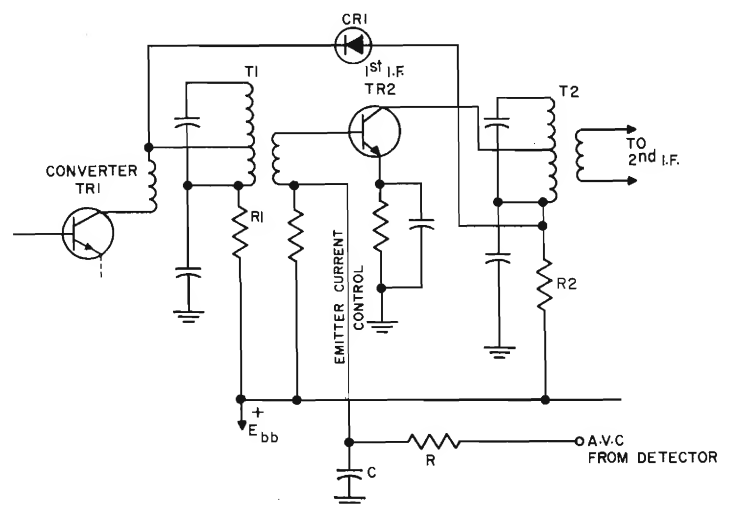



Figure 12.11 AUXILIARY DIODE AVC SYSTEM

In the circuit of Figure 12.11, diode CR_1 is back-biased by the voltage drops across R_1 and R_2 and represents a high impedance across T_1 at low signal levels. As the signal strength increases, the conventional emitter current control AVC system creates a bias change reducing the emitter current of the controlled stage. This current reduction coupled with the ensuing impedance mismatch creates a power gain loss in the stage. As the current is further reduced, the voltage drop across R_2 becomes smaller thus changing the bias across CR_1. At a predetermined level CR_1 becomes forward biased, constituting a low impedance shunt across T_1 and creating a great deal of additional AVC action. This system will generally handle high signal strengths as can be seen from Figure 12.10. Hence, almost all radio circuit diagrams in the circuit section of this chapter use this system in addition to the conventional emitter current control.

DETECTOR STAGE

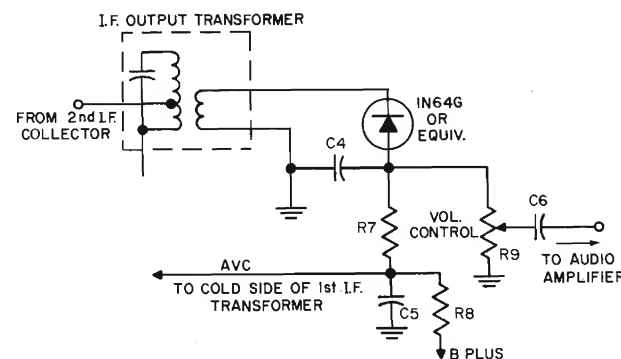
In this stage (see Figure 12.12), use is made of a slightly forward biased diode in order to operate out of the square law detection portion of the I-V characteristics. This stage is also used as source of AGC potential derived from the filtered portion of the signal as seen across the volume control R_9. This potential, proportional to the signal level, is then applied through the AGC filter network C_4, R_7 and C_5 to the base of the 1st IF transistor in a manner to decrease collector current at increasing signal levels. R_8 is a bias resistor used to fix the quiescent operating points of both the 1st IF and the detector stage, while C_6 couples the detected signal to the audio amplifier. (See Chapter 11 on Audio Amplifiers.)

DETECTOR STAGE

Figure 12.12

REFLEX CIRCUITS

"A *reflex* amplifier is one which is used to amplify at two frequencies – usually intermediate and audio frequencies."*

The system consists of using an IF amplifier stage and after detection to return the audio portion to the same stage where it is then amplified again. Since in Figure 12.13, two signals of widely different frequencies are amplified, this does not constitute a *"regenerative effect"* and the input and output of these stages can have split audio/IF loads. In Figure 12.14, the IF signal (455 KC) is fed through T_2 to the detector circuit CR_1, C_3 and R_5. The detected audio appears across the volume control R_5 and is returned through C_4 to the cold side of the secondary of T_1.

* F. Langford-Smith, Radiotron Designers Handbook, Australia, 1953, p. 1140

AUXILIARY A.V.C. IN64G

AUTODYNE CONVERTER 2N1087 — FIRST I.F. AMPLIFIER 2N292 — 2nd I.F. + AUDIO DRIVER 2N169 — DIODE DETECTOR + A.V.C. IN64G — AUDIO POWER OUTPUT 2N1414

AUDIO — AUDIO — A.V.C.

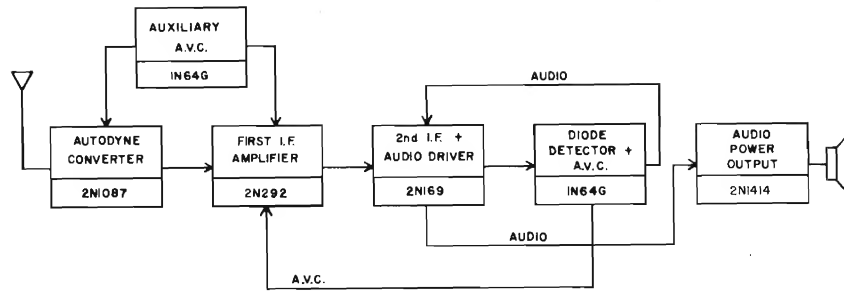



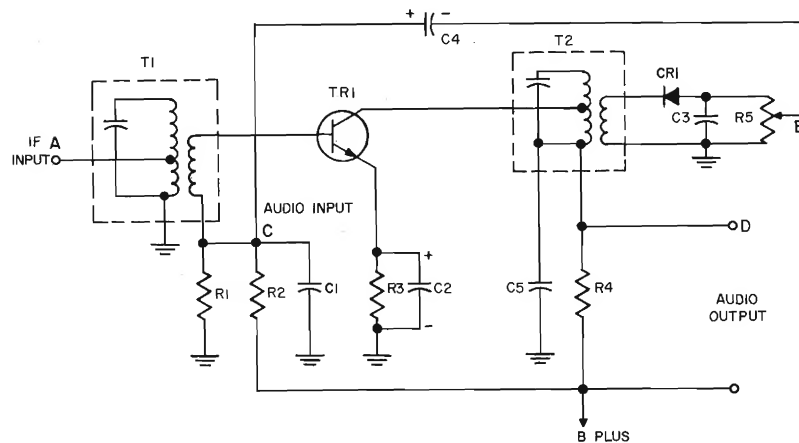
Figure 12.13 REFLEX RECEIVER SYSTEM

REFLEX IF-DETECTOR CIRCUIT

Figure 12.14

Since the secondary consists of only a few turns of wire, it is essentially a short circuit at audio frequencies. C_1 bypasses the IF signal otherwise appearing across the parallel combination of R_1 and R_2. The emitter resistor R_3 is bypassed for both audio and IF by the electrolytic condenser C_2. After amplification, the audio signal appears across R_4 from where it is then fed to the audio output stage. C_5 bypasses R_4 for IF frequencies and the primary of T_2 is essentially a short circuit for the audio signal.

The advantage of *reflex* circuits is that one stage produces gain otherwise requiring two stages with the resulting savings in cost, space, and battery drain. The disadvantages of such circuits are that the design is considerably more difficult, although once a satisfactory receiver has been designed, no outstanding production difficulties should be encountered. Other disadvantages are a somewhat higher amount of "playthrough" (i.e. signal output with volume control at zero setting), and a minimum volume effect. The latter is the occurrence of minimum volume at a volume control setting slightly higher than zero. At this point, the signal is distorted due to the balancing out of the fundamentals from the normal signal and the out-of-phase playthrough component. Schematics of complete receivers will be found at the end of this chapter and in Chapter 15.

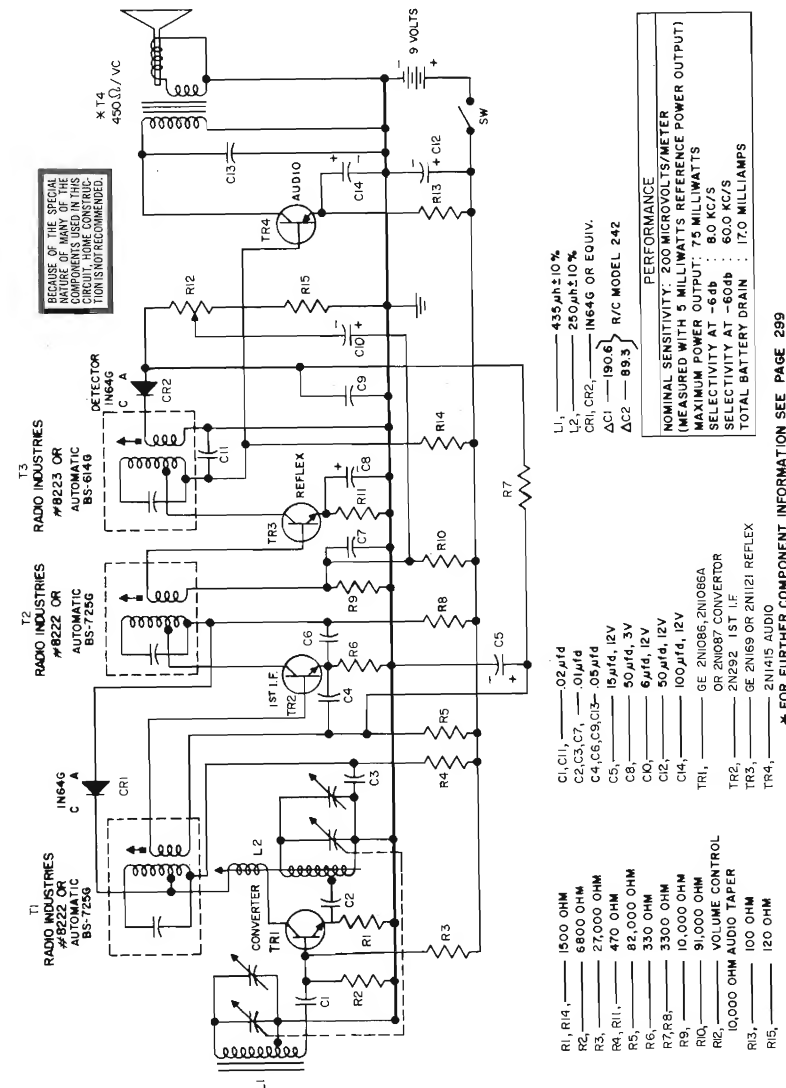
COMPLETE RADIO RECEIVER CIRCUIT DIAGRAMS

FOUR TRANSISTOR — 9 VOLT REFLEX RECEIVER

Figure 12.15

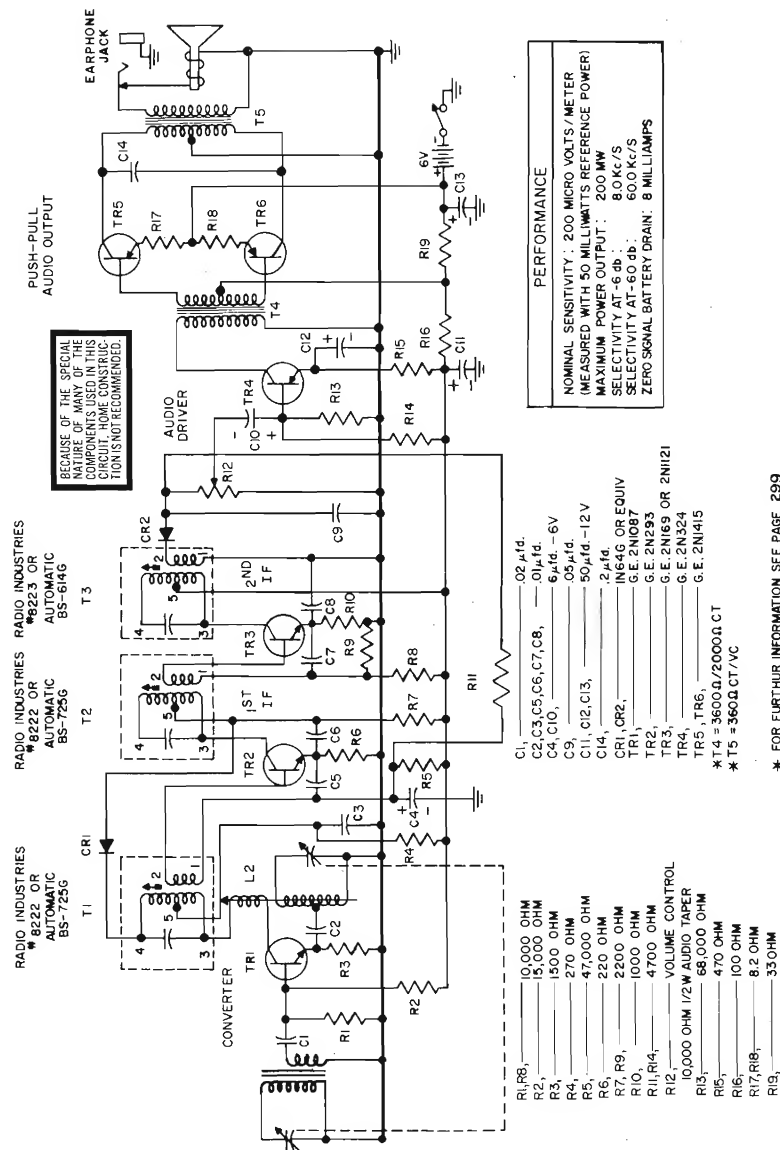
* FOR FURTHUR INFORMATION SEE PAGE 299

SIX TRANSISTOR — 6 VOLT BROADCAST RECEIVER

Figure 12.16

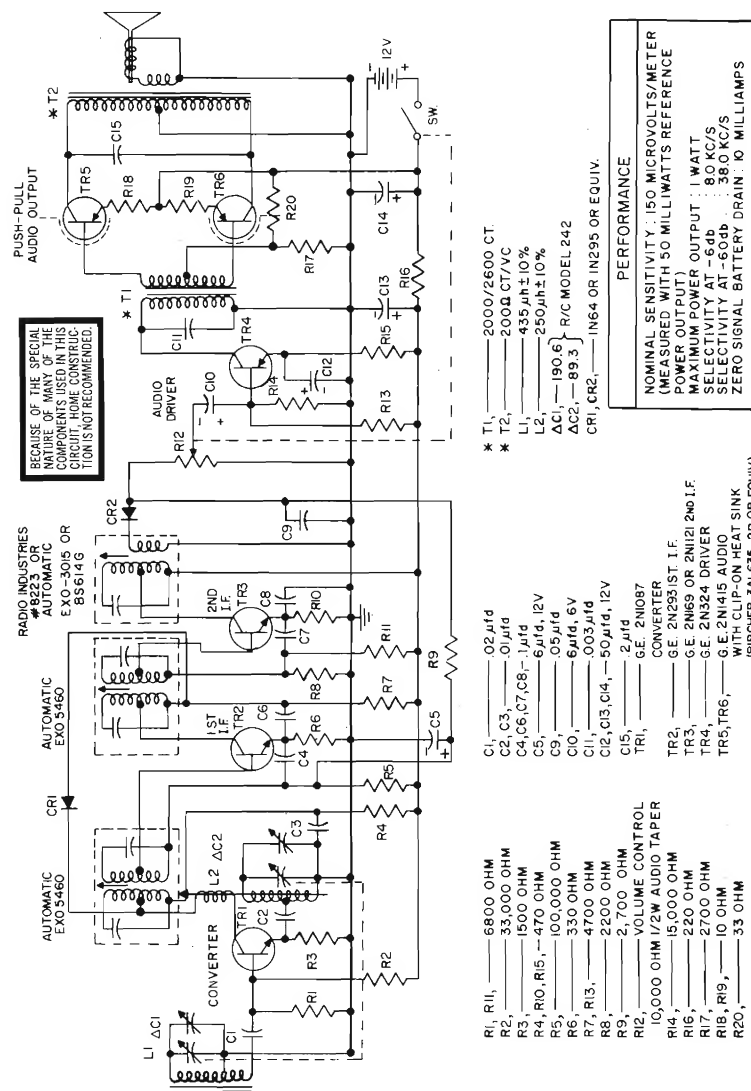
* FOR FURTHER COMPONENT INFORMATION SEE PAGE 299

SIX TRANSISTOR — 12 VOLT 1 WATT RECEIVER

Figure 12.17

*USE 1.0 pf WITH 2N2926 AND 2N3391 SERIES TRANSISTOR, 0.5 pf WITH 2N2715 SERIES

GENERAL ELECTRIC CO.

Q1, Q3 2N2926 (RED) OR 2N2715 OR 2N3394
Q2, Q4 2N2926 (ORANGE) OR 2N2716 OR 2N3393
Q5, Q6 2N321
D1 1N4009 (SILICON)
D2 1N60 (GERMANIUM)

RADIO INDUSTRIES, INC.

T1 13964-R1
T2, T3 13964
L1 16413
L2 16411
ΔC MODEL 42-2A

PERFORMANCE	
NOMINAL SENSITIVITY	75 μv/m
RATED OUTPUT POWER	280 MW
BATTERY DRAIN	10.5 MA

OTHER COMPONENTS
T4 7K/3K C. T.

SIX TRANSISTOR — 6 VOLT RECEIVER
Figure 12.18

GENERAL ELECTRIC CO.

Q1,Q3 2N2926 (RED) OR 2N2715 OR 2N3394
Q2,Q4 2N2926 (ORANGE) OR 2N2716 OR 2N3393
Q5,Q6 2N2714 (WITH HEAT SINK)
D1 1N60 (GERMANIUM)
D2,D3 1N4009 (SILICON)

RADIO INDUSTRIES, INC.

T1 - 13964-R1
T2,T3-13964
L1 16413
L2 16411
ΔC MODEL 42-2A

PERFORMANCE	
NOMINAL SENSITIVITY	20 μv/m
RATED OUTPUT POWER	500 MW
BATTERY DRAIN	10 MA

OTHER COMPONENTS
T4-5K/2K CT
T5-250 Ω CT/VC

*USE 1.0 pf WITH 2N2926 AND 2N3391 SERIES TRANSISTORS, 0.5 pf WITH 2N2715 SERIES.

SIX TRANSISTOR — 9 VOLT RECEIVER
Figure 12.19

SIX TRANSISTOR — 9 VOLT RECEIVER WITH TUNED RF STAGE

Figure 12.20

FOUR TRANSISTOR LINE SET

Figure 12.21

SIX TRANSISTOR LINE SET
Figure 12.22

Heatsinks for the 2N2714 transistor may be constructed by epoxy glueing, or clamping the "flat side" of the transistor to a 2" x 2" piece of copper or aluminum. Both transistors may be mounted on the same heatsink, as the case is electrically insulated from the transistor.

The 2N2196 and 2N2107 may be bolted or clamped to a 2" x 2" copper or aluminum heatsink. Observe proper isolation of the heatsink, as the collector of the transistor is connected to the case. See Chapter 11 for further details.

ADDITIONAL COMPONENT INFORMATION

ANTENNA, IF TRANSFORMERS, OSCILLATOR COIL, TUNING CONDENSER

Original equipment manufacture (OEM) should contact Radio Industries Inc., 666 Garland Place, Des Plaines, Illinois for further information.

NOTES

SILICON UNIJUNCTION TRANSISTORS

Type TO-18	Type TO-5	R_{BB} Interbase Resistance $V_{BB} = 3V$ $I_E = 0$	η Intrinsic Standoff Ratio $V_{BB} = 10V$	I_P (Max) Peak Point Emitter Current $V_{BB} = 25V$	I_{EO} (Max) Emitter Reverse Current $T_J = 25°C$	V_{OB1} (Min) Base One Peak Pulse Voltage	Comments	
		Kilohms	—	μa	μa	volts		
2N2417	2N489(1)	4.7-6.8	.51-.62	12	2.0	—	Industrial and Military Types	A versions are guaranteed in recommended circuit to trigger G.E. SCR's over range $T_A = -55°C$ to 125°C.
2N2417A	2N489A	↓	↓	12	2.0	3		
2N2417B	2N489B	↓	↓	6	0.2	3		
2N2418	2N490(1)	6.2-9.1	↓	12	2.0	—		
2N2418A	2N490A	↓	↓	12	2.0	3		
2N2418B	2N490B	↓	↓	6	0.2	3		
2N2419	2N491(1)	4.7-6.8	.56-.68	12	2.0	—		
2N2419A	2N491A	↓	↓	12	2.0	3		
2N2419B	2N491B	↓	↓	6	0.2	3		
2N2420	2N492(1)	6.2-9.1	.56-.68	12	2.0	—		
2N2420A	2N492A	↓	↓	12	2.0	3		
2N2420B	2N492B	↓	↓	6	0.2	3		
2N2421	2N493(1)	4.7-6.8	.62-.75	12	2.0	—		B versions in addition to SCR triggering, guarantees lower I_{EO} and I_P for long timing periods with a smaller capacitor.
2N2421A	2N493A	↓	↓	12	2.0	3		
2N2421B	2N493B	↓	↓	6	0.2	3		
2N2422	24N94(1)	6.2-9.1	↓	12	2.0	—		
2N2422A	2N494A	↓	↓	12	2.0	3		
2N2422B	2N494B	↓	↓	6	0.2	3		
—	2N494C	↓	↓	2	0.02	3		
—	2N1671	4.7-9.1	.47-.62	25	2.0	—	Industrial Types	
—	2N1671A	↓	↓	25	2.0	3		
—	2N1671B	↓	↓	6.0	0.2	3		
—	2N2160	4.0-12.0	.47-.80	25	2.0	3	Low Cost UJT (SCR Trigger)	
2N2646	—	4.7-9.1	.56-.75	5	2.0	3		
2N2647	—	4.7-9.1	.68-.82	2	0.2	6	For long timing periods & trigger high current SCR's	
			V_P					
2N2840	—	4.7-9.1(2)	1.3-1.5(2)	10(2)	1	—	Low Voltage Applications	

NOTES (1) Available as USAF TYPES (MIL-T-19500/75) (2) V_{BB} = 1.5 volts

CHAPTER 13

UNIJUNCTION TRANSISTOR CIRCUITS

The unijunction transistor (UJT) is a three-terminal semiconductor device which has electrical characteristics quite different from those of a conventional two-junction transistor. Its most important features are: (1) a stable triggering voltage (V_P) which is a fixed fraction of the applied interbase voltage, (2) a very low value of firing current (I_P), (3) a negative resistance characteristic which is uniform from unit to unit and stable with temperature and life, (4) a high pulse current capability, and (5) a low cost. These characteristics make the unijunction transistor advantageous in oscillators, timing circuits, voltage and current sensing circuits, SCR trigger circuits and bistable circuits.

The unijunction transistor is available in 47 distinct types to meet the needs of a wide range of applications. The chart on the opposite page shows 45 of these types as to package size, main parameter differences, and some general comments as to the circuit application for which they are characterized. Types 5E35 and 5E36 are not shown since they are characterized in a specific multivibrator circuit and are discussed later.

THEORY OF OPERATION

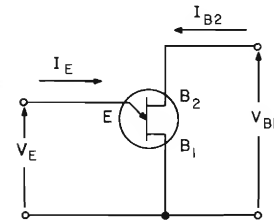
The symbol of the unijunction, Figure 13.1, and a simplified equivalent circuit, Figure 13.2, show a resemblance. R_{B2} plus R_{B1} represents the interbase resistance, R_{BB},

SYMBOL FOR UNIJUNCTION TRANSISTOR WITH IDENTIFICATION OF PRINCIPLE VOLTAGES AND CURRENTS

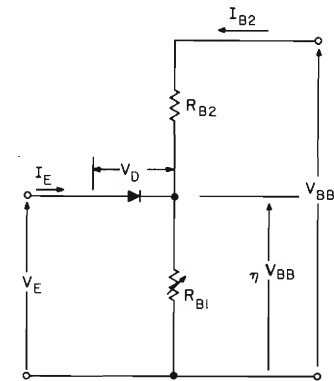
Figure 13.1

SIMPLIFIED EQUIVALENT CIRCUIT OF THE UNIJUNCTION TRANSISTOR

Figure 13.2

and is between 5K and 10K ohms. This is the resistance of an n-type silicon bar with ohmic contacts, called *base-one* (B1) and *base-two* (B2), at opposite ends. A single rectifying contact, called the *emitter* (E), is made between base-one and base-two. The diode in the simplified equivalent circuit of Figure 13.2 represents the unijunction's emitter diode. In normal circuit operation base-one is grounded and a positive

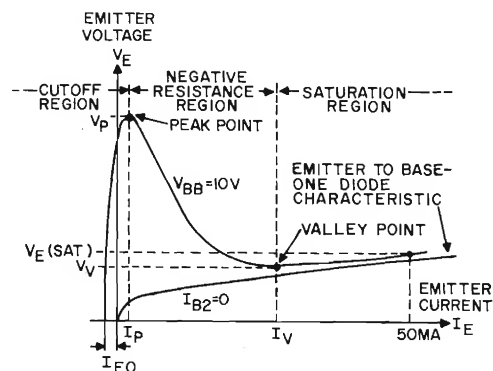
bias voltage, V_{BB}, is applied at base-two. With no emitter current flowing, the silicon bar acts like a simple voltage divider (Figure 13.2) and a certain fraction, η, of V_{BB} will appear at the emitter. If the emitter voltage, V_E, is less than ηV_{BB}, the emitter will be reverse biased and only a small emitter leakage current will flow. If V_E becomes greater than ηV_{BB}, the emitter will be forward biased and emitter current will flow. This emitter current consists primarily of holes injected into the silicon bar. These holes move down the bar from the emitter to base-one and result in an equal increase in the number of electrons in the emitter base-one region. The net result is a decrease in the resistance between emitter and base-one so that as the emitter current increases the emitter voltage decreases, and a negative resistance characteristic is obtained (Figure 13.3).

STATIC EMITTER CHARACTERISTIC CURVE SHOWING IMPORTANT PARAMETERS

Figure 13.3

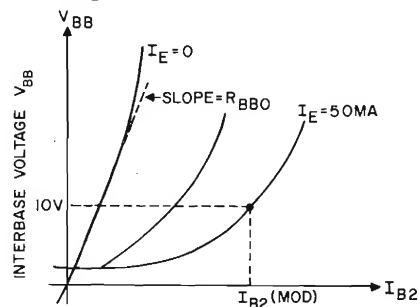
On the emitter characteristic shown in Figure 13.3 curve there are two points of interest, the *peak point* and the *valley point.* The region to the left of the peak point is called the *cut-off region*; here the emitter is reverse biased and only a small leakage current flows. The region between the peak point and the valley point is the *negative resistance region.* The region to the right of the valley point is the *saturation region*; here the dynamic resistance is positive.

BASE-TWO CURRENT STATIC INTERBASE CHARACTERISTICS CURVES

Figure 13.4

The electric field that exists between the base-two and base-one contacts is such that the majority of holes injected at the emitter will be swept toward the base-one contact. R_{B2} is also modulated but to a lesser degree than R_{B1} due to the direction of the electric field in the pellet. This characteristic is specified by measuring the current in base-two for a specified value of emitter current and interbase voltage. This parameter is defined by the symbol $I_{B2(MOD)}$. The resultant static characteristic curve is shown in Figure 13.4. It is important to note that in many applications a large value of peak power is developed between base-two and emitter and it is wise to use a current limiting resistor in series with base-two.

The resistance R_{B1} varies with the emitter current as indicated in Figure 13.5.

I_E (MA)	R_{B1} (OHMS)
0	4600
1	2000
2	900
5	240
10	150
20	90
50	40

VARIATION OF R_{B1} WITH I_E IN REPRESENTATIVE CIRCUIT (TYPICAL 2N492)

Figure 13.5

PARAMETERS — DEFINITION AND MEASUREMENT

1. Interbase Resistance (R_{BB}). The interbase resistance is the resistance measured between base-one and base-two with the emitter open circuited. It may be measured with any conventional ohmmeter or resistance bridge if the applied voltage is five volts or less. The interbase resistance increases with temperature at about 0.8%/°C. This temperature variation of R_{BB} may be utilized for either temperature compensation or in the design of temperature sensitive circuits.

2. Intrinsic Stand-off Ratio (η). This parameter is defined in terms of the peak point voltage, V_p, by means of the equation: $V_p = \eta V_{BB} + V_D$. A circuit which may be used to measure η is shown in Figure 13.6. In this circuit R1, C1 and the unijunction transistor form a relaxation oscillator and the remainder of the circuit serves as a peak voltage detector with the diode automatically subtracting the voltage V_D. To use the circuit, the "cal" button is pushed and R3 adjusted to make the meter read full scale. The "cal" button is then released and the value of η is read directly from the meter (1.0 full scale). If the voltage V_1 is changed, the meter must be recalibrated. Current limiting should be provided in the power supply to protect the unijunction transistor.

3. Peak Point Current (I_P). The peak point current corresponds to the emitter current at the peak point. It represents the minimum current which is required to trigger the unijunction transistor or required for oscillation in the relaxation oscillator circuit. I_P is inversely proportional to the interbase voltage. I_P may be measured in the circuit of Figure 13.7. In this circuit the potentiometer setting is slowly increased until the unijunction transistor fires as evidenced by a sudden jump and oscillation of the meter needle. The current reading just prior to when the jump takes place is the peak point current.

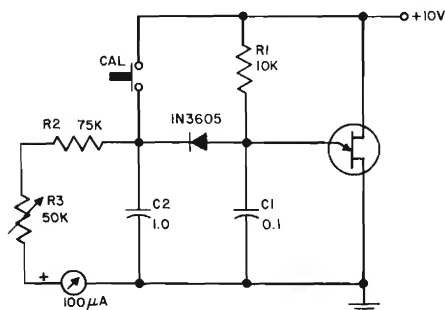
4. Peak Point Emitter Voltage (V_P). This voltage depends on the interbase voltage as indicated in 2. V_P decreases with increasing temperature because of the change in V_D and may be stabilized by a small resistor in series with base-two.

5. Emitter Saturation Voltage (V_E (sat). This parameter indicates the forward drop of the unijunction transistor from emitter to base-one in the saturation region. It is measured at an emitter current of 50 ma and an interbase voltage of 10 volts.

6. Interbase Modulated Current (I_{B2} (mod). This parameter indicates the effective current gain between emitter and base-two. It is measured as the base-two current under the same condition used to measure V_E (sat).

7, Emitter Reverse Current (I_{EO}). The emitter reverse current is measured with an applied voltage between base-two and emitter with base-one open circuit. This current varies with temperature in the same way as the I_{CO} of a conventional transistor.

8. Valley Voltage (V_V). The valley voltage is the emitter voltage at the valley point. The valley voltage increases as the interbase voltage increases, it decreases with resistance in series with base-two and increases with resistance in series with base-one.

9. Valley Current (I_V). The valley current is the emitter current at the valley point. The valley current increases as the interbase voltage increases and decreases with resistance in series with base-one or base-two.

TEST CIRCUIT FOR INTRINSIC STANDOFF RATIO (η)

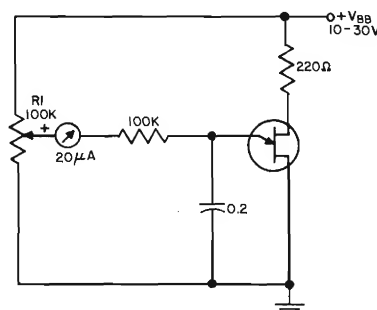



Figure 13.6

TEST CIRCUIT FOR PEAK POINT EMITTER CURRENT (I_p)

Figure 13.7

CONSTRUCTION

The unijunction types shown in the chart at the beginning of this chapter are from two basic unijunction structures which we shall identify as *bar* and *cube* structures. The 2N2646, 2N2647, and 2N2840 types are the cube structure (5E production line), and all the remaining types are bar structure.

A cross-sectional view of the bar unijunction transistor structure is shown in Figure 13.8(A). A ceramic disc having the same thermal expansion coefficient as silicon is used as a mounting platform. The pellet is a single crystal of n-type silicon with dimensions of 8 x 10 x 60 mils. The pn emitter junction is formed by alloying a 3 mil aluminum wire to the top of the pellet nearest the base-two ohmic contact. The resultant device is then surface passivated and hermetically sealed. This design permits T0-5 and T0-18 package sizes with all leads electrically isolated from the case.

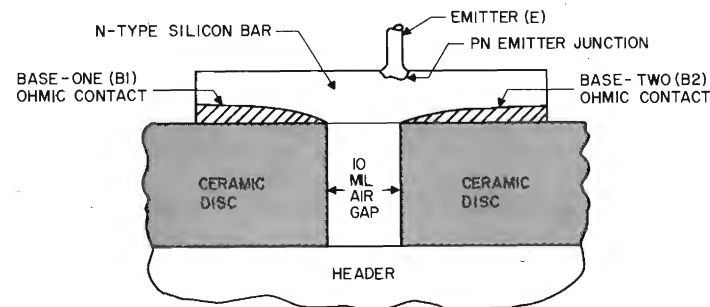
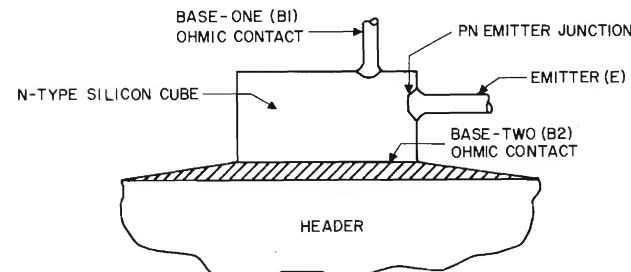
A cross-sectional diagram of the cube unijunction transistor structure is shown in Figure 13.8(B). The pellet consists of single crystal of n-type silicon having dimensions of 13 x 17 x 17 mils. It is mounted directly to the top of a gold-plated kovar header. Thus base-two is common to the header and case. The base-one ohmic contact is formed by alloying a wire, 2 mils in diameter, into the top surface of the pellet. This alloy ohmic contact has a shape which is a section of a sphere giving rise to a non-linear voltage gradient between base-one and base-two. The pn emitter junction

CROSS SECTIONAL VIEWS OF UNIJUNCTION STRUCTURES

Figure 13.8

is formed by alloying an aluminum wire, 3 mils in diameter, into the side of the pellet. The resultant unit is surface passivated and hermetically sealed in a T0-18 size package. Because of the geometry of the small area ohmic contact used for base-one, the voltage gradient in the vicinity of base-one is higher than elsewhere in the silicon, so it is possible to achieve a high standoff ratio with a much smaller spacing between emitter and base-one. This then permits the cube structure to have lower peak point current, turn-on time, and lower emitter saturation voltage with a large base-one peak pulse for triggering silicon controlled rectifiers (SCR). This design also makes possible unijunction operation at low voltage. Cube structure unijunctions, in general, have a lower valley point and a larger value of negative resistance (see Figure 13.9). This results in excellent switching action for this device with its low saturation voltage and high negative resistance. Also, a larger voltage swing may be derived from the cube structure in such applications as oscillators and pulse generators than for the bar structure with a comparable intrinsic standoff ratio. At the same time one must consider the lower valley current of the 2N2646 (cube) with regard to *lock-up* of a circuit in the saturation region by allowing the emitter to supply a steady state current in excess of the valley current.

The electric field gradient between base-one and base-two of the bar structure is essentially linear in contrast to that of the cube. Even with this difference, however,

STATIC EMITTER CHARACTERISTICS T_A = +25°C

V_{BB} = 30V

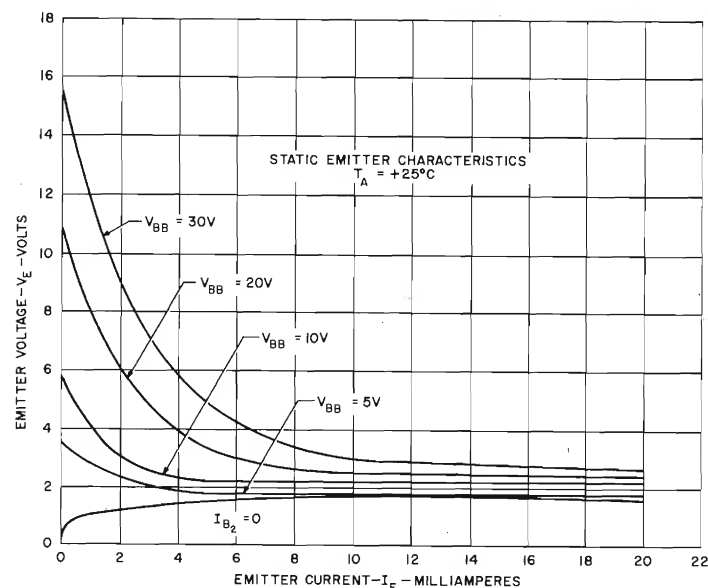
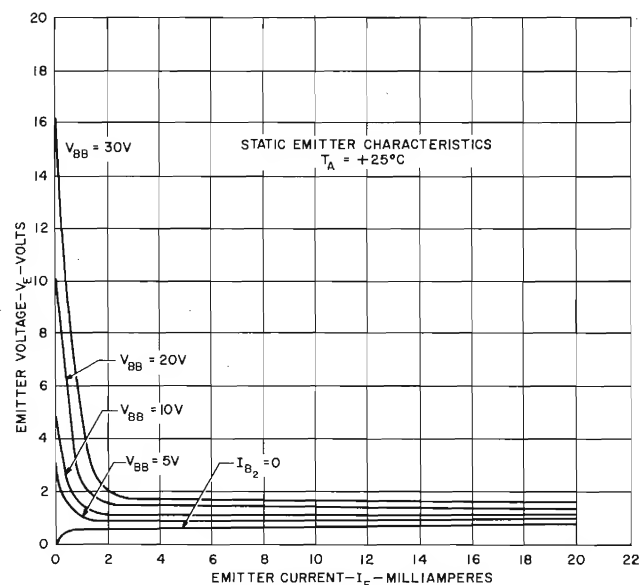
V_{BB} = 20V

V_{BB} = 10V

V_{BB} = 5V

I_{B_2} = 0

EMITTER VOLTAGE-V_E-VOLTS

EMITTER CURRENT-I_E-MILLIAMPERES

(A) BAR STRUCTURE

(B) CUBE STRUCTURE

TYPICAL STATIC EMITTER CHARACTERISTIC CURVES AT 25°C FOR BAR AND CUBE STRUCTURES

Figure 13.9

the interbase resistance characteristics (R_{BB}) of the two structures, for allowable values of voltage and temperature, are essentially identical. The positive temperature coefficient of R_{BB} improves the thermal stability of the unijunction at junction temperatures below 150°C. Of the two structures, the bar structure unijunction types exhibit more stable characteristics at extreme junction temperatures (beyond −40°C and +100°C).

IMPORTANT UNIJUNCTION CHARACTERISTICS

PEAK POINT

The most important characteristic of the unijunction is the *peak point* characteristic since it determines the triggering voltage in bistable circuits, the threshold level in sensing circuits, and the frequency of relaxation oscillators. *Peak point voltage* (V_P) is proportional to the interbase bias voltage and is

$$V_P = \eta V_{BB} + V_D \qquad (13a)$$

where V_D is the voltage drop across the emitter diode with a forward current equal to the peak point current. Generally V_P is not measured directly but is obtained by measurement of η in test circuits such as Figure 13.6. At 25°C the diode voltage for the cube structure is typically 0.4 volt compared with 0.67 volt for the bar structure.

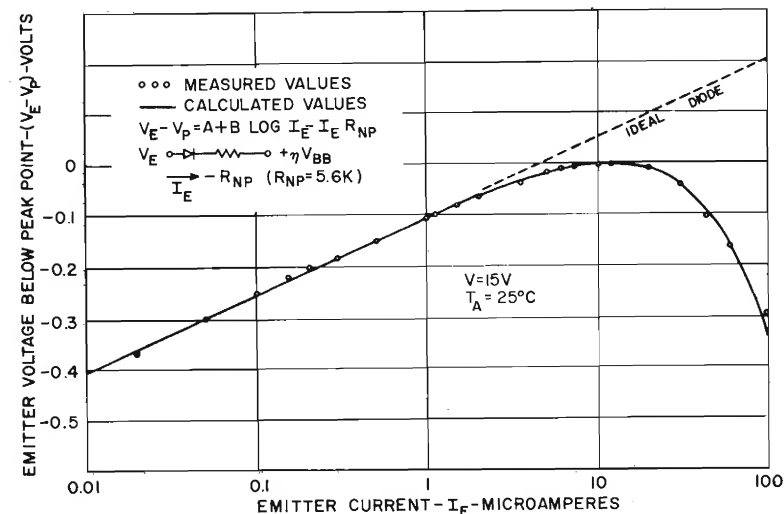
The peak point characteristic for a typical UJT (bar structure) is shown on an expanded scale in Figure 13.10. The solid line in this figure indicates the V-I characteristic calculated for a silicon diode in series with a fixed value of negative resistance. The value of the emitter current at the point where the peak point characteristic has a zero slope is defined as the peak point current (I_P).

UNIJUNCTION TRANSISTOR STATIC EMITTER CHARACTERISTICS AT PEAK POINT

Figure 13.10

PEAK POINT TEMPERATURE STABILIZATION

The principal variation of V_P with temperature is due to the variation of V_D for the bar structure, since the η variation is negligible. This effect may be compensated

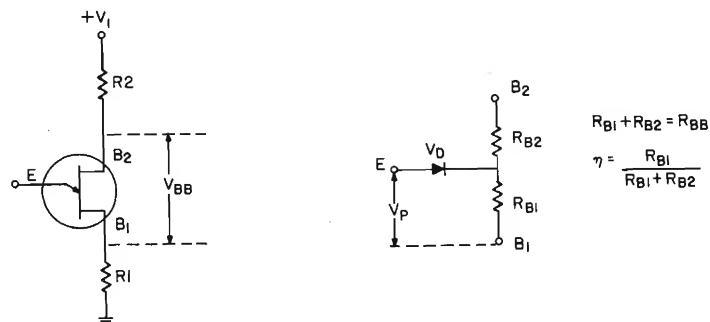



Figure 13.11

by means of a smaller resistor (R2) as shown in Figure 13.11. As the ambient temperature increases the interbase resistance (R_{BB}) will increase and V_{BB} will also increase due to the voltage divider action of R2, R_{BB} and R1.

If R2 is chosen correctly the increase in interbase voltage will compensate for the decrease in V_D. The approximate value of R2 is

$$R2 \cong \frac{0.70\, R_{BB}}{\eta V_1} \tag{13b}$$

If R2 satisfies this equation the peak point voltage will be given by

$$V_P = \eta V_1 \tag{13c}$$

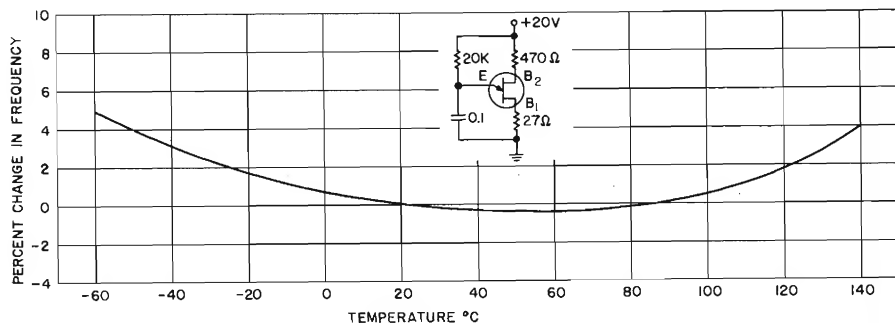
In a following discussion on valley point it will be shown in Figure 13.16 that it is generally desirable to keep the value of R1 in Figure 13.11 less than 100 ohms. This is the condition under which equation (13b) is valid. Figure 13.12 shows a typical variation of relaxation oscillator frequency with temperature where the UJT was the only component submitted to the varying ambient temperature. Frequency stability could be improved if the other components had compensating temperature coefficients. The value of the compensating resistor in series with base-two was selected using equation (13b).

UNIJUNCTION ONLY SUBMITTED TO TEMPERATURE

Figure 13.12

When circuit operation over the extreme temperature range (−60 to +140°C) is not required better compensation can be achieved. The reason being that the temperature coefficient of the UJT is not perfectly linear, and over a more limited range the actual slope of the temperature coefficient can be compensated more accurately with R2. For temperatures below 100°C more accurate compensation can be obtained by using a smaller value for R2; this is given by equation (13d).

2N489 series 2N1671 series 2N2417 series

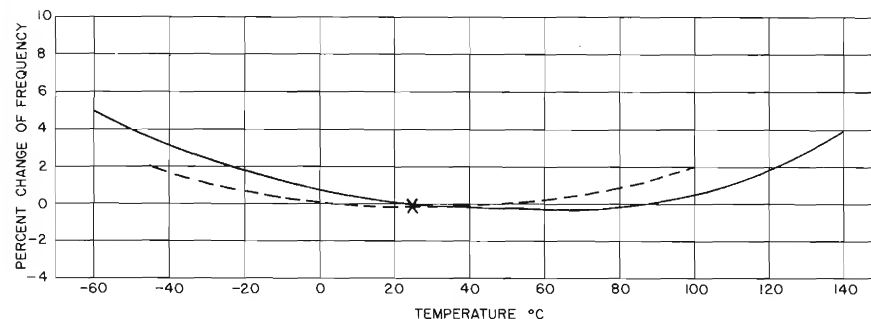
$$R2 \cong \frac{0.4\, R_{BB}}{\eta\, V_1} \tag{13d}$$

TYPICAL FREQUENCY VS TEMPERATURE CURVE

Figure 13.13

The solid curve in Figure 13.13 is the same as Figure 13.12. If the value of R2 is decreased it causes the curve to rotate counter-clockwise with 25°C as the pivot point (see dashed curve). Thus, if the temperature range of interest is from −45°C to 100°C, then the value of R2 can be decreased to compromise between the ½% deviation at 100°C and the 3½% at −45°C, to give approximately 2% at each temperature extreme as shown by the dashed curve of Figure 13.13.

Each individual unijunction has its own value of R2 that gives best compensation. Therefore using one fixed value of R2 for a group of unijunctions, one would expect the majority to follow a curve similar to that of Figure 13.13, with a scattering at the more extreme temperature on each side. The best average value of resistance can be determined for R2 by taking a random sample of unijunctions, and then determining the average fixed resistance which compensates best over the desired temperature range. With this general compensation method, one should be able to attain a frequency stability of better than 2% for most all of the units over a temperature range of 0°C to 100°C. Typically the stability should be better than ½%.

If the compensating resistor (R2) is adjusted or selected for each unit (by placing the circuit in an oven and adjusting R2 of each circuit) the frequency change from 0°C to 100°C will generally be less than ¼% (all units under 1%). It is easier and often adequate to place a thermal probe on the UJT and adjust R2 for minimum frequency change from room ambient conditions. This method gives very good results when the values of the resistors and capacitors are quite stable with temperature.

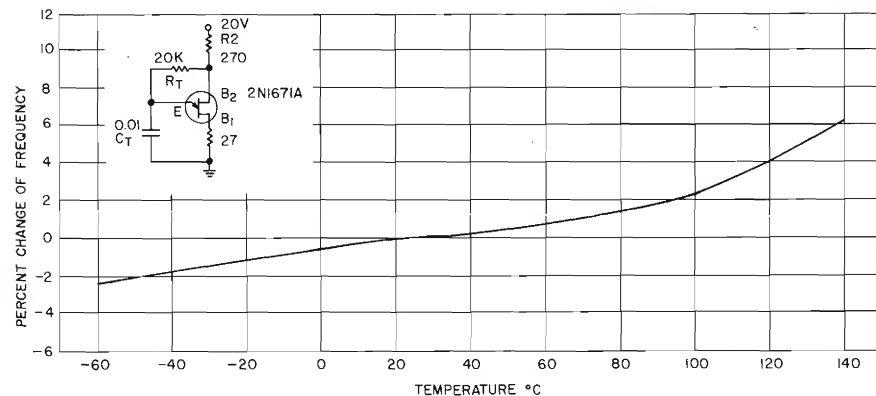
If a stability of better than 0.05% is required over a wide ambient temperature range, then the complete relaxation circuit can be operated in a small components (crystal) oven.

TYPICAL FREQUENCY VS TEMPERATURE (UJT ONLY SUBMITTED TO TEMPERATURE)

Figure 13.14

Stability at temperatures below 25°C can be improved by returning R_T to base-two of the UJT as shown in Figure 13.14. R2 may be tapped at an optimum point for best temperature compensation for the particular supply voltage and temperature range.

The circuit mode used in Figure 13.14 offers another advantage in that the temperature characteristic is more linear making compensation easier. In fact, the temperature characteristic of a mylar capacitor compliments the curve in Figure 13.14, and is about the right compensation when used as C_T for a temperature range of —25°C to +85°C.

In some applications a diode has been used in series with either base-two or the emitter of the unijunction to improve the temperature stabilization or to reduce the dependance on power supply variation.

The foregoing discussion on bar construction types applies in general to the cube structure also, except that the 2N2646 and 2N2647 (5E production line) types have a greater variation of η with temperature. Therefore, this has to be considered along with the variation of V_D and requires a larger value for R2 to temperature compensate these types. R2 for the most usual ambient temperature requirements is given by

$$\left.\begin{array}{l}\text{2N2646}\\ \text{2N2647}\end{array}\right\} R2 = \frac{10{,}000}{\eta\, V_1} \qquad (13e)$$

Figure 13.15 shows a temperature characteristic that is typical for the 2N2647 with a value for R2 as given in equation (13e). It is expected that a few units may depart considerably from this curve. Such units would require a lower value resistor for R2 if they fall below the curve at 100°C and a larger value resistor for R2 if they fall above the curve.

In the preceding discussion of UJT oscillator frequency stability vs. temperature, although the primary consideration has been to stabilize the peak point, the valley point also is involved in the total compensation.

VALLEY POINT

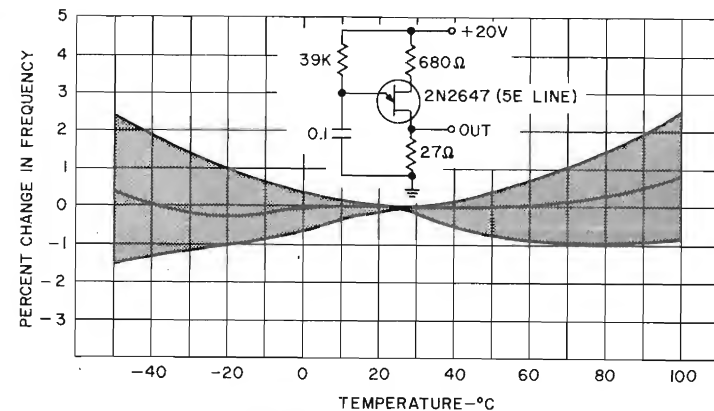
Both the valley point and the shape of the negative resistance characteristics are circuit dependent and may be varied over a moderate range by choice of suitable

2N2647 TEMPERATURE CHARACTERISTIC

Figure 13.15

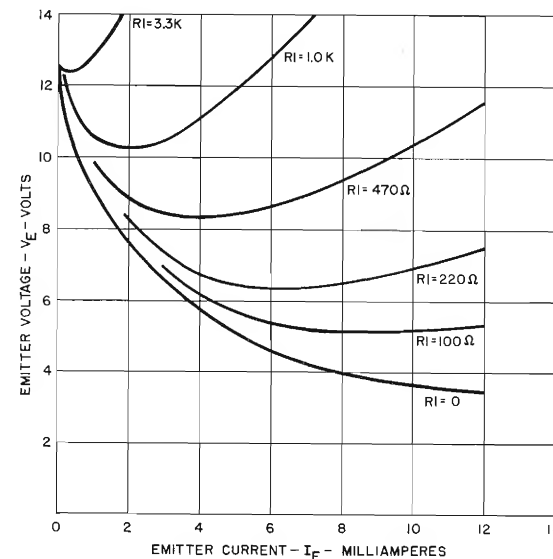
circuitry. For example, valley voltage may be increased by increasing the interbase voltage, by increasing the resistor in series with base-one, or by decreasing the resistor in series with base-two. Similarly, valley current may be increased by increasing the interbase voltage, by decreasing the resistance in series with base-one, or by decreasing the resistance in series with base-two. Th emitter characteristics for different values of base-one series resistance are shown in Figure 13.16. The emitter characteristics for different values of base-two series resistance are shown in Figure 13.17. In

EMITTER CHARACTERISTIC CURVES FOR TYPE 2N492 UNIJUNCTION TRANSISTOR WITH BASE-ONE SERIES RESISTANCE

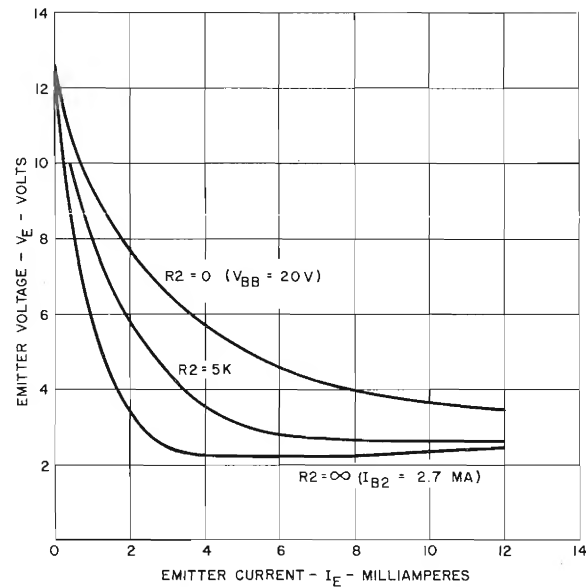
Figure 13.16

EMITTER CHARACTERISTIC CURVES FOR TYPE 2N492 UNIJUNCTION TRANSISTOR WITH BASE-TWO SERIES RESISTANCE

Figure 13.17

taking the data for Figures 13.16 and 13.17, the bias voltage, V_1, was adjusted to give the same peak point voltage. In regard to Figure 13.17, the curves for all possible values of base-two series resistor lie between the curve for constant interbase voltage and the curve for constant interbase current. The range of valley voltage and valley currents are determined by the valley points on these two curves.

POWER DISSIPATION RATINGS

The power rating of the UJT is given in terms of the total dissipation which is the sum of the emitter dissipation and the interbase dissipation.

It is important or provide circuit stabilization in the interbase circuit when the UJT is used in pulse type applications since the instantaneous temperature of the silicon could rise to a high enough value to permit runaway if the interbase current is not limited by R2.

Measurement of the thermal resistance of the UJT in a particular socket or heat sink is best accomplished by making use of R_{BB} as the temperature sensitive parameter.

RELAXATION OSCILLATOR

CIRCUIT OPERATION

The relaxation oscillator circuit shown in Figure 13.18 is a basic circuit for many applications. It is useful as a timing circuit, a pulse generator, a trigger circuit, or a sawtooth wave generator.

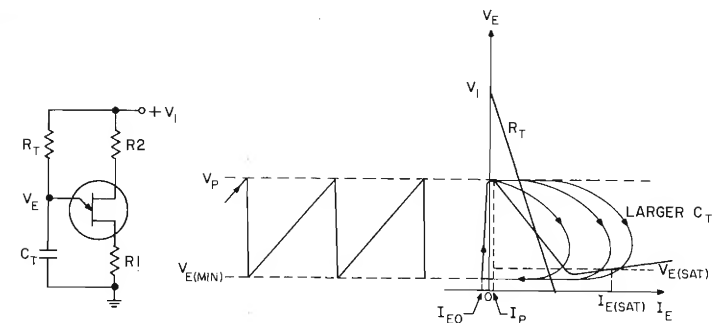
At the beginning of an operating cycle the emitter is reverse-biased and hence non-conducting. As the capacitor C_T is charged through the resistor R_T the emitter voltage rises exponentially towards the supply voltage V_1. When the emitter voltage

BASIC RELAXATION OSCILLATOR WITH TYPICAL WAVEFORMS

Figure 13.18

reaches the peak point voltage V_P the emitter becomes forward biased and the dynamic resistance between the emitter and base-one drops to a low value. Capacitor C_T then discharges through the emitter. When the emitter voltage reaches $V_{E(MIN)}$, as shown in Figure 13.18, the emitter ceases to conduct and the cycle is repeated.

$V_{E(MIN)}$ is the minimum emitter voltage and is relatively independent of bias voltage, temperature, and capacitance if R1 is zero. $V_{E(MIN)}$ is approximately equal to 0.5 $V_{E(sat)}$. For small values of R1 and R2 the frequency of oscillation is

$$f \cong \frac{1}{R1\, C \ln\left(\frac{1}{1-\eta}\right)} \qquad (13f)$$

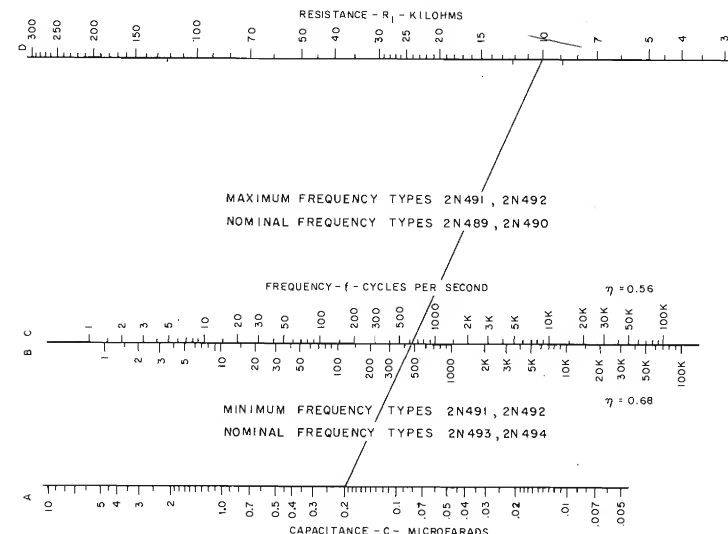
and may be obtained conveniently from the nomogram of Figure 13.19.

NOMOGRAM FOR CALCULATING FREQUENCY OF RELAXATION OSCILLATION

Figure 13.19

OSCILLATION REQUIREMENTS AND COMPONENT LIMITS

The UJT relaxation oscillator is noteworthy for its ability to operate over a wide range of circuit parameters and ambient temperature. There are, however, several important conditions which must be satisfied if this circuit is to operate satisfactorily:

1. The load line formed by the resistor R_T and the supply voltage V_1 must intersect the emitter characteristic curve to the right of the peak point. This condition ensures that the resistor R_T can supply sufficient current to the emitter to trigger the UJT. This condition may be written

$$\frac{V_1 - V_P}{R_T} > I_P \quad (13g)$$

I_P is generally specified at an interbase voltage of 25 volts and is inversely proportional to V_{BB}. Equation (13g) sets a maximum limit on R_T so that R_T must be chosen to satisfy the inequality under the worst conditions for each of the other parameters. The worst conditions would include, (a) the maximum value of V_P, (b) the minimum value of V_1, and (c) the maximum value of I_P at the minimum temperature of operation.

The limit value of R_T can be greatly increased by supplying an externally generated negative pulse at base-two. This will be discussed later under both time delay and sensing circuits.

2. The second condition which must be satisfied is that the load line formed by R_T and the supply voltage V_1 must intersect the emitter characteristic to the left of the valley point.

$$\frac{V_1 - V_V}{R_T} < I_V \quad \text{(where } V_V \text{ is circuit dependent and should be measured in the actual circuit)} \quad (13h)$$

If this condition is not satisfied the load line will intersect the emitter characteristic curve in the saturation region and the UJT may not turn off after it triggers on the first cycle. Note that the valley current given in equation (13h) refers to the valley current of the UJT in the circuit together with the base-one and base-two series resistors. If these external resistors are large the value of I_V will be reduced as indicated in Figure 13.16 and 13.17.

In general the limitations imposed by condition 1 and 2 are not severe. A maximum value of I_P might be 2 microamperes and a minimum value of I_V might be 8 milliamperes so that the allowable range of R_T should be 1000 to 1 (approximately 3K to 3 Meg).

3. A final condition for the operation of the UJT relaxation oscillator concerns the allowable range of capacitance C_T. As the size of C_T is decreased below about 0.01 μfd (0.001 μfd for 2N2646 and other 5E production line types) the amplitude of the emitter voltage waveform will decrease as indicated in Figure 13.20. This decreases the frequency stability of the circuit and also reduces the allowable range of R_T.

The emitter peak current should not exceed two amperes for values of C_T less than 10 μfd and peak point voltages less than 30 volts. For higher values of C_T or V_P, resistance should be used in series with the capacitor to protect the emitter circuit. This additional series resistance should be at least one ohm per microfarad of C_T.

TRANSIENT WAVEFORM CHARACTERISTICS

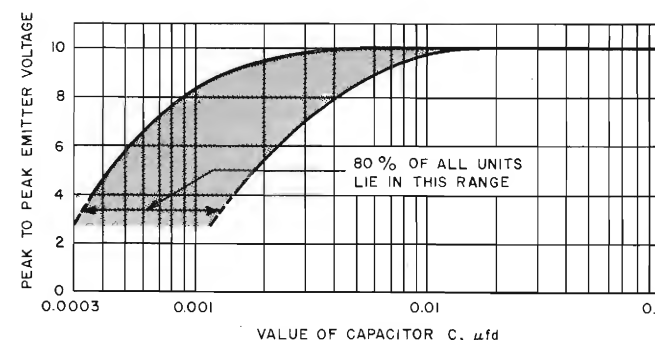
In a UJT relaxation oscillator circuit the most important transient characteristic is the emitter voltage fall-time (t_f), or turn-on time. This is shown on unijunction specification sheets as *Emitter Voltage Fall-time (t_f) Microseconds vs. Capacitance (C_1) Microfarads,* C_1 being the emitter capacitor and sometimes referred to as C_T. The fall-time is found to be independent of the supply voltage and is determined

VARIATION OF PEAK TO PEAK EMITTER VOLTAGE WITH CAPACITANCE IN UNIJUNCTION RELAXATION OSCILLATOR

Figure 13.20

primarily by the value of the capacitor C_T and the ambient temperature, T_A. For values of R1 other than zero the fall-time will be increased in proportion to the time constant R1 C_T.

PULSE GENERATION

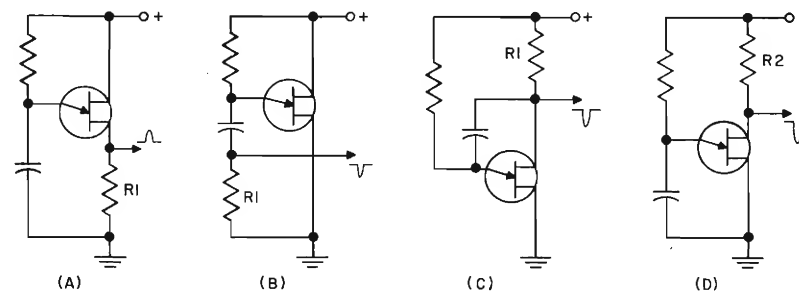
Each time the UJT in the relaxation oscillator circuit conducts, a current pulse flows in the emitter, base-one, and base-two circuits. The relaxation oscillator can be used as an efficient pulse generator which may be used to generate either positive or negative pulses at various impedance levels. Various configurations of the pulse generator are shown in Figure 13.21. The first three configurations (A, B, C) use the discharge current of the capacitor to generate the pulse and hence have a low output impedance. The configuration shown in 13.21(D) uses the base-two current to generate the pulse and has a higher output impedance although this configuration is capable of generating higher voltages. In configuration 13.21(C) it is important to note that the capacitor discharge current flows through the external supply so that a low impedance power supply is required.

CONFIGURATIONS OF THE RELAXATION OSCILLATOR FOR USE AS PULSE GENERATORS

Figure 13.21

The emitter current pulse width, measured between the 10% points, is approximately equal to 2 t_f. For small values of R1 the peak emitter current is given ap-

proximately by

$$I_{E\,(PEAK)} \cong \frac{[V_p - 1/2\ V_E(sat)]C_T}{t_t} \qquad (13i)$$

and the corresponding base-two current is given approximately by

$$I_{B2\,(PEAK)} \cong \frac{I_{B2\,(MOD)}}{7}\sqrt{I_{E\,(PEAK)}} \qquad (13j)$$

where the units are ma, volts, mμf, and μsec.

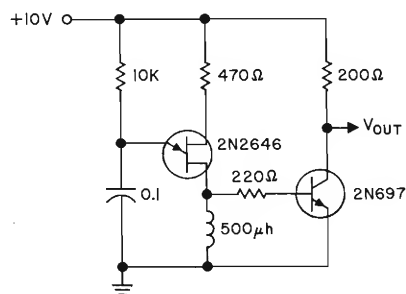
The output pulse from a conventional UJT relaxation oscillator has a moderately fast rise-time and a very slow fall-time. In applications where a well shaped pulse is required with controlled width and fast rise and fall times the use of an inductance as shown in the circuit of Figure 13.22 can yield a significant improvement over the conventional resistance coupled circuit. The inductance is given approximately by $0.4t^2/C$ where t is the desired pulse width and C is the value of the emitter capacitor.

UJT PULSE SHAPING CIRCUIT

Figure 13.22

For the circuit shown the pulse width for various transistors fell between 11 and 12 microseconds and the rise and fall times were typically 0.3 microseconds. With a 47 ohm resistor substituted for the inductance the rise-time was typically 0.3 microseconds, but the fall-time was typically 3 microseconds.

FREQUENCY STABILITY

Frequency variation of the relaxation oscillator with temperature is discussed in a previous section on Peak Point Temperature Stabilization. The base-two circuit resistor, R2, which is normally selected to stabilize the oscillator frequency with temperature also is adequate for stabilizing the frequency for supply voltage variations. Frequency change is usually less than ±1% with supply variations up to ±25%.

SYNCHRONIZATION

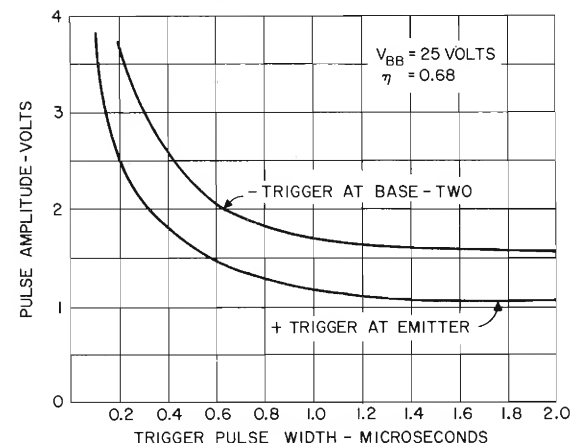
The UJT relaxation oscillator can be synchronized by means of either positive pulses at the emitter or negative pulses at base-two. Amplitude of the synchronizing pulses must be large enough to reduce the peak point voltage below the instantaneous emitter voltage according to equation (13a). The effect of pulse width on the required trigger amplitude is shown in Figure 13.23. For pulse widths greater than 1 microsecond the required trigger amplitude approaches the dc conditions, for pulse widths of less than 1 microsecond the required pulse amplitude is inversely proportional to the pulse width. The equivalent electric charge required for triggering is approximately 10^{-9} coulombs for the bar structure and 10^{-10} coulombs for the cube structure.

MINIMUM TRIGGER AMPLITUDE AS A FUNCTION OF TRIGGER PULSE WIDTH FOR TURN ON OF UNIJUNCTION TRANSISTOR

Figure 13.23

SAWTOOTH WAVE GENERATORS

GENERAL CONSIDERATIONS

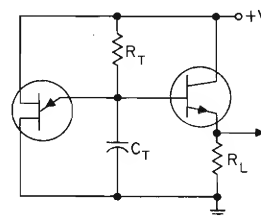
The voltage waveform at the emitter of the UJT in the basic relaxation oscillator is a fair approximation to a sawtooth waveform. The most practical method to couple this signal to a load is by the use of a direct-coupled emitter follower as shown in Figure 13.24. It will be noted that simple direct coupling is made possible by the fact that the minimum emitter voltage at the emitter of the UJT, $V_{E\,(MIN)}$, is 1.0 volt or more. If $V_{E\,(MIN)}$ is less than the normal base to emitter drop of the junction transistor, then the waveform across the load, R_L, will be clipped at the bottom.

UNIJUNCTION SAWTOOTH GENERATOR WITH NPN EMITTER FOLLOWER OUTPUT STAGE

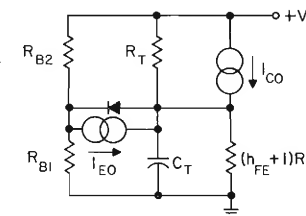
Figure 13.24

EQUIVALENT CIRCUIT FOR CALCULATION OF TEMPERATURE AND LOADING EFFECTS

Figure 13.25

The first order effects of the emitter follower output stage on the voltage waveform are indicated in the equivalent circuit of Figure 13.25. The loading effect of the emitter follower stage is approximated by an equivalent circuit $(h_{FE} + 1)\ R_L$ across the capacitor C_T. It is seen from this equivalent circuit that loading will change the frequency of oscillation since the capacitor charging circuit will be changed by the

presence of the resistor $(h_{FE} + 1)\ R_L$. To minimize the effects of loading on the frequency, the value of R_L and h_{FE} should be as large as possible. If the values of h_{FE} or R_L are too small, the circuit will not oscillate. To ensure oscillation h_{FE} and R_L must satisfy the condition,

$$\frac{(h_{FE}+1)\ R_L}{R_T + (h_{FE}+1)\ R_L} > \eta_{(MAX)} \qquad (13k)$$

TEMPERATURE EFFECTS

Two important temperature effects are involved in the use of the emitter-follower output stage. The variation in h_{FE} with temperature will change the loading and effect the frequency of oscillation; to minimize this temperature effect, $(h_{FE} + 1)\ R_L$ should be much greater than the resistor R_T. The second temperature effect results from the collector leakage current, I_{CO}, of the junction transistor as indicated in Figure 13.25. It will be noted that this current adds to the emitter leakage current, I_{EO}, of the UJT. Both of these leakage currents tend to increase the frequency as temperature increases. The effect of the leakage currents on the frequency can be minimized by using a large capacitor C_T. If the NPN transistor is silicon, the effects of the two leakage currents can generally be neglected at temperatures below 100°C.

Some improvement in circuit operation can be achieved by the use of an PNP emitter follower output stage. For this circuit configuration the effective load resistance, $(h_{FE} + 1)\ R_L$, is in parallel with R_T so that the possibility of nonoscillation due to low values of h_{FE} or R_L is eliminated. Another advantage is that the I_{CO} of the transistor subtracts from I_{EO} of the UJT so that some degree of temperature compensation is obtained. This is particularly true if a silicon transistor is used as the PNP output transistor.

IMPROVING LINEARITY

For many applications the linearity obtained with the basic UJT relaxation oscillator is inadequate. To achieve the best linearity with the basic circuit, it is necessary to use a UJT having the minimum value of η (types 2N489, 2N490). The best linearity which can be obtained with these types is about 10%.

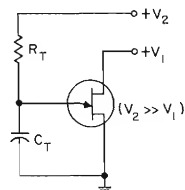
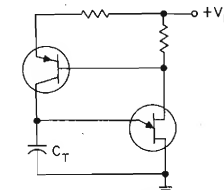
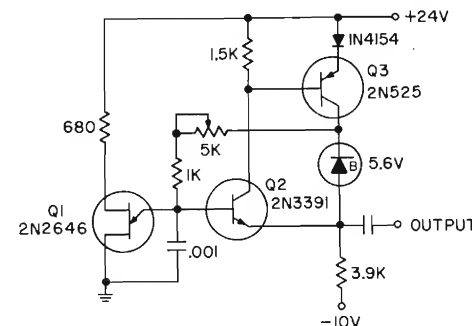
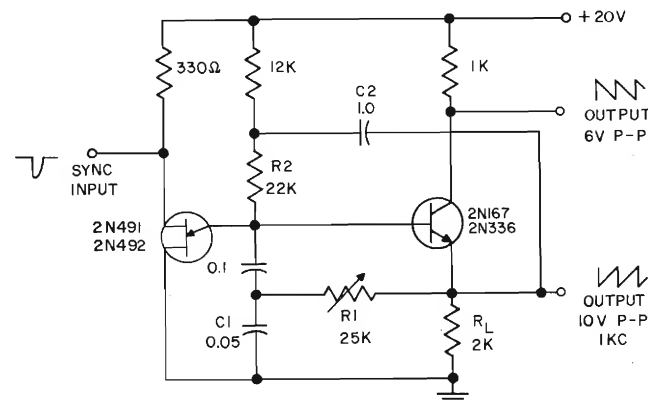
A number of simple circuit techniques can be used to improve the linearity of the sawtooth waveform. The direct approach of using a higher supply voltage for charging the timing capacitor is illustrated in Figure 13.26(A). This is an inexpensive method of improving linearity if a high voltage supply is available in the system under design. It suffers from the disadvantage that the frequency would not be as stable as it would with a single power supply.

TWO CIRCUITS FOR IMPROVING LINEARITY OF SAWTOOTH GENERATORS
Figure 13.26

Figure 13.26(B) illustrates the use of the high output impedance of a common-base transistor to maintain a constant charging current for the capacitor.

LINEAR SAWTOOTH WAVE GENERATORS

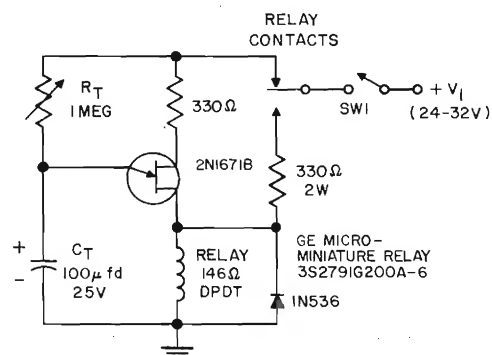
Two variations of a bootstrap charging circuit are shown in Figures 13.27 and 13.28. In 13.27 a constant voltage is maintained across the charging resistor by the zener diode and the emitter follower transistor amplifier stage so that the capacitor charging current is constant over the complete cycle. This circuit is quite economical in that it makes double use of the transistor, both as the driver for the bootstrap circuit and as an output amplifier stage. Note that the 3.9K load resistor is returned to a negative voltage to prevent clipping at the bottom of the sawtooth waveform. Q3 maintains the zener current constant for improved linearity and also assists Q2 in supplying current to the load. The circuit will generate a linear sawtooth up to 50 kc.

50 KC SAWTOOTH GENERATOR
Figure 13.27

The circuit shown in Figure 13.28 makes use of a capacitor in place of the zener diode. This variation permits the negative supply to be eliminated. The NPN transistor serves as an output buffer amplifier with the capacitor C2 and resistor R2 serving in a bootstrap circuit to improve the linearity of the sawtooth. R1 and C1 act as an integrating network to provide second order compensation for the non-linearity of the waveform. By varying the value of R1 the output waveform can be made concave upward, concave downward, or linear.

SAWTOOTH GENERATOR WITH HIGH LINEARITY
Figure 13.28

The feedback networks in Figure 13.28 are frequency sensitive. C2 will not be effective at low frequencies and the effective emitter capacity can not be much less than .01 μf without affecting the linearity and operation at the higher frequencies. C1 could be reduced to about .001 μf by using the higher frequency type 2N2647.

PRECISION TIMING CIRCUITS

TIME DELAY RELAY

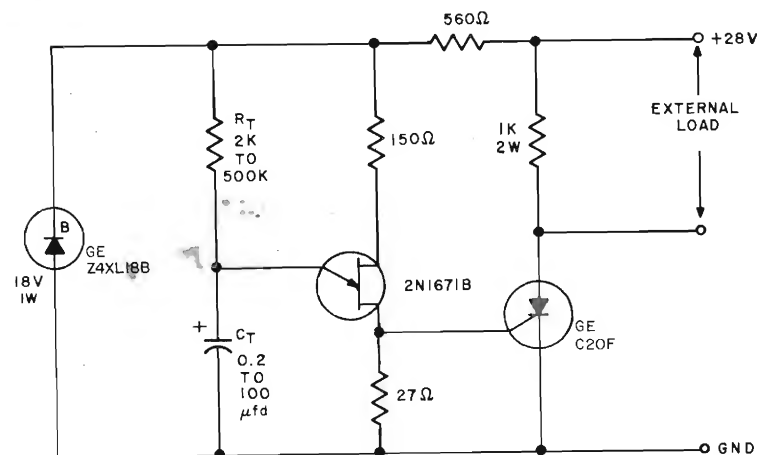
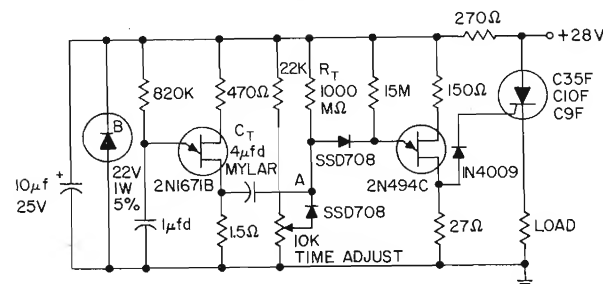
Figure 13.29 shows how the unijunction transistor can be used to obtain a delay in the operation of a relay. When the switch SW1 is closed, capacitor C_T is charged to the peak point voltage at which time the unijunction triggers and the capacitor discharges through the relay causing it to close. One set of relay contacts holds the relay closed and the second set of contacts can be used for control functions. To be used in this circuit, relays must have fast operating times, low coil resistance and low operating power.

TIME DELAY CIRCUIT WITH RELAY
Figure 13.29

The time delay of this circuit is determined by R_T, about one second of delay for each 10K of resistance. The time delay is quite independent of temperature and supply voltage.

PRECISION SOLID STATE TIME DELAY CIRCUITS

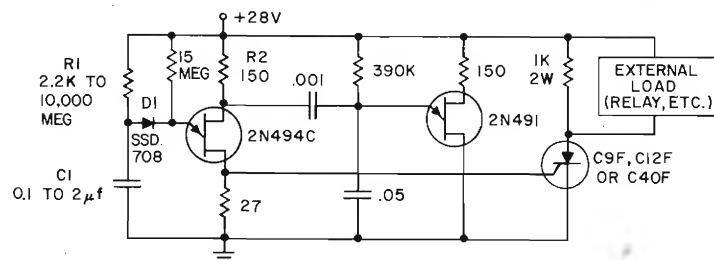
Figure 13.30 illustrates a typical time delay circuit using the unijunction transistor together with a low cost SCR. The timing interval is initiated by applying power to the circuit. At the end of the timing interval, which is determined by the value of R_TC_T, the unijunction triggers the SCR and the full supply voltage minus about one volt is applied to the load. By suitable choice of R_T and C_T this circuit will give time delays from 0.4 milliseconds to 1 minute. Load currents are limited only by the rating of the SCR; up to 6 amperes for the C20F (stud mounted). Use of a precision calibrated resistor such as helipot in place of R_T permits the time delay to be set accurately over a wide range after one initial calibration.

The timing resistor in a conventional UJT time delay circuit must be small enough to supply the minimum trigger current (I_P) of the UJT plus the leakage current of the timing capacitor when the UJT emitter is biased at its peak point voltage. The 2N494C has a maximum I_P requirement of 2 μa. This places a limit of 3 megohms on R_T and for $C_T = 4$ μf permits time delays to 12 seconds with a conventional circuit.

The circuit shown in Figure 13.31 reduces the effective trigger current by a factor

SOLID STATE TIME DELAY CIRCUIT
Figure 13.30

ONE HOUR TIME DELAY CIRCUIT
Figure 13.31

of more than 1000 and allows time delays of up to 1 hour to be achieved with a low leakage 4 μfd mylar capacitor. This is achieved by periodically sampling the voltage on the timing capacitor. Between samples the timing capacitor is isolated from the emitter of the UJT by ultra-low leakage planar silicon diodes (the SSD-708 has a leakage current of less than 20 picoamperes at 25°C). The sampling pulse is generated by a UJT relaxation oscillator operating at approximately 2 cps.

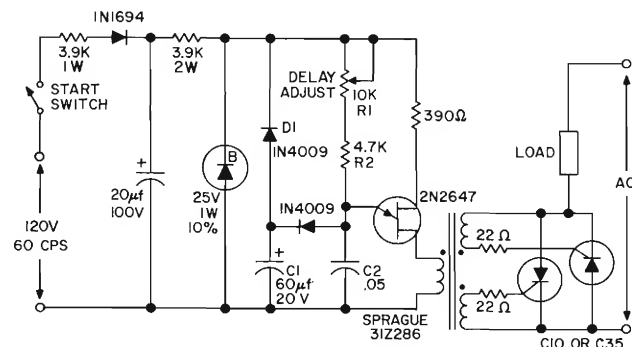
The 2N494C is biased continuously at the peak point by a 15 megohm resistor to reduce the triggering energy required. Adjustment of the time interval is obtained by means of the 10K potentiometer which sets the initial voltage on the timing capacitor. Extreme care must be taken in the choice of components and the layout to minimize leakage. A high quality mylar capacitor must be used for C_T. A glass sealed resistor must be used for R_T. Point A should be supported by the leads only or by a single teflon standoff insulator.

The circuit in Figure 13.32 gives time delays from 0.3 milliseconds to 5 hours without using a tantalum or electrolytic capacitor. The timing interval is initiated by applying power to the circuit. At the end of the timing interval, which is determined

FIVE HOUR TIME DELAY CIRCUIT
Figure 13.32

by the value of R1 C1, the 2N494C triggers the controlled rectifier. Load currents are limited only by the rating of the controlled rectifier which is from 1 ampere up to 25 amperes for the types specified in the circuit.

Charging resistor R1 must be small enough to supply the minimum trigger current (peak point current, I_P) of the 2N494C plus the leakage current of the capacitor when the emitter of the unijunction is biased at its peak point voltage. This would place a limit of 3 megohms for R1 and permit time delays to 6 seconds ($C1 = 2\ \mu f$) without using the additional 2N491 relaxation oscillator.

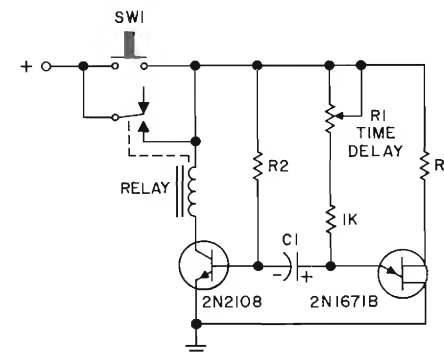
The circuit as shown effectively reduces the minimum I_P requirement more than 1000 times by pulsing the upper base of the 2N494C with a ¾ volt negative pulse. This negative pulse rate is not critical but it should have a period that is less than 0.02 (R1 C1). The negative pulse causes the peak point voltage to drop slightly and if the voltage level at C1 is greater than this, the unijunction will trigger with the necessary I_P supplied from C1. The low leakage requirement for C1 is easily obtained with a mylar capacitor. R2 can be adjusted or selected for best stabilization over the required temperature range. A pulse transformer can be used in place of the 27 ohm resistor if it is necessary to have the timing circuit isolated from the power switching (controlled rectifier) circuit which, for instance, might be connected to the ac line.

The input impedance of the 2N494C is greater than 1500 megohms before it is triggered. The maximum time delay that can be achieved by this circuit is mainly dependent upon the maximum values that can be obtained for R1 and C1 consistent

SOLID STATE AC TIME DELAY (ONE SECOND)
Figure 13.33

with the low leakage requirement. Without diode D1, R1 is limited to 15 megohms for an accuracy of 0.5% at 25°C and 5% at 55°C, but with D1, R1 can be increased to 10,000 megohms.

An all solid state time delay circuit with ac output can be achieved with a single UJT as shown in Figure 13.33. The timing sequence is started by closing the START SWITCH and applying voltage to the UJT circuit. The time delay is determined by the time constant (R1 + R2) (C1 + C2). When the voltage at the emitter of the UJT reaches the peak point voltage, capacitor C1 remains charged and the UJT oscillates at a high frequency determined by the time constant (R1 + R2) C2. The pulses from the UJT are then coupled through the pulse transformer to the SCR's, turning them on and applying voltage to the load. Since the UJT oscillates at a frequency much higher than the line frequency the switching of the SCR's is practically from full on to full off. The 2N2647 is needed to obtain the high output pulse required to fire two SCR's in parallel at a high repetition rate. When the start switch is opened diode D1 provides a path to discharge C1. Larger values of time delay can be obtained by increasing the value of C1. The timing circuit and the load circuit can be operated from a common ac supply or a seperate ac supply as desired.

DELAYED DROPOUT RELAY TIMER

The circuit of Figure 13.34 provides a simple means for accurately delaying the dropout of a relay after it is energized. In the quiescent state no power is applied to the circuit. When SW1 is momentarily closed the transistor will turn on and the relay will pull in. Voltage to the circuit is then maintained through the relay contact so that the relay will remain energized when SW1 is opened. After a time interval determined by the values of R1 and C1 the UJT will trigger, and the discharge of C1 will turn off the NPN transistor, allowing the relay to drop out. If SW1 is open the voltage to the circuit will be removed and the circuit will revert to its quiescent state.

DELAYED DROPOUT RELAY TIMER
Figure 13.34

An output voltage can be obtained from the relay contacts shown or extra sets of contacts on the relay can be used as desired.

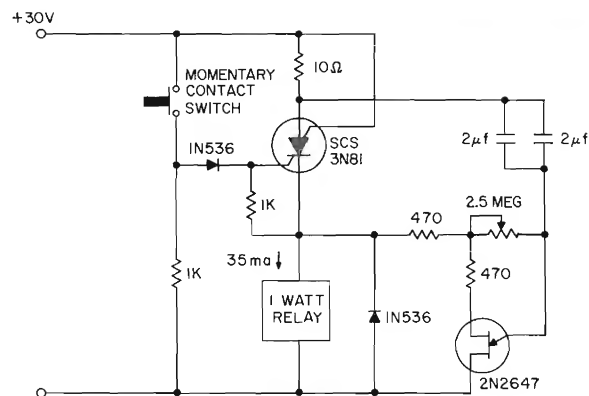
After deciding on the supply voltage and the relay to be used, R2 is then selected to provide sufficient base current to the NPN transistor with regard to the resistance of the relay coil and the minimum specified current gain of the transistor. The size of the capacitor is then selected to provide sufficient off time for the NPN transistor to allow the relay to drop out. Resistor R1 is then chosen for the maximum time delay

10 SECOND TIMER

Figure 13.35

required and the maximum peak point current of the UJT. Finally, resistor R3 is chosen for the required overall temperature compensation.

The circuit of Figure 13.35 provides for the relay to be energized for a preset period of time up to 10 seconds. Closing S1 triggers the silicon controlled switch (SCS), and places most of the supply voltage across the relay which also starts the unijunction timing interval. After a preset interval the unijunction will be triggered and discharge the 4 μf capacitance through the 10 ohm resistor. This discharge pulse makes the anode negative with respect to the anode gate (connected to +30 volts) and turns off the SCS which drops out the relay.

SENSING CIRCUITS

VOLTAGE SENSING CIRCUIT

The high sensitivity of the unijunction transistor and the extreme stability of V_P make it ideally suited for use in go no-go types of voltage sensing circuits such as shown in Figure 13.36. This circuit includes a simple floating power supply with zener diode regulation which operates from the 115 volt ac line. If the input signal is negative the unijunction will not trigger and there will be no output. If the input signal is slightly positive, the unijunction will trigger and pulses will occur at the output as long as the input signal remains positive. The output pulses are of sufficient magnitude to trigger a flip-flop, an SCR, or other pulse sensitive devices. Note that the transformer coupled supply and output of this circuit give complete freedom of choice in connecting the circuit to the signal source since there are no common grounds.

Most of the output pulse energy is supplied by capacitor C3. This capacitor is charged rapidly through R1 after each pulse and hence does not limit the response time of the circuit. Diode D2 provides a discharge path for C3, and diodes D1 and D2 clamp the input voltage to enable C3 to charge to its steady state voltage when very large voltages are present at the signal input. Capacitors C1 and C2 provide the initial trigger energy for the unijunction transistor and also serve as a filter for transients appearing at the signal input and across the supply. In some cases a small capacitor will also be required across the primary of the pulse transformer to prevent false triggering due to transients.

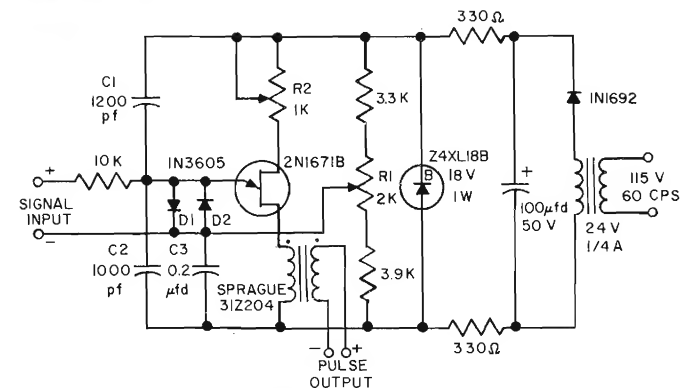
The circuit is initially adjusted by shorting the signal input and setting R1 so that the circuit is on the verge of triggering. If close temperature compensation is needed

VOLTAGE SENSING AND TRIGGER CIRCUIT

Figure 13.36

R2 is adjusted so that the triggering voltage does not change appreciably when the unijunction is heated or cooled. It is normally possible to adjust the temperature compensation so that the drift in trigger voltage is within ±2 millivolts from 0°C to 55°C. After the temperature compensation is completed it will normally be necessary to reset R1. The long term stability of this circuit is normally better than ±10 millivolts and the hysteresis is normally less than 1 millivolt. The change in triggering voltage with a change in the supply voltage (ΔV_1) will be less than 0.7 $\Delta V_1/V_1$. The voltage stability can be improved by adding two silicon diodes in series with R2.

NANOAMPERE SENSING CIRCUIT WITH 100 MEGOHM INPUT IMPEDANCE

The circuit in Figure 13.37 may be used as a sensitive current detector or as a voltage detector having high input impedance. R1 is set so that the voltage at point A is ½ to ¾ volts below the level that triggers the 2N494C. A small input current (I_{in}) of only 40 nanoamperes will charge C2 and raise the voltage at the emitter to the triggering level. When the 2N494C is triggered, both capacitors, C1 and C2 are discharged through the 27 ohm resistor, which generates a positive pulse with sufficient amplitude to trigger a silicon controlled rectifier (SCR), or other pulse sensitive circuitry. C2 is kept small for faster triggering response time and C1 is used to provide the pulse output energy. Rapid recovery is obtained after the 2N494C triggers since both capacitors are charged through R1. This configuration has the advantage that the leakage current of the silicon diode effectively subtracts from the leakage current of the unijunction and thus provides some temperature compensation.

The input current available (I_{in}) through the 100 megohm resistor will be much lower than the minimum trigger requirement for the 2N494C (peak point current (I_P) = 2.0 μa). Use of a sampling technique described for Figure 13.31, however, permits a reduction in the external triggering current (I_{in}) by as much as 1000 times below I_P. By pulsing the upper base of the 2N494C with a 0.75 volt amplitude negative pulse the peak point voltage V_P will drop slightly and if the voltage level at C2 is greater than this, the unijunction will trigger with the necessary I_P supplied from C2. By use of this technique, the 2N494C has been triggered with external input currents (I_{in}) as low as 1 nanoampere with a 2000 megohm resistor for R2.

The period of the 2N491 relaxation oscillation is not critical, but it should have a time constant of 0.02, or less, than that of the 2N494C.

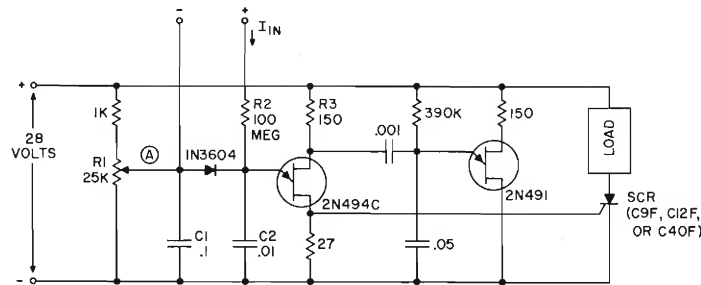
For this sensing circuit a floating power supply using a zener diode will permit

NANOAMPERE SENSING CIRCUIT WITH 100 MEGOHM INPUT IMPEDANCE

Figure 13.37

grounding one of the sensing input terminals if this is desirable. R1 should be adjusted so the circuit will not trigger at the maximum ambient temperature in the absence of the current or voltage sensing signal. R3 can be adjusted or selected for best stabilization of V_P over the required temperature range.

SCR TRIGGER CIRCUITS

SIMPLIFIED SCR TRIGGER CIRCUIT DESIGN PROCEDURES

SCR trigger circuits using the unijunction are simple and compact with low power consumption yet the 2N2647 can easily trigger a 235 amp rms SCR. An added advantage is that triggering is assured over a wide ambient temperature range even with UJT and SCR limit units (due to production variations). This assurance is available by using the tailored trigger circuits as outlined in Figures 13.38 and 13.39. These circuits essentially marry the particular UJT and SCR in a configuration that takes into account the dynamic triggering requirement of the SCR. Whereas most SCR specification sheets give consideration only to the static requirements. These design curves give the condition for the required minimum trigger energy, and it is then simple to double the value of C_T or increase V_1 for a guaranteed 2 to 1 above this minimum which is often desirable to decrease the SCR turn-on time and switching losses.

The value of R1 in the trigger circuits is kept low enough to prevent the dc voltage at the gate, due to interbase current, from exceeding the minimum gate triggering voltage for the SCR.

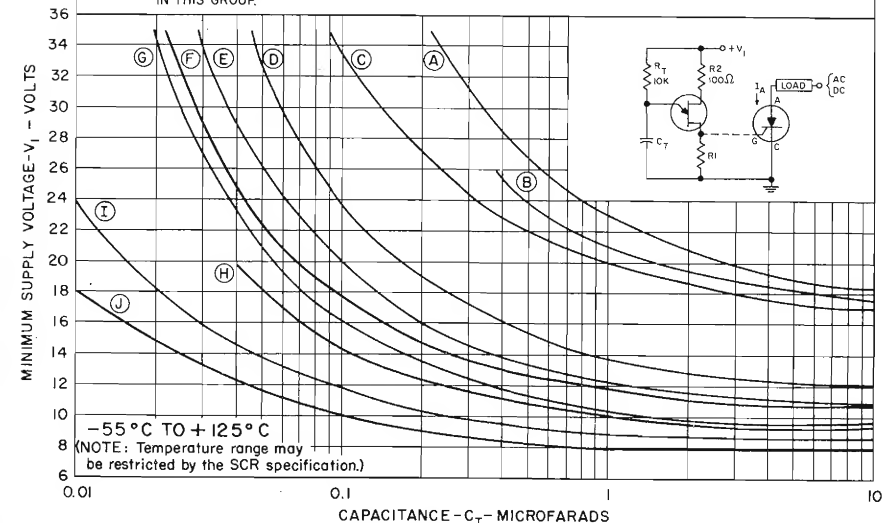
The design of a suitable SCR triggering circuit can be achieved rapidly and easily by using the design curves that are given. These curves give the minimum supply voltage required to guarantee triggering of the various types of SCR's over the specific temperature range as a function of the UJT emitter capacitor, C_T. The value of the resistor R_T is not important for the purposes of the design provided that it is within the limits required for the UJT to oscillate. If R2 is significantly greater than 100 ohms the minimum supply voltage which is assumed (V_1') should be calculated from the minimum supply voltage (V_1) given in the design curves using the equation (131).

$$V_1' = \frac{(2200 + R2)\, V_1}{2300} \qquad (131)$$

As an example of the practical design of an SCR triggering circuit, consider the following:

Problem: A circuit is required to trigger a high current type 2N1913 SCR and the trigger circuit supply is 22 volts. We choose the 2N2647 UJT because of its guar-

UJT TYPE	SCR TYPE	CURVE	R1	$V_{1(MAX)}$
2N489A & B THROUGH 2N494A, B, AND C (ALSO USAF TYPES)	C60(2N2023-30) C55 AND C56 C52(2N1792-98) C50(2N1909-16) C46 C45 C37 C36(2N1842-50)	A	27Ω ± 10%	35V
		B	47Ω ± 10%	26V
		C	PULSE TRANS. PE2231	35V
2N2417A & B THROUGH 2N2422A, B, AND C	C40 C38* C35(2N681-92) C30 AND C32** C20 AND C22** C15	D	27Ω ± 10%	35V
		E	47Ω ± 10%	20V
		G	PULSE TRANS. SPRAGUE 31Z204	35V
2N1671A & B 2N2646	C12 C11(2N1770-78, 2N2619) C10(2N1770A-77A) C9 C8(2N1929-35) 2N1595-99	E	27Ω ± 10%	32V
		G	47Ω ± 10%	18V
		I	PULSE TRANS. SPRAGUE 31Z204	35V
2N2647***	C7(2N2344-48) C6 C5	F	15Ω ± 10%	35V
		H	27Ω ± 10%	20V
		J	SPRAGUE 31Z204	35V

NOTES: * LIMITED TO 27 VOLTS MAX ON "D" CURVE AND 15 VOLTS ON "E" CURVE.
** TRIGGER REQUIREMENTS LESS THAN OTHERS IN THIS GROUP.
*** MINIMUM TRIGGER PULSE IS TWICE THE AMPLITUDE OF OTHER UJT'S, THIS ASSURES 2:1 OVER MINIMUM SCR TRIGGER REQUIREMENTS.

SCR TRIGGER CIRCUIT DESIGN CURVES

(Assures minimum trigger requirement for I_A rise <10A/μsec.)

Figure 13.38

anteed high trigger pulse, V_{OB1}. Assume that the value of capacitance, chosen on the basis of operating frequency, is 0.2 μf and that the value of the base-two resistor, calculated for temperature compensation, is 620 ohms.

Solution: From Figure 13.39 it is seen that curve B meets the above requirements with a 27 ohm resistor for R1. On curve B it is seen that the minimum voltage for $C_T = 0.2$ μf is 11.7 volts. Correcting this value to take into account the value of R2, equation (131) gives $V_1' = (1.22)(11.7) = 14.3$ volts. Triggering is therefore assured for a supply voltage range of 14.3 to 35 volts. If the supply voltage is

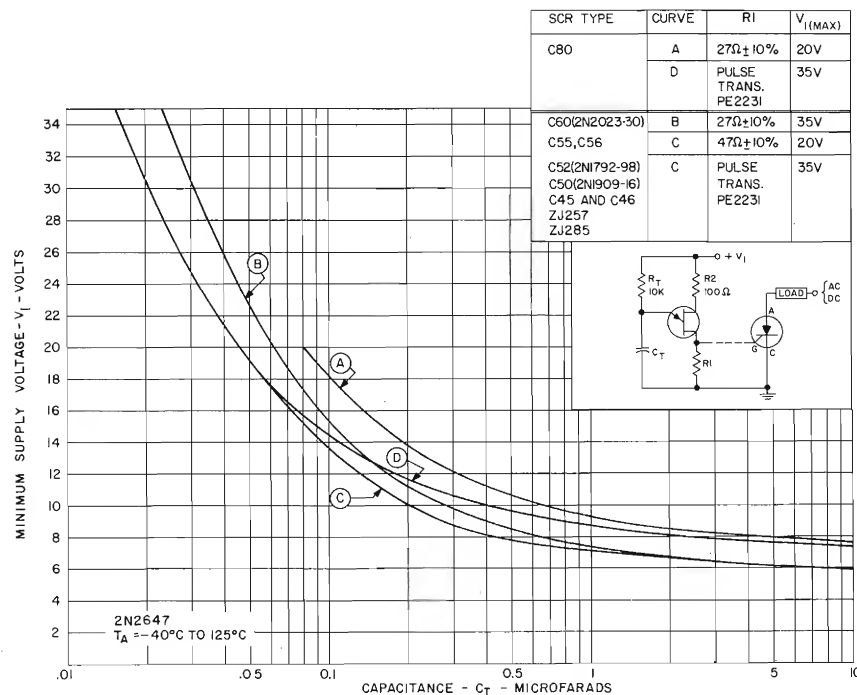
SCR TYPE	CURVE	R1	$V_{1(MAX)}$
C80	A	27Ω ± 10%	20V
	D	PULSE TRANS. PE2231	35V
C60(2N2023-30)	B	27Ω ± 10%	35V
C55,C56	C	47Ω ± 10%	20V
C52(2N1792-98) C50(2N1909-16) C45 AND C46 ZJ257 ZJ285	C	PULSE TRANS. PE2231	35V

HIGH CURRENT SCR TRIGGER CIRCUIT DESIGN CURVES USING 2N2647

Figure 13.39

greater than 35 volts the SCR may be triggered by the dc voltage across R1 at an elevated SCR junction temperature. Thus, a suitable design using the 2N2647 in the triggering circuit would be $C_T = 0.2\ \mu f$, R2 = 620 ohms, R1 = 27 ohms, and $V_1 = 22$ volts, +60% or −35%.

TRIGGERING PARALLEL-CONNECTED SCR'S

If two or more SCR's in parallel are to be triggered by a single UJT the design of the trigger circuit must take into consideration the possibility that an SCR with a low gate resistance may be paralleled with an SCR having a high gate resistance, thus loading down the output pulse sufficiently to prevent the second SCR from being triggered. To reduce this possibility it is recommended that the trigger pulse be coupled by means of a separate capacitor to each SCR gate. These capacitors act to equalize the charge coupled to each gate during the trigger pulse and thus tend to reduce the effects of unequal loading. The optimum value of capacitor for this purpose has been found to be 0.1 μf. In addition to this capacitor, a resistor having a value of 220 ohms to 1K should be connected between gate and cathode of each SCR. Using this approach of equalizing capacitors, the design curves of Figures 13.38 and 13.39 can be used for parallel triggering of SCR's, provided that the minimum supply voltage is multiplied by a factor of 1.5 if two SCR's are to be triggered in parallel and by a factor of 1.8 if three SCR's are to be triggered in parallel. Since the gates are not direct coupled, the maximum supply voltage allowed is limited only by the 35 volt rating of the UJT.

Alternatively, a larger value of base-one resistance, R1, can be used to reduce the otherwise required increase in value of supply voltage for parallel triggering. For example, if R1 = 100 ohms, and using equalizing capacitors, the curves for R1 = 27 ohms apply for triggering two SCR's in parallel with no increase in supply voltage. For triggering three SCR's in parallel under this condition the supply voltages given by these curves should be increased by a factor of 1.25.

SIMPLIFIED SCR TRIGGER CIRCUITS FOR AC LINE OPERATION

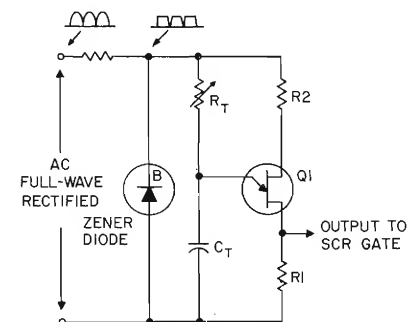
A trigger circuit that is synchronized from the ac line is shown in Figure 13.40.

LINE SYNCHRONIZED TRIGGER CIRCUIT

Figure 13.40

A full wave rectified signal obtained from a rectifier bridge or a similar source is used to supply both power and a synchronizing signal to the trigger circuit. The zener diode is used to clip and regulate the peaks of the ac as indicated in Figure 13.40. At the end of each half-cycle the voltage at base-two of the UJT will drop to zero, and any charge on the capacitor will forward bias the emitter diode of UJT into conduction. The capacitor is thus discharged at the beginning of each half cycle and the trigger circuit synchronized with the line. A pulse is produced at the output at the end of each half cycle which can cause the SCR to trigger and produce a small current in the load.

A simplified type of trigger circuit results if base-two and the emitter timing circuit of the UJT are supplied directly from the line by way of dropping resistor R_D which keeps the peak voltage on the UJT within its specifications. (See Figure 13.41.) The voltage across capacitor C will increase at a rate determined by the time constant of the circuit. When it reaches the peak point voltage the UJT will trigger and turn on the SCR.

SIMPLIFIED UNIJUNCTION TRANSISTOR TRIGGER CIRCUIT

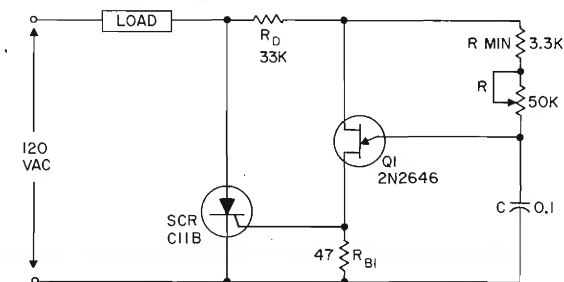
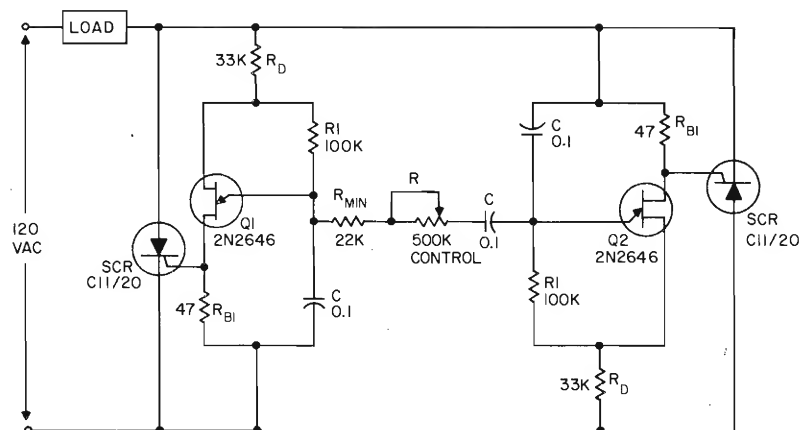
Figure 13.41

SIMPLIFIED FULL-WAVE UJT TRIGGER CIRCUIT

Figure 13.42

The half-wave circuit of Figure 13.41 can be extended to full-wave operation. In Figure 13.42 two of the basic circuits of Figure 13.41 have been placed back-to-back. The emitters of the two UJT's have been cross-coupled with a network that exerts full cycle phase control over both SCR's.

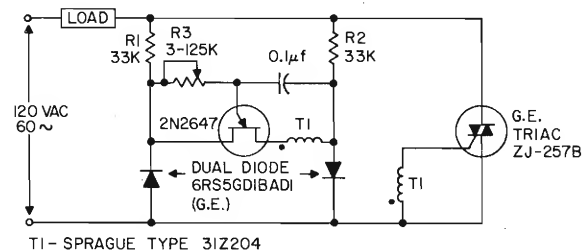
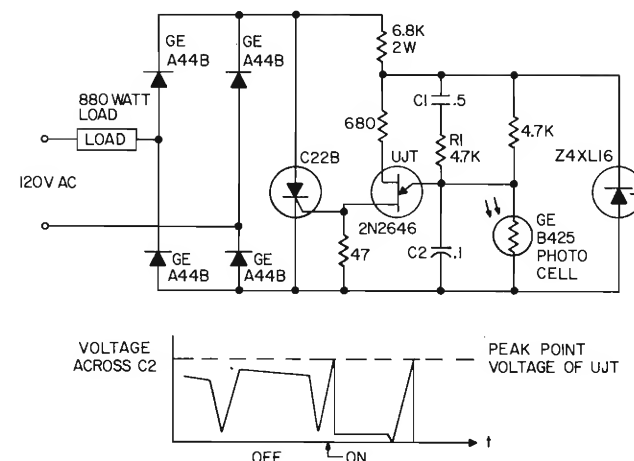
The unijunction phase-control circuit in Figure 13.43 has a wide range of stable control without hysteresis or dependence upon supply voltage. Automatic feedback control systems can be designed with this UJT circuit since the UJT is essentially half of a balanced bridge with built-in un-balance detection of high sensitivity and stability. The dual diode is selenium and has a low peak reverse voltage requirement in this circuit.

UJT/TRIAC PHASE CONTROL

Figure 13.43

SENSITIVE AC POWER SWITCH

The circuit Figure 13.44 switches load in response to a gradually changing signal such as light on a cadmium sulfide photocell, temperature of a thermistor and so on. Switching is a positive snap action from full "off" to full "on" and vice versa. Differential in input between switching conditions may be adjusted over a wide range by changing values of C1 and R1.

SENSITIVE AC POWER SWITCH

Figure 13.44

The conventional unijunction transistor circuit has been modified so the voltage waveshape across capacitor C2 has a higher value at the beginning of each half-cycle than at the end. This wave is the result of C1 and R1 producing a higher charging current to C2 at the beginning of the cycle. As the photocell resistance (in this case) increases, the voltage on C2 rises until it reaches the peak-point voltage of the UJT. Since this condition occurs first at the leading edge of the cycle, the UJT will only trigger at that point, turning the SCR on early in each half cycle. Triggering the SCR removes voltage from the UJT circuit, and capacitor C1 discharges. At the beginning of the next half cycle, the discharged condition of C1 produces a higher charging current for C2, assuring a snap action full "on" condition. Photocell resistance must then be reduced to a value lower than before in order to stop triggering the UJT and SCR, hence the differential between "on" and "off" conditions.

The photocell can be replaced with a grounded emitter NPN transistor to make the circuit sensitive to dc input signals. This on/off ac switch can be used for photoelectric controllers, temperature regulators, overheat protection, latch-on functions, ac motors, driving compressors, conveyors, and fans.

SENSITIVE DC POWER SWITCH

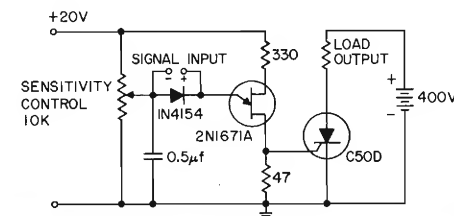
The circuit in Figure 13.45 features a latching action. That is, once triggered, it stays on. In this circuit

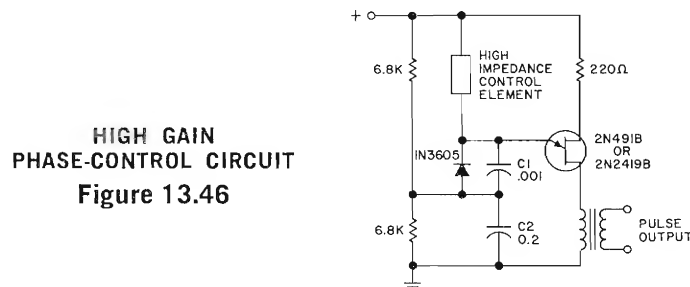
Power input $= 0.1$ volt at 25 μamp $= 2.5$ μwatts

Power output $= 400$ volts at up to 110 amps dc $= 44$k watts

$$\text{Power gain} = \frac{\text{Output}}{\text{Input}} = \frac{44 \times 10^3}{2.5 \times 10^{-6}} = 17.5 \times 10^9 \cong 92\text{db}$$

SENSITIVE DC POWER SWITCH

Figure 13.45

HIGH GAIN PHASE-CONTROL CIRCUIT

The minimum size of the capacitor C2 in a conventional UJT/SCR phase-control circuit is dictated by the minimum acceptable pulse amplitude at the output. For reliable firing of high current SCR's a capacitor in the range of 0.20 μfd is necessary. Once the minimum size of the capacitor and the required range of phase control are determined the required current from the control element will be fixed. If the available current from the control element is insufficient, one or more stages of amplification must be added between the control element and the phase-control circuit.

HIGH GAIN PHASE-CONTROL CIRCUIT
Figure 13.46

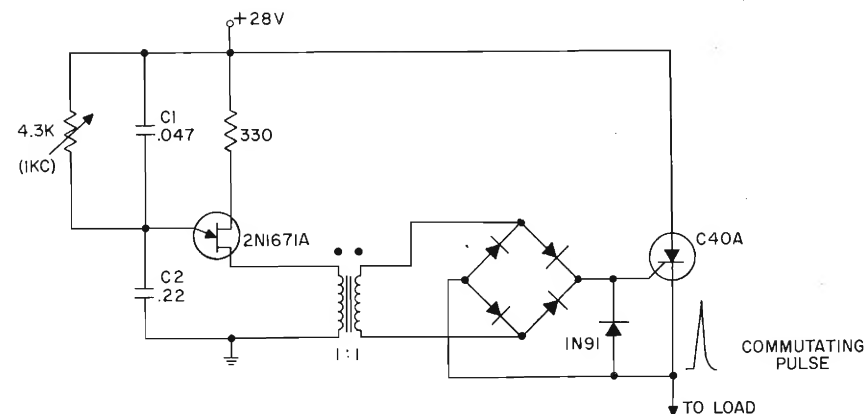
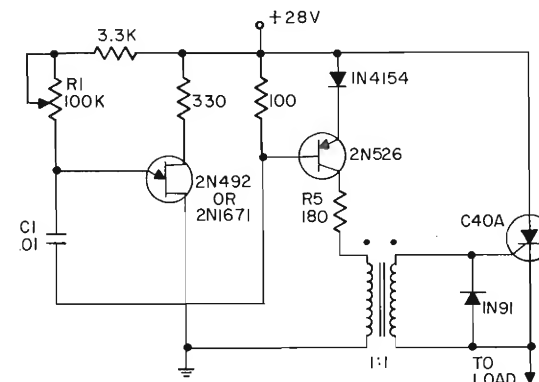
The simple modification of the phase-control circuit shown in Figure 13.46 permits an increase in the effective gain by a factor of up to 10,000 times and in many applications will duplicate the performance of two or three stages of transistor amplification. In this circuit the larger capacitor, C2, is rapidly charged through the 6.8K resistors at the beginning of the timing interval. The smaller capacitor, C1, is charged through the control element and since this capacitor is in series with C2 it can be charged simultaneously with C2. The effective gain of the circuit is very large since a smaller voltage change is required across a smaller capacitor than with the conventional phase control circuit. Thus the current required from the control element is much less than if C2 were charged directly. At the same time the full pulse energy from C2 is available at the output.

In designing this circuit, C2 is chosen large enough to provide the required output pulse amplitude. Capacitor C1 is chosen small enough to provide sufficient gain for the circuit and large enough to ensure regeneration at the peak point. Usually a value of 500 pf will be adequate to meet the latter requirement for the 2N489-2N494, 2N2417-2N2422 or 2N1671, and 100 pf will be adequate for the 2N2646 or 2N2647.

TRIGGERING CIRCUITS FOR DC CHOPPERS AND INVERTERS

The impulse commutation often used in dc choppers and inverters can cause premature triggering of the unijunction. The positive commutating pulse applied to the cathode of the SCR, results in a negative pulse gate to cathode. If these negative pulses reach base-one of the unijunction it may be triggered prematurely. When transformer coupling is used, transients can be greatly attenuated by a diode bridge as shown in Figure 13.47. A negative gate to cathode pulse at the SCR may be further attenuated by the low impedance 1N91.

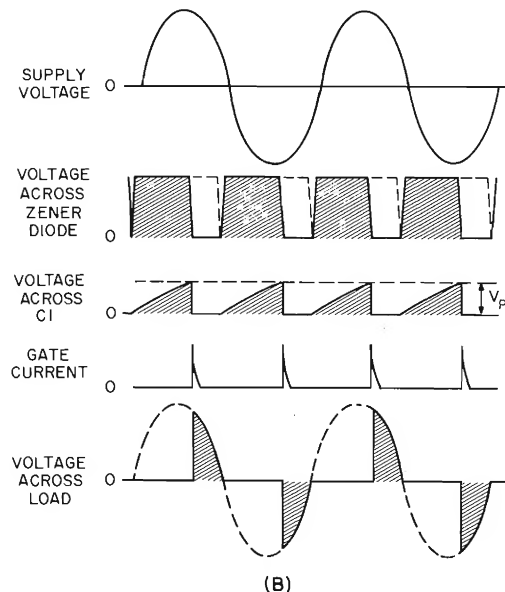
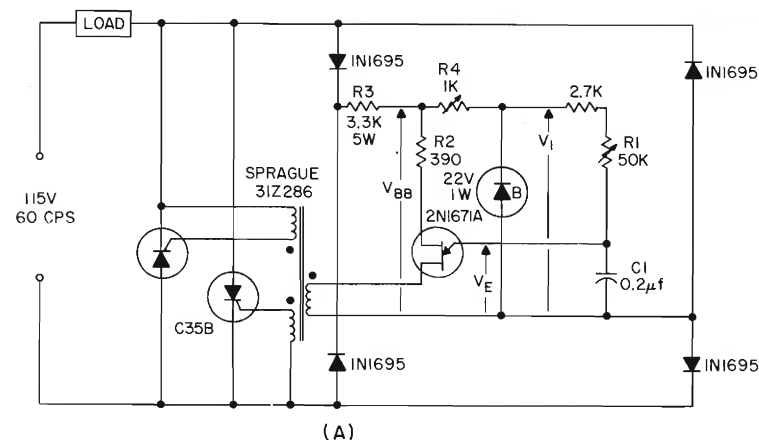
Supply voltage transients can be decoupled from the unijunction emitter by choosing the impedance of C1 and C2 so the transient has negligible effect on V_P. The sum of C1 and C2 constitute the total unijunction timing capacitance.

The triggering circuit of Figure 13.48 uses the UJT to drive the 2N526 from cut-off to saturation. Since we are not using the energy in C1 to trigger the SCR, the smaller .01 μf capacitor size can be used and thus achieve UJT operation to 20 kc. The 1N4154 keeps the emitter-base junction of the 2N526 reverse biased except for

TRIGGER CIRCUIT FOR ELIMINATION OF TRANSIENT INTERFERENCE
Figure 13.47

20 KC TRIGGER GENERATOR
Figure 13.48

the discharge interval of C1. R5 limits the voltage amplitude of the trigger pulse to the SCR. The 2N526 also isolates the SCR turn-off pulse from the UJT timing circuit.

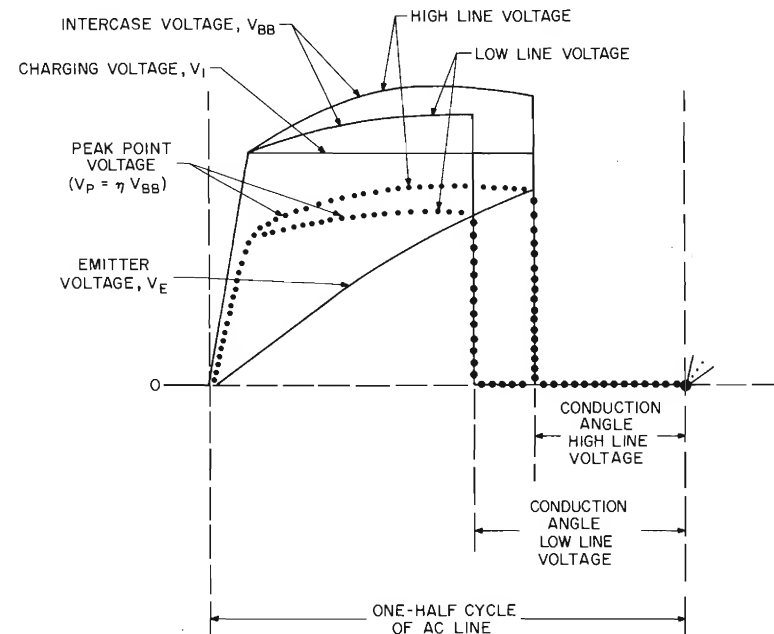
The square wave inverter drive circuit shown in Figure 10.12 (Chapter 10) has been used successfully as the control and trigger source for parallel inverters using General Electric type C40 SCR's.

REGULATED AC POWER SUPPLY

The unijunction triggering circuit in Figure 13.49(A) uses the voltage developed across the SCR's during blocking for the interbase supply as well as synchronization for the unijunction transistor. The firing circuit is connected to the output of a single phase bridge formed by the 1N1695's. Through the action of the bridge, the zener diode and the resistor R3, a clipped and rectified voltage with a waveform as shown in Figure 13.49(B) is applied to the UJT and its emitter circuit.

REGULATED AC POWER SUPPLY AND WAVESHAPES
Figure 13.49

The regulating ability of the supply in Figure 13.49(A) results from having R4 in the circuit. The charging voltage for the capacitor is equal to the zener voltage and is essentially constant over the half cycle prior to the instant when the SCR is triggered. This is shown in the waveforms of Figure 13.50. The interbase voltage, V_{BB}, of the UJT is not constant during this interval, but is equal to the breakdown voltage of the zener diode plus a small fraction of the line voltage determined by the voltage dividing ratio of R3 and R4. Thus at any given phase angle the interbase

voltage will increase if the line voltage increases as shown in Figure 13.50. The peak point voltage of the unijunction transistor is equal to the interbase voltage times the standoff ratio and is given in Figure 13.50 to correspond to the two interbase voltage curves.

The emitter voltage follows the normal exponential charging characteristic since the charging voltage, V_1, is constant. The UJT and SCR's trigger when the emitter voltage equals the peak point voltage. It is readily apparent from Figure 13.50 that, as the line voltage increases, the delay before the UJT and SCR's are triggered increases and hence the conduction angle of the SCR's decreases. The decreased conduction angle reduces the power to the load, thus offsetting the increase of power to the load otherwise due to the increase in line voltage. By proper choice of the voltage divider ratio of R3 and R4 it is possible to obtain perfect compensation of the circuit for small changes in line voltage.

VOLTAGE WAVEFORMS OF SCR/UJT REGULATED AC SUPPLY WITH HIGH AND LOW LINE VOLTAGE
Figure 13.50

The circuit shown was adjusted to give optimum regulation at 25 volts rms output and 115 volts input, and the component values listed were found to be suitable. For a change in line voltage from 115 volts to 100 volts the change in output voltage was less than 0.1 volt with any output voltage setting from 10 volts to 30 volts.

If regulation is desired over a wide range of output voltage, a ganged pot can be used with R1, and the value of R4 can be changed with the position of the potentiometer. The value of R2 is chosen to achieve the desired temperature compensation in the ordinary manner. There is some interaction between the adjustment of R4 for voltage compensation and the adjustment of R2 for temperature compensation, so several successive adjustments may be required.

TRANSISTOR CONTROL OF UNIJUNCTION

SHUNT TRANSISTOR CONTROL OF UJT

In circuits using a shunt transistor to control the UJT similar to the arrangement in Figure 13.51, it is seen that Q1 can shunt some of the charging current supplied to C1 by resistor R1 in an amount dependent of the base drive to Q1. The more Q1 is turned on, the greater the delay before the UJT is triggered. With R1 set for about 4.7K ohms, base current I_B to Q1 will then control the diversion of charging current from C1 and retard or advance the triggering of the UJT. Q1 can prevent the triggering of the UJT if

$$I_B \geq \frac{V_1 (1 - \eta)}{h_{FE} R1} \qquad (13m)$$

where

I_B is in amperes
$V_1 = 20$ volts, and
h_{FE} = current gain of Q1

SIGNAL DROPOUT DETECTOR
Figure 13.51

The circuit of Figure 13.51 can be used to provide an indication of a momentary dropout of an input signal. The signal monitored could be a dc voltage, an ac voltage, or a pulse voltage. The time between the disappearance of the signal and the indication of a fault can be adjusted as desired.

Capacitor C1 will be charged through R1 continuously. In the presence of an input signal the NPN transistor will discharge C1 in a periodic manner so that the voltage at the emitter of the UJT will not reach the peak point voltage and neither the UJT nor the SCS will be triggered. If the input signal disappears or the time between pulses exceeds the preset value, the UJT and the SCS will be triggered and provide a dc output signal. The output signal will remain until the SCS is turned off by momentarily opening the reset switch. The 100K resistor in the anode gate of the SCS is used to prevent the rate effect from interfering with the reset action.

SERIES TRANSISTOR CONTROL OF UNIJUNCTION

A transistor in series with C1 instead of in shunt with it can be used to regulate the charging rate of the capacitor and thereby retard or advance the triggering of

the UJT. Such a circuit is shown in Figure 13.52. An additional NPN transistor, Q3, is required if it is desired to keep one side of the input signal at the potential of the lower line. Series control often offers an advantage in noise immunity in a system.

SERIES TRANSISTOR CONTROL OF UJT
Figure 13.52

HYBRID TIMING CIRCUITS

The unijunction transistor can be used in conjunction with conventional PNP or NPN transistors to obtain versatile timing circuits such as symmetrical and nonsymmetrical multivibrators, one-shot multivibrators, variable frequency oscillators, and time delay circuits. The advantages of these circuits include: (1) the output at the collector of each transistor is very nearly an ideal rectangular waveform, (2) the circuits will tolerate large variations in h_{FE} or I_{CO} of the transistors as compared to conventional circuits, (3) the circuits are not prone to "lock-up" or non-oscillation, (4) the timing stability is excellent, and (5) a single small timing capacitor C_T can be used, avoiding the use of electrolytic capacitors in many applications.

The hybrid timing circuits can use either germanium or silicon transistors as desired. The basic circuits for PNP or NPN transistors are shown in Figures 13.53(A) and 13.53(B). In both of these circuits, the junction transistors form a conventional flip-flop with the unijunction transistor serving the timing and triggering functions. Each time the unijunction transistor conducts, the discharge current from the capacitor C_T develops a pulse across R_A which triggers the flip-flop from one state to the other.

The basic circuits as shown in Figures 13.53(A) and 13.53(B) will operate at frequencies from about 1 cycle to 500 cycles, and at temperatures above 75°C. Frequencies from 1 cycle per minute to 100 kc can be obtained by proper choice of C_T and R_A and suitable flip-flop design. The operating temperature range may be extended to 150°C by the use of silicon transistors.

The basic hybrid timing circuits in Figures 13.53(A) and 13.53(B) can be adapted to perform desired functions by connecting resistors or potentiometers, as indicated below, between the circuit points C1, C2, E, and G.

BASIC HYBRID TIMING CIRCUITS USING PNP AND NPN TRANSISTORS

Figure 13.53

SYMMETRICAL MULTIVIBRATOR (SQUARE WAVE GENERATOR)

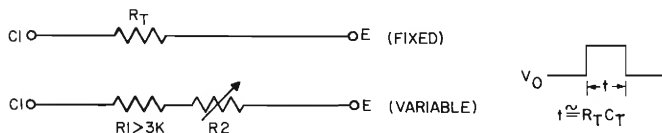
E — R_T — G (FIXED)

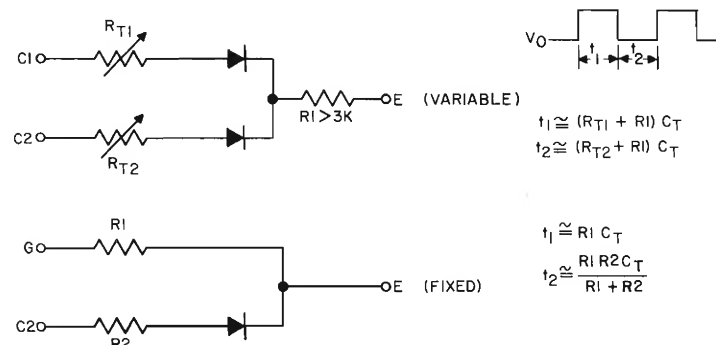
E — R_1>3K — R_2 — G (VARIABLE) V_O

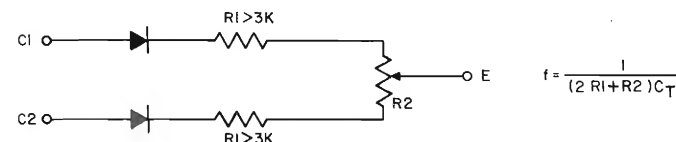
Connecting the resistor between points E and G in the basic circuits gives a square wave generator which has perfect symmetry. By the use of a 2 megohm potentiometer the frequency may be varied continuously from 1 cps to 500 cps. The frequency is $f = 1/2\, R_T C_T$.

ONE-SHOT MULTIVIBRATOR

C1 — R_T — E (FIXED)

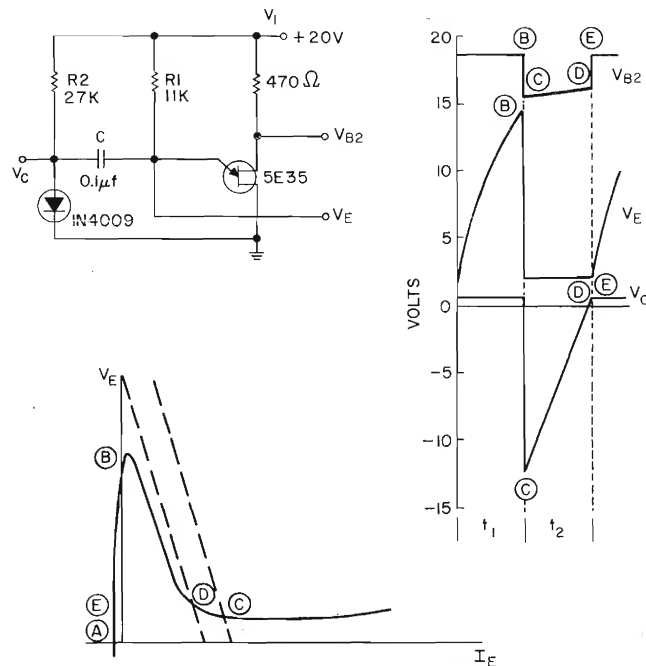
C1 — R1>3K — R2 — E (VARIABLE) V_O $t \cong R_T C_T$

In the quiescent state, Q2 is *on* in Figure 13.53(A), therefore a positive pulse at the base of Q2 will trigger the circuit. For Figure 13.53(B), Q1 is *on* in the quiescent state, therefore a negative pulse at the base of Q1 will trigger the one-shot. At the end of the timing interval, the unijunction will be triggered and cause the circuit to revert to its quiescent state. This circuit has the advantage of a fast recovery time so it may be operated at a high duty ratio without any loss of accuracy.

NON-SYMMETRICAL MULTIVIBRATOR

The timing capacitor C_T will be charged through the resistor R_{T1} or R_{T2} which is connected to the positive collector. The diodes will isolate the other resistor from the timing capacitor. The two parts of the period (t_1, t_2) can thus be set independently by R_{T1} and R_{T2} and may differ by as much as 1000 to 1.

NON-SYMMETRICAL MULTIVIBRATORS (Constant Frequency)

This configuration gives a multivibrator which has a constant frequency but a variable duty cycle.

MULTIVIBRATOR

Figure 13.54 shows a unijunction transistor multivibrator circuit which operates at 400 cycles. The length of time during which the unijunction transistor is *off* (no emitter current flowing) is determined primarily by R1. The length of time during which the unijunction transistor is *on* is determined primarily by R2. Assume power is applied to the circut at time t = 0. Current will flow through R2 and the diode to ground. The capacitor will be charged through R1 with the right hand side rising towards +20V. In Figure 13.54 the emitter voltage rises from point A as the capacitor voltage increases. When the emitter voltage reaches the peak point voltage (point B), the UJT is triggered *on*. The emitter voltage falls to the value determined by the intersection of the load line formed by R1R2/R1+R2 and the emitter characteristic, point C. At the same time the voltage across the diode drops by an equal amount and the diode becomes reverse biased. The capacitor is then discharged through R2 with the left hand side rising towards +20V. During this interval the current through the emitter of the UJT is the sum of the current through R1 and the discharging current from the capacitor.

The UJT remains stable in the negative resistance region as long as the emitter sees the high resistance of R2 in series with the capacitor. After the capacitor is discharged to a point where the diode again becomes forward biased, the current through R2 will be diverted into the diode and the emitter current will fall to a value determined by the load line formed by R1 (point D). Now unstable, because of the low impedance of the forward biased diode, the UJT will turn off and its operating

UNIJUNCTION MULTIVIBRATOR
Figure 13.54

point will move to E. This cycle will repeat with the operating point of the UJT moving around the characteristic in an E B C D sequence, as shown in Figure 13.54.

During the *on* time of the UJT the capacitor is discharged through R2 and the emitter current decreases. This in turn increases the interbase resistance and produces a slight increase in the interbase voltage as indicated between points C and D on the waveform.

The frequency of the multivibrator is inversely proportional to the capacitor.

$$f = \frac{A}{C}$$

where A = 40 for R1 = 11K and R2 = 27K. The UJT *off* time is determined primarily by R1 and the *on* time by R2.

$$t_1 = R1\,C\,l_n \left[\frac{V_1 - V_{E\,(MIN)}}{V_1 - V_P}\right] \quad (13n)$$

$$t_2 = R2\,C\,l_n \left[\frac{V_1 + V_P - V_{E\,(MIN)}}{V_1}\right] \quad (13o)$$

where $V_{E\,(MIN)}$ is measured at

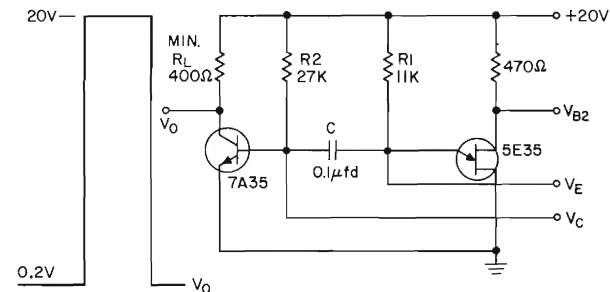
$$I_E = \frac{V_1\,(R1 + R2)}{R1\;R2} \quad (13p)$$

which is point C on the waveform in Figure 13.54.

In Figure 13.55, the diode is replaced by the emitter-base junction of the NPN transistor. This turns the transistor *on* and *off* when this diode is forward and reverse biased, respectively. The collector load has a negligible effect on the timing of the

circuit. It should be noted, however, that the load must be large enough to permit the minimum base current of

$$\frac{V_1}{R2} + \frac{V_1 - V_P}{R1} \quad (13q)$$

to drive the transistor into saturation. It is not necessary to supply the transistor from the same power supply as the multivibrator. Any NPN transistor can be used in this circuit if the emitter-base breakdown voltage is adequate ($BV_{EB} \geq 15V$). The 7A35, a low-cost silicon mesa with an emitter-base voltage rating of 15 volts and a minimum h_{FE} of 50 at 50 ma, is recommended for use in this application.

TRANSISTOR-UJT MULTIVIBRATOR
Figure 13.55

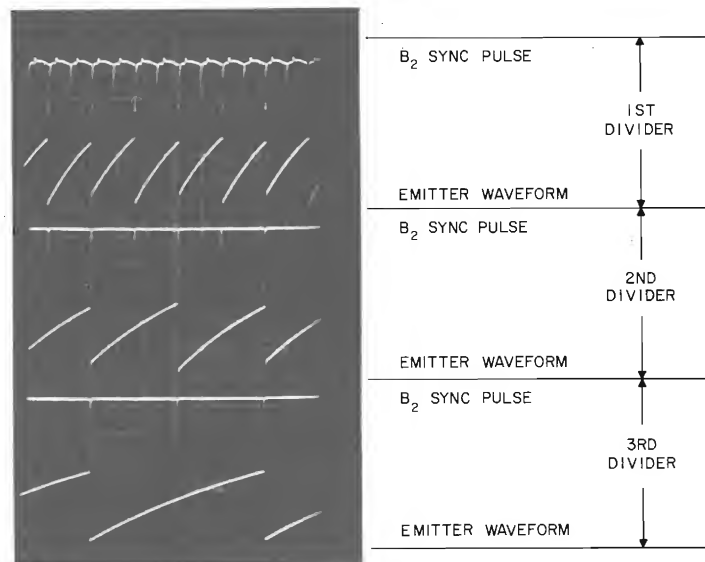
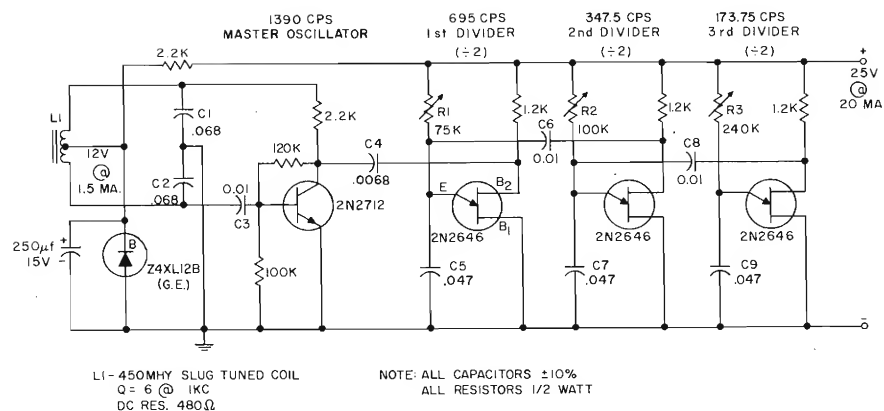
The specification sheet for the unijunction types 5E35 and 5E36 give design curves and performance capability for the UJT multivibrator.

FREQUENCY DIVIDER

The simple unijunction relaxation oscillator circuit can easily be adapted for frequency division by cascading several of these basic circuits and synchronizing from a master oscillator. From each divider stage there is available a sawtooth waveform as well as pulse outputs of either polarity.

The divider circuit in Figure 13.57 consists of a class C Hartley oscillator followed by three basic unijunction relaxation oscillators each having its own "free-running" frequency when unsynchronized. Each unijunction stage functions as a relaxation oscillator synchronized to the preceding stage by pulses coupled through C4, C6, and C8. Frequency division by two (÷ 2) will result with maximum divider stability when the oscillator free-runs at about three times the period of its synchronizing pulse. About 5% increase in period will result in the first and second dividers because of the parallel value of the emitter timing capacitor plus the sync pulse coupling capacitor.

The ideal timing resistor (R1, R2, R3) for each stage can always be determined by checking the maximum and minimum resistance values before the stage drops out of synchronization; the divider stage that follows should be connected since it does load the previous stage.

The UJT relaxation oscillator can be synchronized by applying positive pulses at the emitter or negative pulses at base-two. At the emitter the pulse amplitude requirement is approximately ⅔ of that required at base-two when using the 2N2646. Since base-two synchronization offers less loading on the pulse source and since a negative pulse of suitable amplitude is readily available, this method of synchronizing is used

UJT FREQUENCY DIVIDER WAVEFORMS
Figure 13.56

UNIJUNCTION FREQUENCY DIVIDER
Figure 13.57

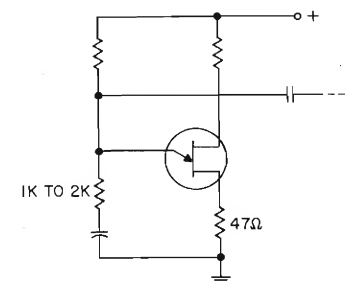
in Figure 13.57. Using a high amplitude sync pulse permits wide variations in component tolerance. Total component variation for each divider including the unijunction, can approach ±25% when dividing by two. If the pulse amplitude is too high it will lock the divider stage on every sync pulse instead of counting down by two. For division by two with a 25 volt supply, synchronizing pulses from about 6 to 10 volts may be used, with about 8 volts ideal. When the countdown is increased, however,

allowable component variation decreases. In addition, synchronizing pulse amplitude becomes more critical. To illustrate, dividing by six (÷ 6) in a single stage, synchronized by a 1½ to 3 volt pulse, permitted a total component variation of only ±7%.

Two capacitors, C1 and C2, are used across L1 rather than only a single capacitor for two reasons: a balanced tank to ground results in improved wave shape across the resonant tank, and, the prime reason, rapid turn-on of current conduction by the 2N2712 results in a sharp synchronizing pulse with more than twice the amplitude obtained when only a single capacitor is used. If L1 is tapped at the optimum point, C3 can then be used for dc blocking only. Any stable oscillator that will produce a negative 6 to 8 volt pulse with sharp wavefront and a few microseconds wide, will drive this unijunction divider system.

Capacitor C4 is selected to provide a 6 to 8 volt pulse at base-two of the first divider. This pulse amplitude allows good locking action between the oscillator and the first divider with minimum oscillator loading. In addition, feedback of the pulse generated at base-two by the unijunction when the 1st divider triggers is minimized. To completely alleviate the feedback pulse, a blocking diode can be used in series with, or in place of, C4.

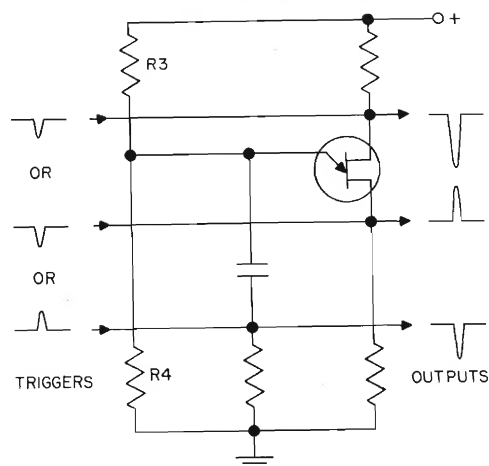
By adding a 1K to 2K resistor in series with each emitter timing capacitor, as shown in Figure 13.58, an additional ±5% circuit tolerance can be expected. An advantage in adding the base-one resistors is the availability of a positive going pulse at base-one. Duty cycle, up to about 5%, as well as the pulse amplitude are dependent on the resistor values used.

When subjected to temperatures of 0°C to 70°C the frequency dividers remain locked.

ADDING 1K TO 2K RESISTOR IMPROVES CIRCUIT TOLERANCE
Figure 13.58

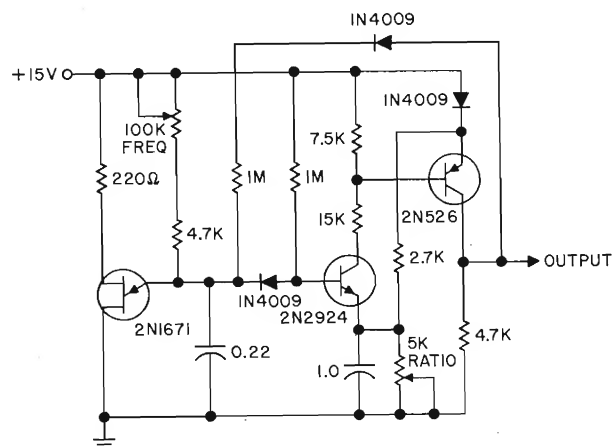
MISCELLANEOUS CIRCUITS

REGENERATIVE PULSE AMPLIFIER

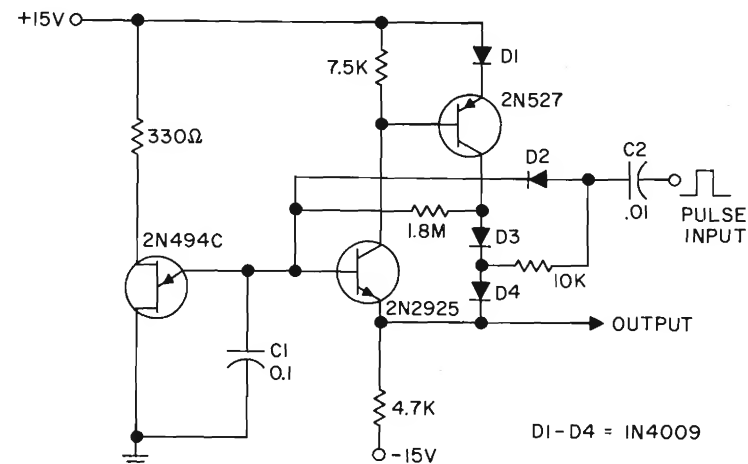
The basic UJT relaxation oscillator may be adapted to form a regenerative pulse amplifier by adding a resistor between emitter and ground. Resistors R3 and R4 should have a ratio such that the emitter voltage does not exceed the peak point voltage for the quiescent state, similar to the level sensing circuits. The values of the resistors should be large enough so that the UJT is not stable in the *on* state as discussed under relaxation oscillators. Figure 13.59 shows a general pulse amplifier with three possible inputs and three outputs. Two trigger input pulses could be used for coincident pulse detection. Either pulse by itself should not have sufficient amplitude to trigger.

REGENERATIVE PULSE AMPLIFIER CIRCUIT
Figure 13.59

PULSE GENERATOR (VARIABLE FREQUENCY AND DUTY CYCLE)

The frequency and duty ratio can be varied independently with the rectangular wave generator shown in Figure 13.60. The UJT is used in a conventional sawtooth generator and the two transistors serve to provide a positive going output when the voltage at the emitter of the UJT exceeds the voltage at the emitter of the NPN transistor as determined by the setting of the RATIO potentiometer. The loading of the sawtooth by the transistors is compensated by feeding a current from the output to the emitter of the UJT which is equal to the current diverted into the base of the NPN transistor at the switching point. If this was not done the frequency would be dependent on the setting of the RATIO potentiometer.

The ratio of the circuit as shown can be varied from 0 to 100% and the frequency can be varied from approximately 60 cps to 1000 cps. Rise and fall times of the output waveform are approximately 1/500 of the period of oscillation.

PULSE GENERATOR (VARIABLE FREQUENCY AND DUTY CYCLE)
Figure 13.60

STAIRCASE WAVE GENERATOR

The circuit shown in Figure 13.61 can be used to generate a staircase waveform over a wide frequency range. An NPN-PNP emitter follower output circuit is used to achieve a high input impedance and a low output impedance to reduce the droop in the output voltage between pulses. The bias for the NPN transistor is obtained from the 1.8 megohm resistor across D3 and D4 and is effectively bootstrapped on the output to maintain the high input impedance. The staircase wave is generated by a diode-capacitor pump (D2 and C2) which is also bootstrapped on the output to maintain equal amplitude on each step. The number of steps per cycle depends on the ratio of C1 to C2 and the amplitude of the input pulse. For the circuit values shown a staircase of 10 steps is obtained with a 12 volt pulse input having a width = 4 (Rg C2) microseconds, where Rg is the impedance of the pulse generator. The input impedance of the amplifier as determined by the droop on the output voltage is approximately 15 megohms, giving satisfactory waveforms at frequencies as low as 50 cycles.

STAIRCASE WAVE GENERATOR WITH LOW IMPEDANCE OUTPUT
Figure 13.61

ONE-SHOT MULTIVIBRATOR (Fast Recovery and Wide Frequency Range)

This hybrid one-shot multivibrator circuit, Figure 13.62, is an improved configuration which provides a wide timing range, good timing stability, fast clean waveforms, and operation over an extreme range of duty cycle. Even though silicon diodes and transistors are used exclusively the overall circuit cost is low owing to the low cost of the components.

In the quiescent state Q1 is *off*, Q2 is *on* and the emitter voltage of the UJT is clamped to a low voltage through D2 and the collector of Q2. A negative trigger at the input turns off Q2 and permits C1 to charge through R1. When the UJT triggers, the negative pulse generated across the 10 ohm resistor is coupled through D3 to the base of Q1, turning off Q1 and setting the circuit back to its initial state. Capacitor C1 is rapidly discharged through D2 and the collector Q2 resulting in fast recovery. The circuit can thus be retriggered immediately after completion of a timing cycle without loss in overall timing accuracy. Resistor R1 provides the main time delay adjustment. Resistor R2 provides a normalizing adjustment for R1 to compensate for

minor variations in the value of C1, R1, D2, and the intrinsic standoff ratio (η) of the UJT. If this normalizing adjustment is not required R2 can be eliminated and a single 1K resistor used in the collector of Q2.

ONE-SHOT MULTIVIBRATOR WITH FAST RECOVERY AND WIDE FREQUENCY RANGE

Figure 13.62

VOLTAGE-TO-FREQUENCY CONVERTER

This voltage-to-frequency converter shown in Figure 13.63 gives an output frequency proportional to the input voltage with 1 volt producing a frequency of 1 kc. The input impedance is 100K. The linearity is better than 0.1% and the short term equivalent input voltage drift is less than 0.5 millivolts.

Overall negative feedback is used to achieve the high degree of linearity and stability. The transistors form an operational amplifier with an overall voltage gain of 5000 at the emitter of the UJT. Each time the UJT fires a fixed quantity of charge is fed back to the input of the operational amplifier through C1, C2, and the diode.

VOLTAGE-TO-FREQUENCY CONVERTER

Figure 13.63

The average current fed back to the input is proportional to the frequency so that the frequency must be proportional to the input voltage to maintain the summing point of the operational amplifier at zero potential.

To adjust the circuit, close SW1 and set R2 to the point where oscillations just start. Open SW1, apply 1 millivolt at the input and set R3 to the point where the frequency is approximately 1 cps. Apply 1 volt at the input and set C2 to the point where the frequency is 1000 cps. If this setting is outside the range of C2 replace or trim C1, using mica capacitors only. The voltage supplies used for this circuit should be at least as stable as the required measurement accuracy.

REFERENCES

(1) Sylvan, T.P., "Notes on the Application of the Unijunction Transistor," Pub. No. 90.10, 1961, General Electric Company, Electronics Park, Syracuse, New York.

(2) "Silicon Controlled Rectifier Manual", 2nd. Edition, General Electric Company, Rectifier Components Department, Auburn, New York, (1964)

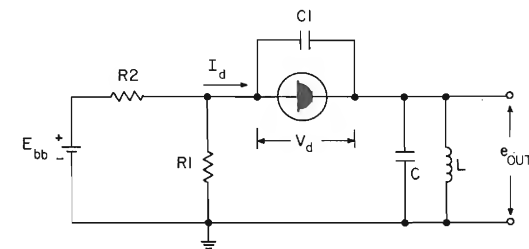
NOTES

NOTES

TUNNEL DIODE CIRCUITS

CHAPTER 14

TUNNEL DIODE OSCILLATORS(1-18)

Tunnel Diode Oscillators are attractive because of their high-frequency capability, low power consumption, good frequency stability and extreme circuit simplicity. These advantages enable a designer to produce stable miniature oscillator circuits with a wide variety of uses. Figure 14.1 illustrates the *basic* "series-parallel" sinewave oscillator. Design equations are also given. Additional design information will be found by consulting the references at the end of this chapter.

$$R1 \leq \frac{|R_d|}{3}$$ where R_d is TD's negative resistance.

$$R2 = \frac{E_{bb} - V_d}{I_d + \frac{V_d}{R1}}$$

$$C1 = \sqrt{\frac{g_{di}\,(1 - R_T\, g_{di})}{R_T\, \omega^2}}$$ where g_{di} is TD's initial negative conductance
R_T is circuit's total dc resistance and

is equal to $\frac{R1\ R2}{R1 + R2} + R_S + R_{DC\,(coil)}$

R_S is TD's total series resistance.

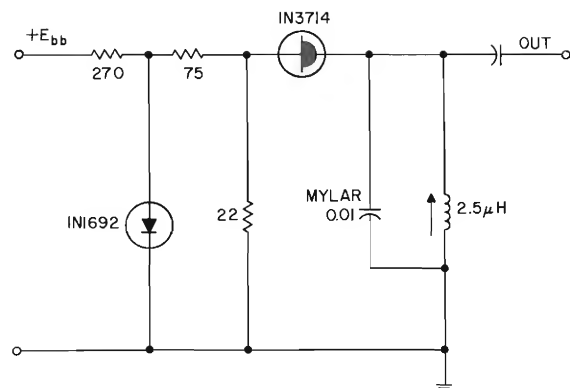
$$C + \frac{C_1}{1 - R_T\, g_d} = \frac{1}{L\, \omega^2}$$ where g_d is TD's negative conductance.

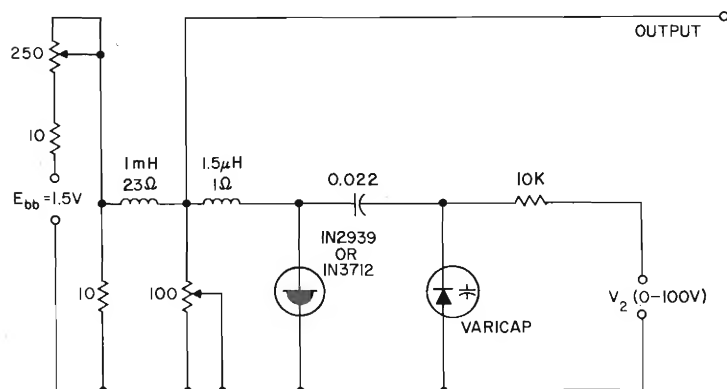
hence

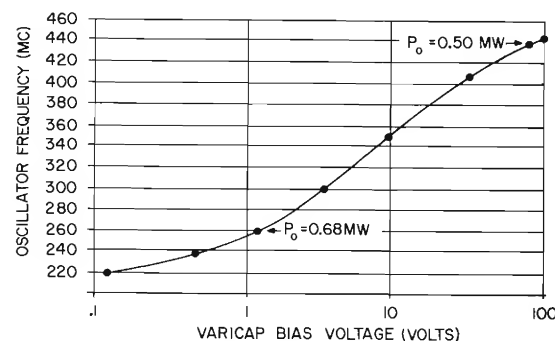
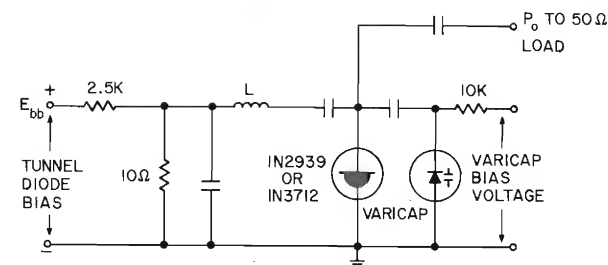
$$L = \frac{1}{\omega^2 \left(C + \frac{C1}{1 - R_T\, g_d}\right)}$$

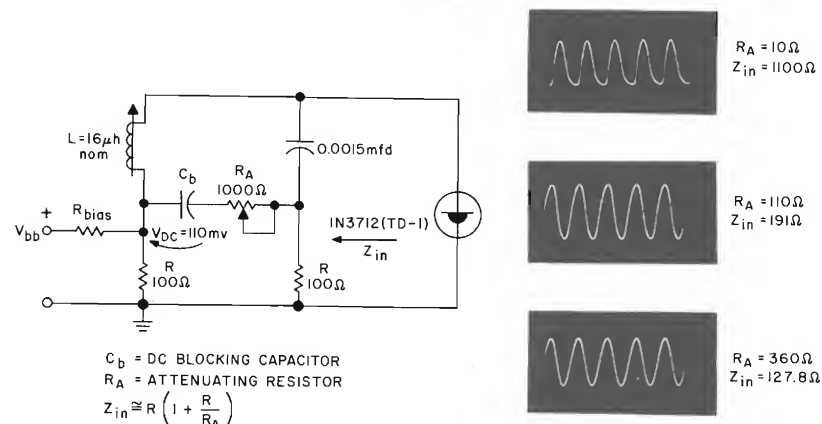
BASIC TUNNEL DIODE SINEWAVE OSCILLATOR AND DESIGN EQUATIONS

Figure 14.1

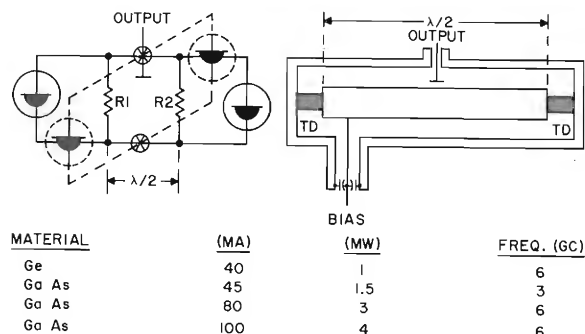
The circuits that follow illustrate the many applications and variety of tasks tunnel diode oscillators are capable of performing. Brief descriptions accompany some circuits. For more complete information readers should consult the specific reference as indicated. An extensive reference list appears at the end of this chapter.

This 1.1 mc oscillator senses temperature changes and translates them into frequency variations. The main temperature sensing element is a mylar capacitor whose characteristics yield a 0.5 kc/°C temperature coefficient.[1]

TEMPERATURE SENSING OSCILLATOR
Figure 14.2

A voltage variable capacitor tunes this oscillator electronically over the 12-22 mc range.[1]

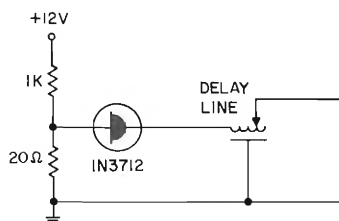
VOLTAGE CONTROLLED OSCILLATOR
Figure 14.3

This VHF oscillator can be electronically tuned over the 200-400 mc range. Output power is over 0.5 milliwatts.[1]

VOLTAGE CONTROLLED VHF OSCILLATOR
Figure 14.4

Resistor R_A is an attenuating resistor which varies the magnitude of the oscillator swing. This enables the oscillator to operate over a limited, hence highly linear portion, of the diode's conductance curve. Note low distortion in the oscilloscope display at the bottom.[4]

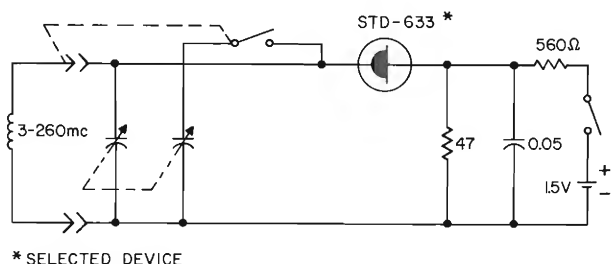
VARIABLE AMPLITUDE OSCILLATOR
Figure 14.5

MATERIAL	(MA)	BIAS (MW)	FREQ. (GC)
Ge	40	1	6
Ga As	45	1.5	3
Ga As	80	3	6
Ga As	100	4	6

Two or more tunnel diodes placed in a half-wave cavity structure delivers 4 milliwatts at 6 kmc.[13]

MICROWAVE OSCILLATOR

Figure 14.6

Using a General Radio Delay-Line (Type 314-S86) this oscillator covers the 0.5-20 mc range. Output is in the square wave category.

DELAY-LINE OSCILLATOR

Figure 14.7

SINEWAVE OSCILLATOR WITH "PLUG-IN" COILS

(Covers 3 to 260 mc range)

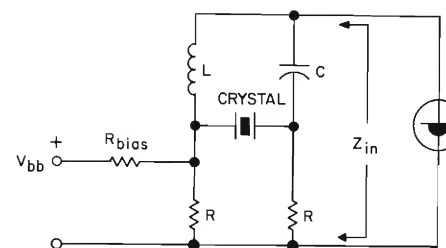
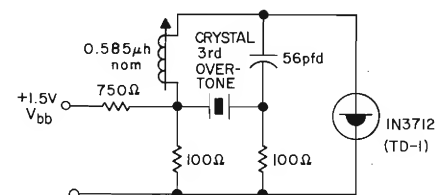
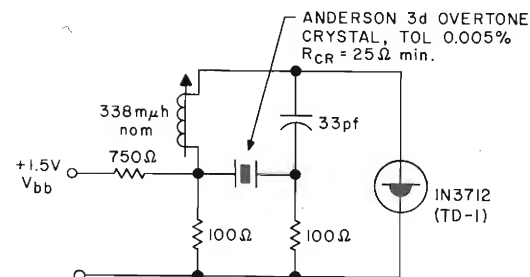
Figure 14.8

BASIC TUNNEL DIODE CRYSTAL CONTROLLED OSCILLATOR[7]

Figure 14.9

Figures 14.10 and 14.11 show crystal controlled Citizens Band and Fire Department oscillators. Both are useable in low power (microwatt) transmitters for short range communications.[7]

THE OSCILLATOR FREQUENCY OPERATES WITHIN THE TOLERANCE OF THE QUARTZ CRYSTAL OVER A TEMPERATURE RANGE OF FROM -55°C TO +85°C AND A BIAS RANGE OF FROM 110 TO 150mv.

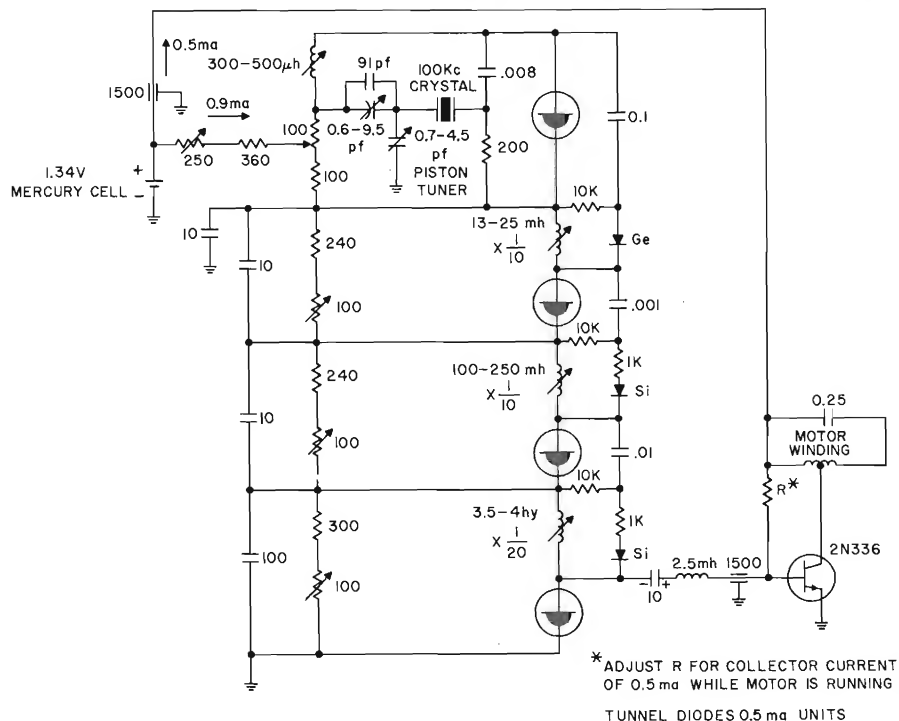
CITIZENS BAND 27.255 MC CRYSTAL CONTROLLED OSCILLATOR

Figure 14.10

THE OSCILLATOR FREQUENCY OPERATES WITHIN THE QUARTZ CRYSTAL TOLERANCE OVER A TEMPERATURE RANGE OF FROM -55°C TO +85°C AND OVER A BIAS RANGE OF FROM 110 TO 150mv.

FIRE DEPARTMENT 47.100 MC CRYSTAL CONTROLLED OSCILLATOR

Figure 14.11

*ADJUST R FOR COLLECTOR CURRENT OF 0.5 ma WHILE MOTOR IS RUNNING

TUNNEL DIODES 0.5 ma UNITS

This circuit illustrates an application where the low power consumption, the low voltage requirements, and the excellent frequency stability of crystal controlled tunnel diode oscillators provides the circuit designer with an ideal device for his job. The complete circuit incorporates trimmers that can adjust the timing of the clock by a few seconds per year. Three tunnel diodes give overall division ratio of 2,000 to 1. Figure 14.13 pictures the finished chronometer.

CRYSTAL CONTROLLED CHRONOMETER[8]

Figure 14.12

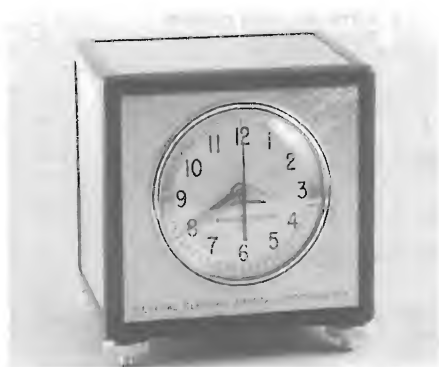
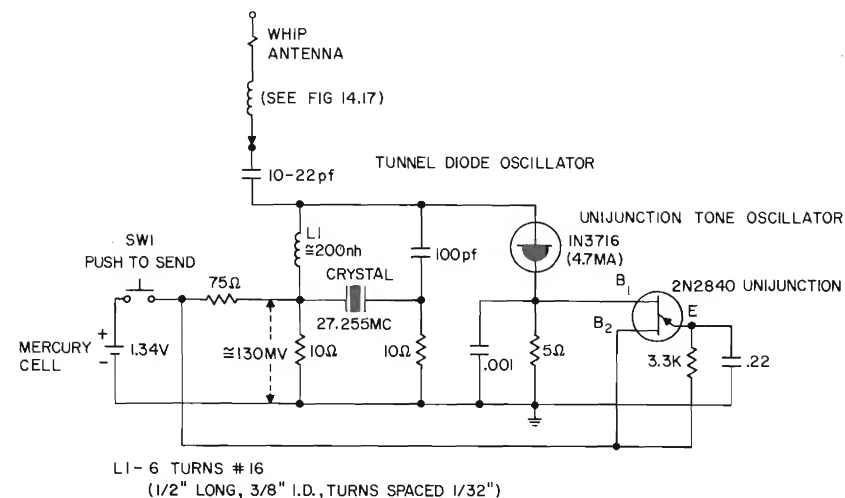



Figure 14.13 HIGH ACCURACY CHRONOMETER

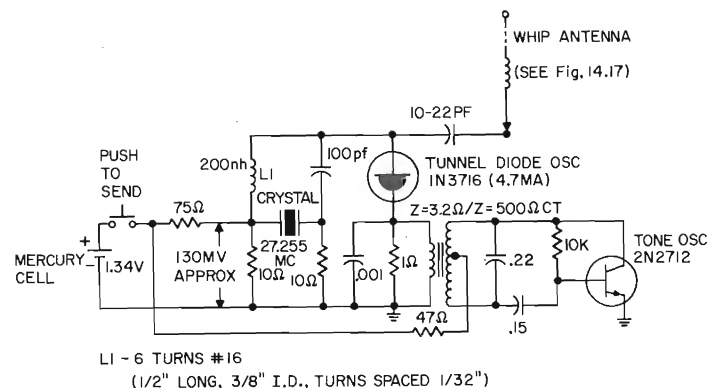
TUNNEL DIODE MICRO-POWER TRANSMITTERS[1,5]

Tunnel diode remote control transmitters have adequate range to remote control toys, garage doors, window displays, etc. Where voice modulated they can be used for short range communications, as in television studios, power plants, bowling alleys, shopping centers, etc.

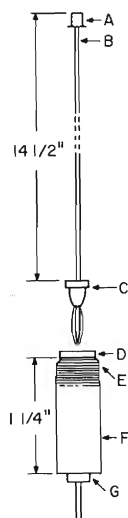
Circuits in Figures 14.15 and 14.16 can be built into miniature hand-held box chassis as shown below.

Figure 14.14

Unijunction tone oscillator modulates this miniature transmitter used to remotely control garage door.

TUNNEL DIODE-UNIJUNCTION REMOTE CONTROL TRANSMITTER

Figure 14.15

Hartley oscillator using silicon transistor modulates tunnel diode transmitter.

TUNNEL DIODE-TRANSISTOR REMOTE CONTROL TRANSMITTER

Figure 14.16

Details of antenna and loading coil construction for Figures 14.5 and 14.6.

ANTENNA

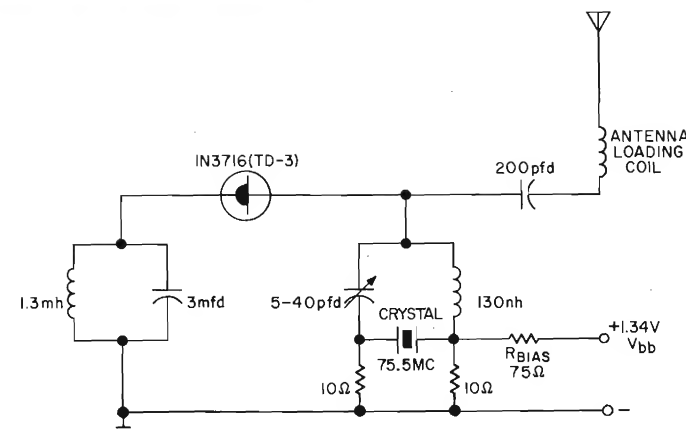
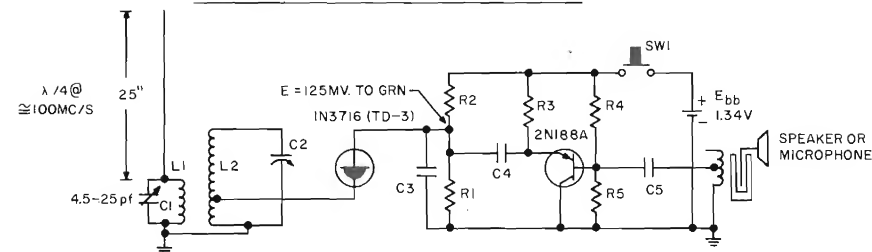
Figure 14.17

73.5 MC CRYSTAL CONTROLLED SELF-MODULATED TRANSMITTER

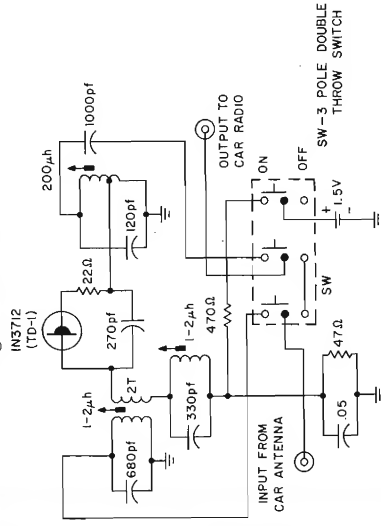
Figure 14.18

L1 2 TURNS #16 COPPER 3/8"ID SPACED 1/8" FROM GROUND END OF L2 (ADJUST FOR BEST STABILITY)
L2 6 TURNS #16 COPPER 3/8"ID CLOSE-WOUND AND CONNECTED DIRECTLY TO C2. TAPPED 1 TURN FROM GROUND.
C1 4.5-25 $\mu\mu$fd CERAMIC TRIMMER
C2 1.5-5 $\mu\mu$fd VARIABLE
C3 800 $\mu\mu$fd (VOLTAGE NOT IMPORTANT-SELECT FOR SMALL SIZE)
C4 50 μfd 6 VDC ELECTROLYTIC (VOLTAGE NOT IMPORTANT-SELECT FOR SMALL SIZE)
C5 1 μfd 35 VDC (VOLTAGE NOT IMPORTANT-SELECT FOR SMALL SIZE)
R1 18Ω 1/2 W 5%
R2 150Ω 1/2 W 5%
R3 470Ω 1/4 W
R4 10KΩ 1/4 W
R5 10KΩ 1/4 W
E_{bb} MALLORY RM-12R MERCURY CELL 1.34 VDC-3600 MAH
Sw1 NORMALLY OPEN SPST "PUSH-TO-TALK" SWITCH
SPKR 2" PM SPEAKER
IN3716 (TD-3) 4.7MA AXIAL TUNNEL DIODE

This circuit has a 200 yard range when used in conjunction with sensitive commercial receiver.

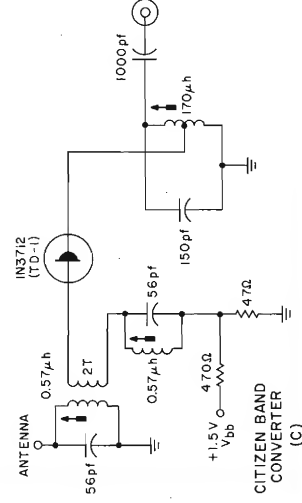
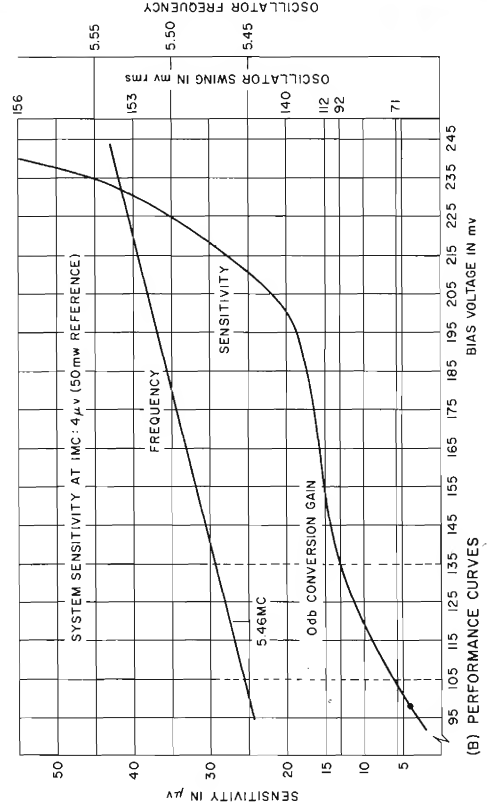
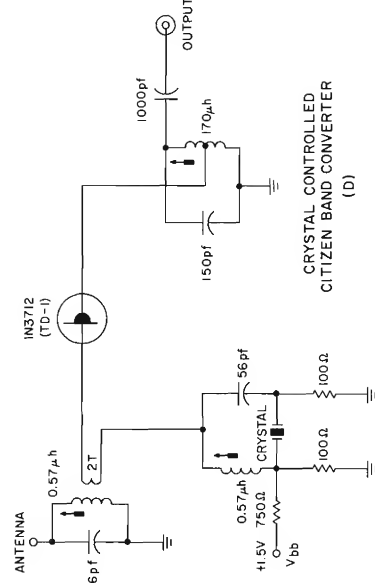
FM WIRELESS MICROPHONE
(96 to 110 mc)

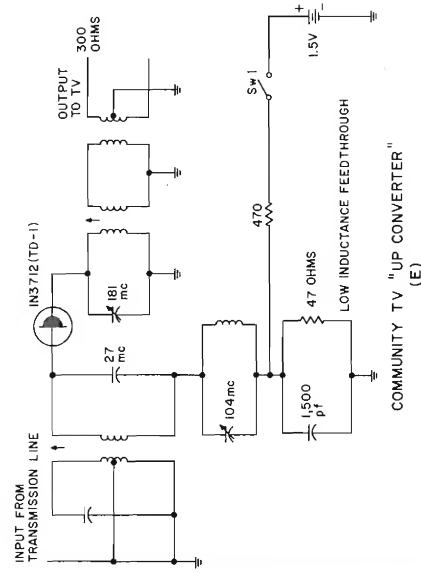
Figure 14.19

TUNNEL DIODE CONVERTERS (1, 2, 19-23)

The tunnel diode oscillator can be used in the design of "self-oscillating" converters.

CIVIL AIR PATROL CONVERTER
(A)

SYSTEM SENSITIVITY AT IMC: 4μv (50mw REFERENCE)
FREQUENCY
SENSITIVITY
5.46MC
0db CONVERSION GAIN
SENSITIVITY IN μv
OSCILLATOR SWING IN mv rms
OSCILLATOR FREQUENCY
BIAS VOLTAGE IN mv

(B) PERFORMANCE CURVES

CITIZEN BAND
CONVERTER
(C)

CRYSTAL CONTROLLED
CITIZEN BAND CONVERTER
(D)

INPUT FROM
TRANSMISSION LINE
IN3712(TD-I)
OUTPUT
TO TV
300
OHMS
27
mc
181
mc
104mc
470
Sw I
1,500
pf
47 OHMS
1.5V
LOW INDUCTANCE FEEDTHROUGH

COMMUNITY TV "UP CONVERTER"
(E)

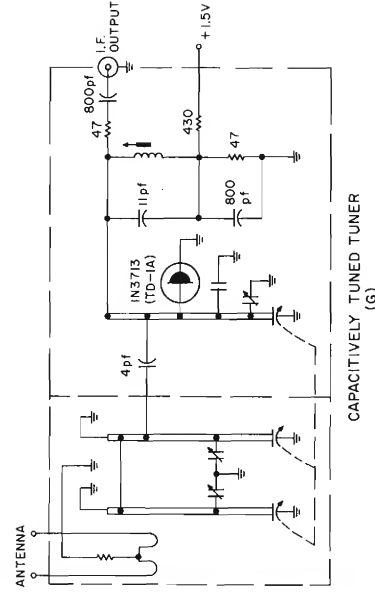
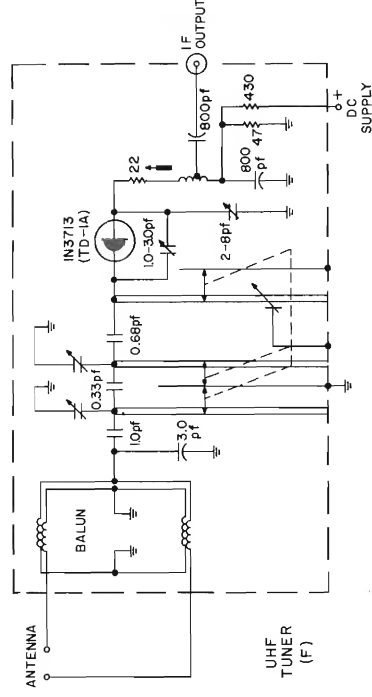
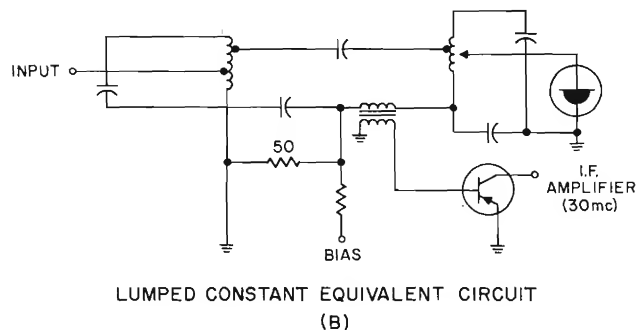
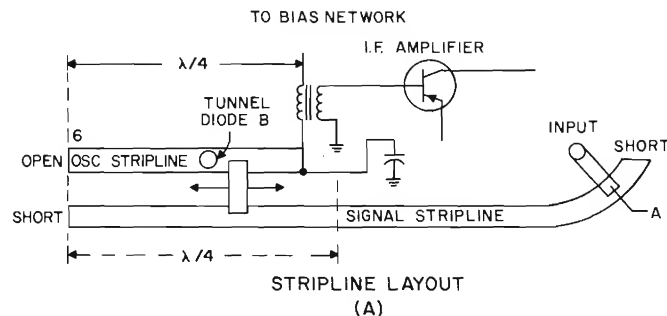
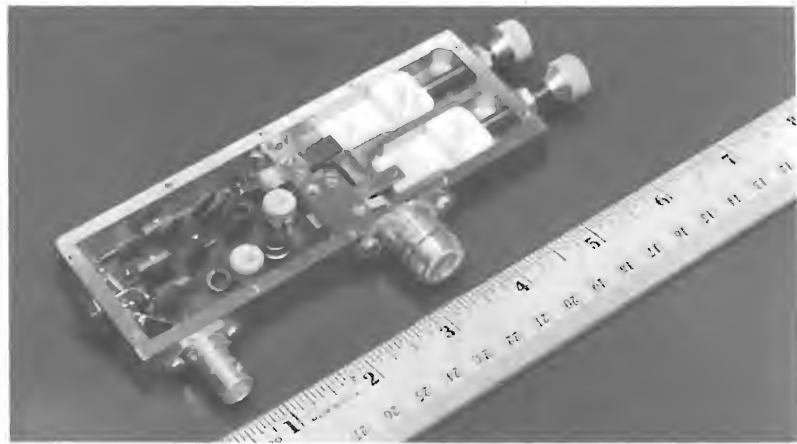
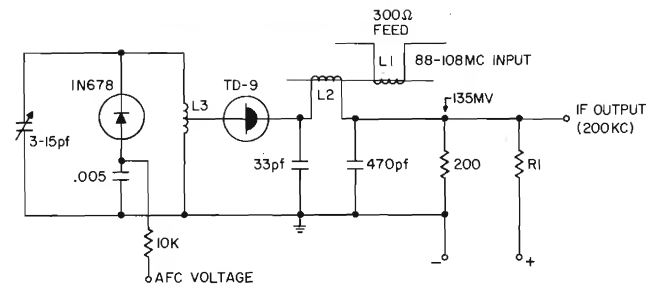
UHF
TUNER
(F)

CAPACITIVELY TUNED TUNER
(G)

(H)

Figure 14.20 SELF-OSCILLATING TUNNEL DIODE CONVERTERS

STRIPLINE LAYOUT
(A)

LUMPED CONSTANT EQUIVALENT CIRCUIT
(B)

L-BAND SELF-OSCILLATING CONVERTER
Figure 14.21

3 KMC L-BAND CONVERTER PACKAGE
Figure 14.22

L1 - 4 TURNS #18-3/8" ID, APPROX. 1/2" LONG
L2 - 4 TURNS #18-3/8" ID, APPROX. 1/2" LONG
L3 - 8 1/2" TURNS #18-3/8" ID, APPROX. 3/4" LONG TAPPED AT 5 TURNS
L1L2 - COUPLED END TO END, SPACED ~ 1/8" APART
R1 - DEPENDS ON SUPPLY VOLTAGE. SELECT FOR BIAS OF APPROX. 135MV ACROSS 200Ω RESISTOR.

This converter is AFC controlled by a variable capacitance diode. The 200 kc IF output is used here because of the type of receiver design (see Figure 15.21).

Figure 14.23 FM-AFC CONTROLLED CONVERTER

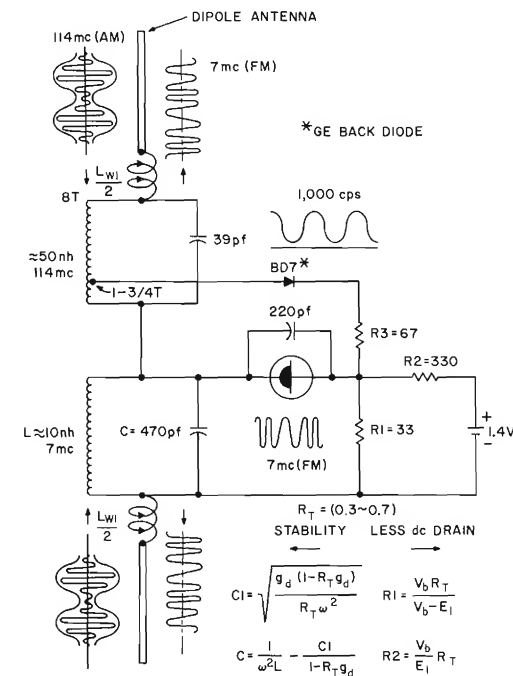



Figure 14.24 TUNNEL DIODE TRANSCEIVER[19]

This transceiver is tuned for a 114 mc AM input signal and a 7 mc FM output signal. The 1N3714 (TD-2) tunnel diode acts as 7 mc RF oscillator and frequency modulator while the BD-7 back diode is the 114 mc detector.

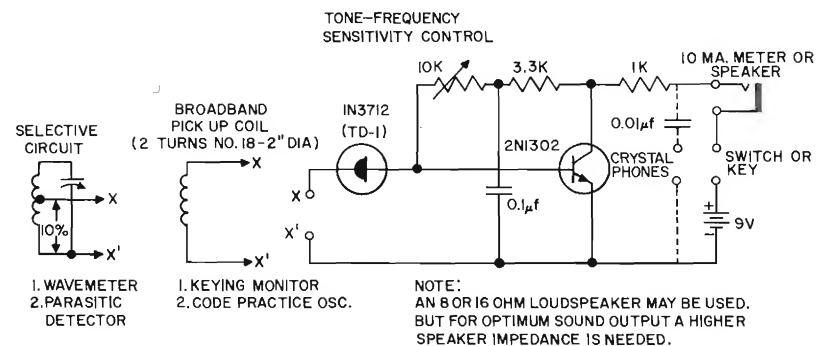
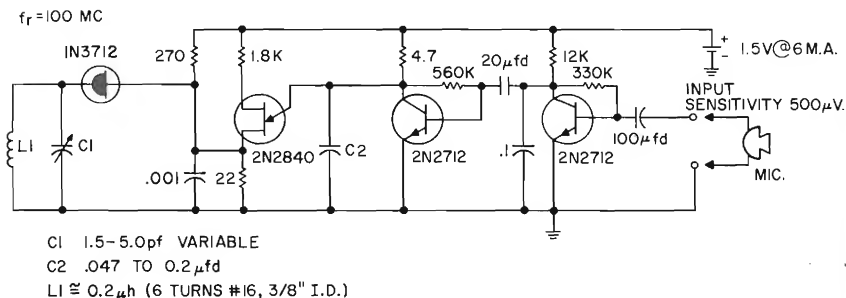
VARIOUS INDUSTRIAL SPECIAL USES OF TUNNEL DIODES(34-41)

SENSITIVE BROADBAND CW KEYING MONITOR-CODE PRACTICE OSCILLATOR-SENSITIVE AURAL/VISUAL PARASITIC DETECTOR OR WAVEMETER

Figure 14.25

100 mc wireless telemetry link transmitter. The microphone picks up signal which is amplified by 2N2712; second 2N2712 inhibiting C1 turns off allowing C1 to charge up and fire 2N2840 unijunction oscillator. Unijunction pulse modulates a tunnel diode transmitter.

WIRELESS PULSE MONITOR

Figure 14.26

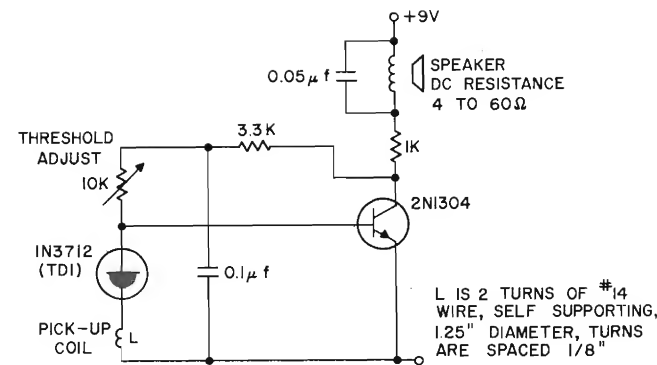
This circuit illustrates a 200 mc, RF radiation detector giving audible (1800 cps) alarm oscillations. A small slot antenna or a pick-up coil can be used as sensors.

RF RADIATION DETECTOR(41)

Figure 14.27

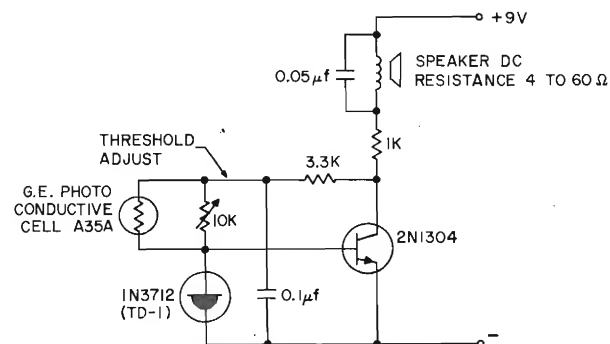
This is a variation of the circuit shown in Figure 14.27. Here the sensor is a photo-conductive cell giving alarm at below 0.1 foot candles of illumination near 5500 angstroms.

LIGHT DETECTOR

Figure 14.28

TUNNEL DIODE AMPLIFIERS(1, 2, 42-45)

The performance of tunnel diodes in low noise amplifiers is especially attractive at UHF and microwave frequencies where ferrite isolators, circulators, and/or hybrid-couplers can be used to unilateralize the signal flow. At frequencies where these devices are not available, stable gain is difficult to achieve. Tunnel diodes have been used at L, S, C, and X band with excellent stability and low noise performance.

THREE PORT CIRCULATOR (A)

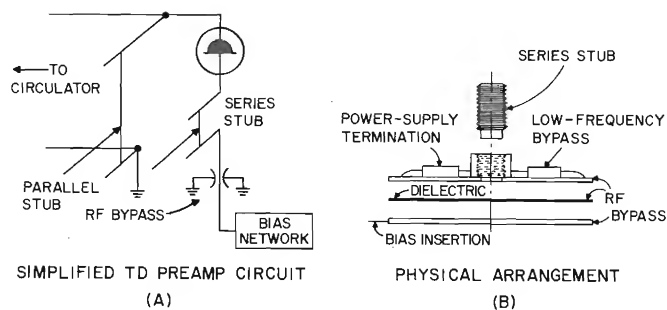
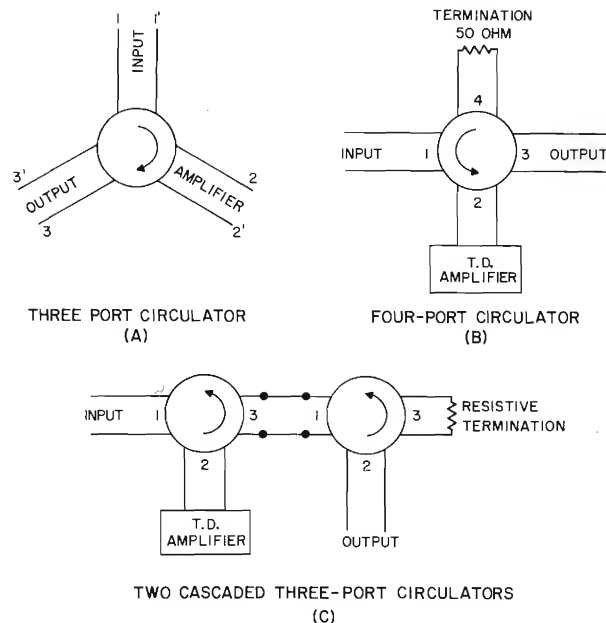
FOUR-PORT CIRCULATOR (B)

TWO CASCADED THREE-PORT CIRCULATORS (C)

TUNNEL DIODE UHF CIRCULATORS
Figure 14.29

SIMPLIFIED TD PREAMP CIRCUIT (A)

PHYSICAL ARRANGEMENT (B)

THREE-PORT CIRCULATOR COUPLED L-BAND AMPLIFIER (C)

UHF PREAMPLIFIERS
Figure 14.30

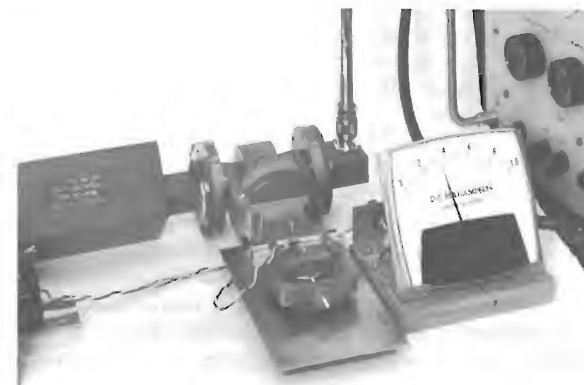



Figure 14.31 TUNNEL DIODE SIX-GIGACYCLE WAVEGUIDE AMPLIFIER

SIGNAL DISTRIBUTION IN HYBRID-COUPLER (A)

TUNNEL DIODE AMPLIFIER (B)

$$r^2 = \frac{\left[\frac{f_0^2}{f_1^2} - 1 - \frac{Z_0}{|-R_d|} + \frac{R_S}{-R_d}\right]^2 + \frac{f_0^2}{f_1^2}\left[\frac{Z}{|-R_d|} + \frac{Z_0/|-R_d|}{Z/|-R_d|} - \frac{R_S/|R_d|}{Z/|-R_d|}\right]^2}{\left[\frac{f_0^2}{f_1^2} - 1 + \frac{Z_0}{|-R_d|} + \frac{R_S}{|-R_d|}\right]^2 + \frac{f_0^2}{f_1^2}\left[\frac{Z}{|-R_d|} - \frac{Z_0/|-R_d|}{Z/|-R_d|} - \frac{R_S/|-R_d|}{Z/|-R_d|}\right]^2}$$

Z_0 = CHARACTERISTIC IMPEDANCE $\quad f_1 = \frac{1}{2\pi\sqrt{LC}}$

$Z = \sqrt{L/C}$ $\quad |-R_d|$ = NEGATIVE RESISTANCE OF THE DIODE

HYBRID-COUPLED TUNNEL DIODE AMPLIFIER AND GAIN EQUATION (C)

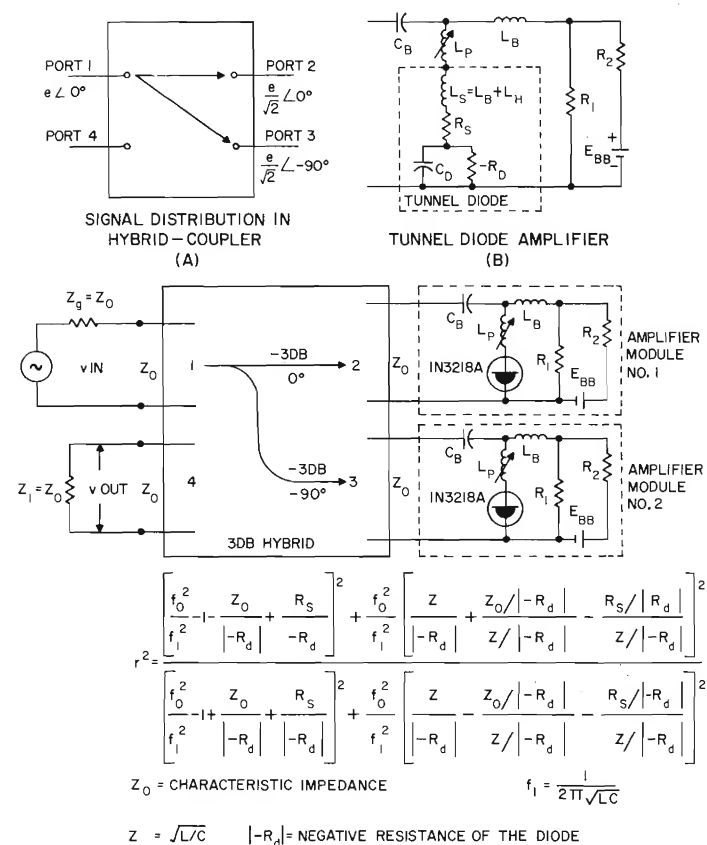



Figure 14.32

The tunnel diode is a very useful device in switching circuits because of its

1. Very high switching speed capabilities
2. Low power consumption
3. Well defined thresholding properties
4. Stable characteristics
5. Radiation resistance

It is the fastest switching device known, with transistion times as low as 27 picoseconds (27×10^{-12} second or the time it takes light to travel 0.3 inches). The speed of most high speed circuits is limited by the circuit and package inductance and capacitance and not by the tunnel diode.

Figures 14.33 through 14.35 show various types of low power consumption tunnel diode multivibrators. Figure 14.36 through 14.41 is representative of circuits where the tunnel diode is used with a transistor. The transistors are used to provide amplification with the exception of Figures 14.38 and 14.39 where they are used as a shorting — resetting element.

Figure 14.42 shows a selection of some high speed logic circuits developed to take advantage of the tunnel diodes ultra-high-speed switching capabilities.

TUNNEL DIODE MULTIVIBRATORS[2]

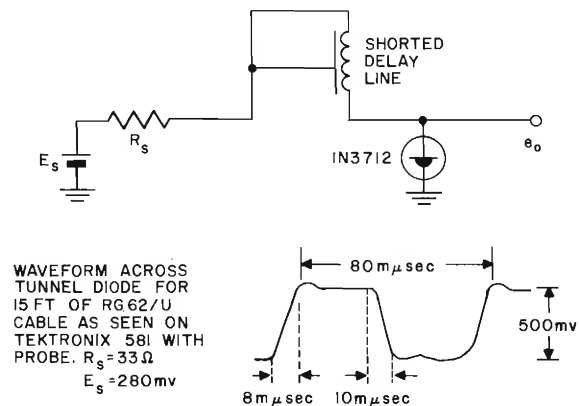



Figure 14.33 RELAXATION OSCILLATOR USING A SHORTED DELAY LINE

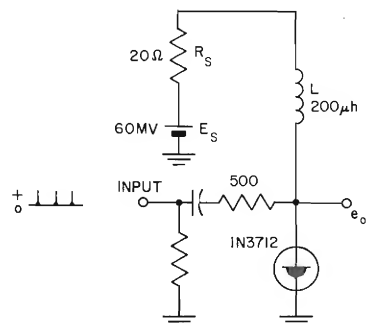



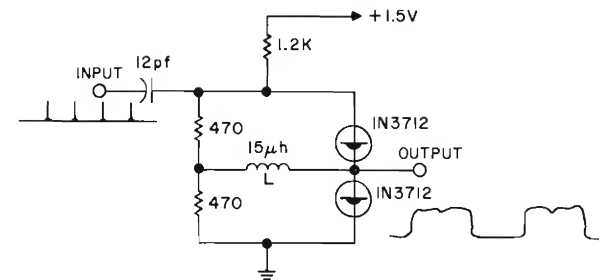
Figure 14.34 TUNNEL DIODE MONOSTABLE OSCILLATOR

TUNNEL DIODE FLIP-FLOP

Figure 14.35

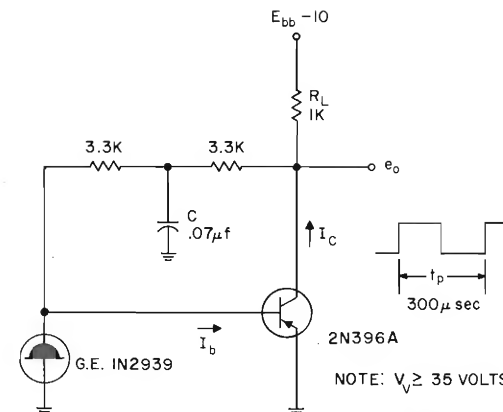
HYBRID (TRANSISTOR-TUNNEL DIODE) MULTIVIBRATORS[2]

ASTABLE HYBRID OSCILLATOR

FIGURE 14.36

BISTABLE CIRCUIT USING TUNNEL DIODE AND NPN GERMANIUM ALLOY TRANSISTOR

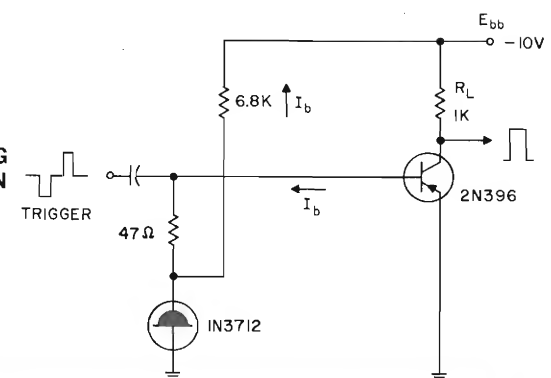
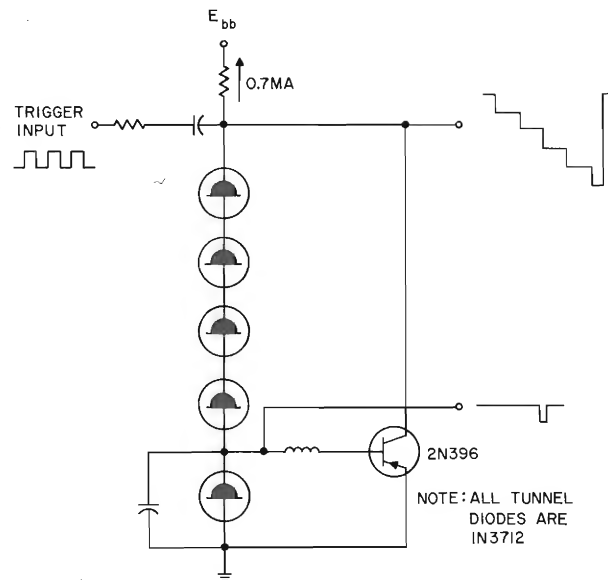
Figure 14.37

TUNNEL DIODE COUNTERS[1, 2]

SERIES CONNECTED TUNNEL DIODES USED FOR 5:1 PULSE FREQUENCY DIVIDER OR STAIRCASE WAVE GENERATOR

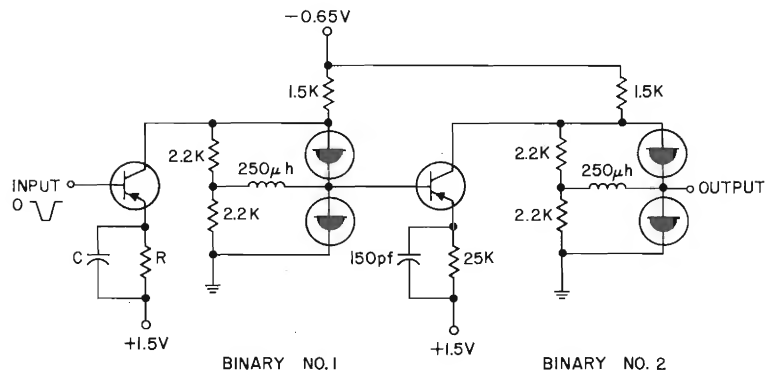
Figure 14.38

LOW LEVEL TUNNEL DIODE COUNTER

Figure 14.39

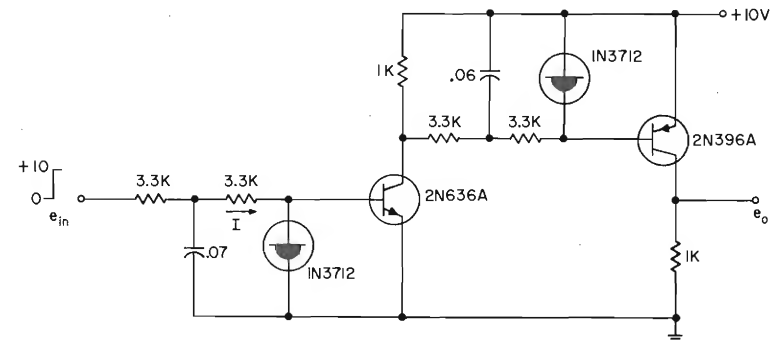
MISCELLANEOUS TUNNEL DIODE CIRCUITS[2]

TUNNEL DIODE TIME DELAY CIRCUIT WITH TWO CASCADED COMPLIMENTARY STAGES

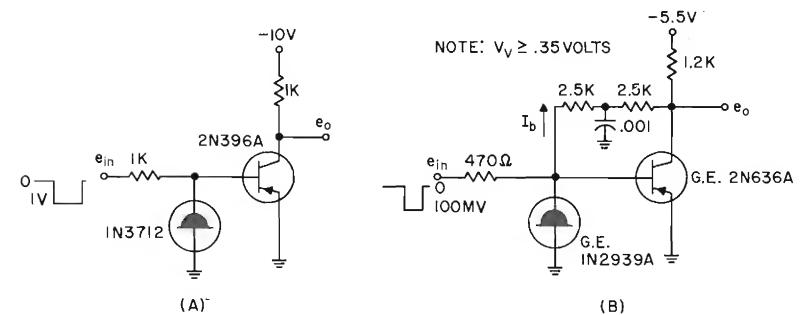
Figure 14.40

HYBRID LEVEL DETECTOR CIRCUITS

Figure 14.41

TUNNEL DIODE COMPUTER CIRCUITS[1]

TWO CASCADED MONOSTABLES FORM AN "OR" GATE
(A)

THREE CASCADED MONOSTABLES PROVIDE ADEQUATE GAIN IN "AND" GATE
(B)

BASIC PUMPED TUNNEL DIODE TRANSISTOR LOGIC GATES SHOWN INTERCONNECTED
(C)

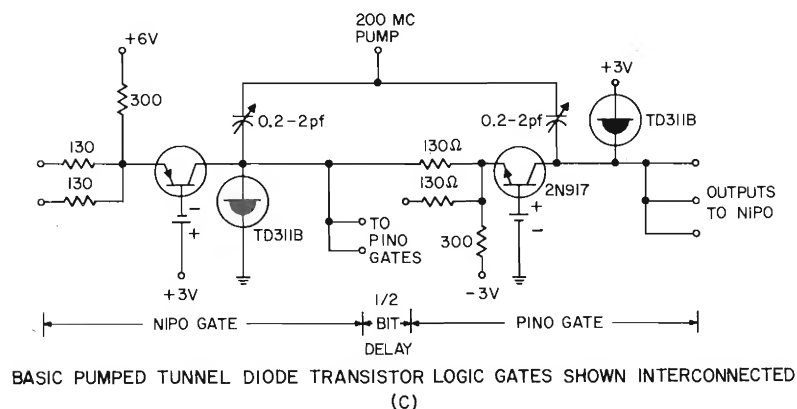
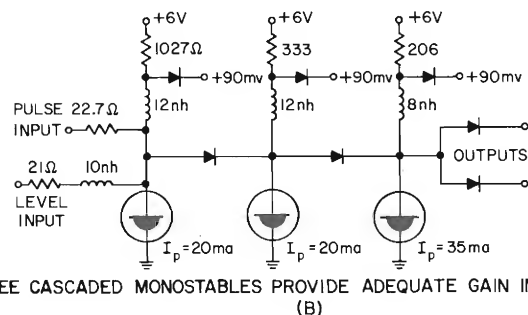
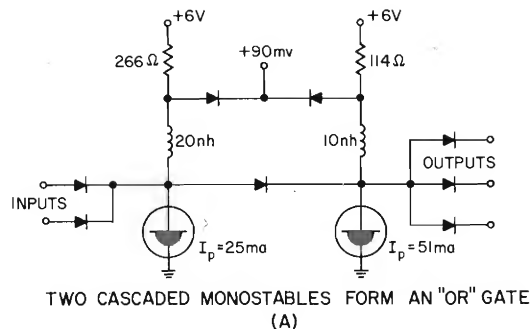
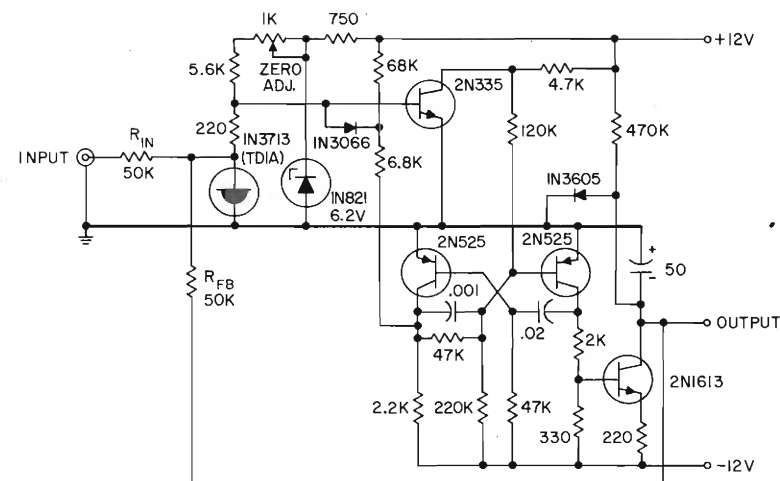
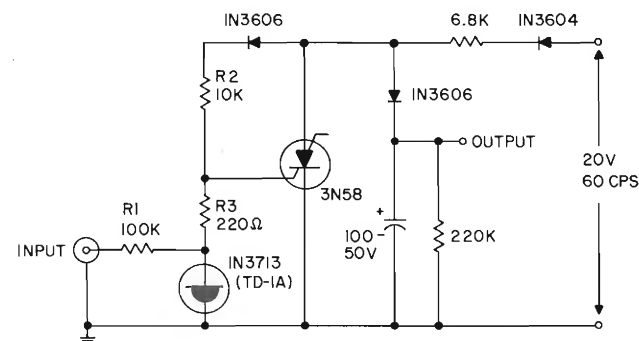
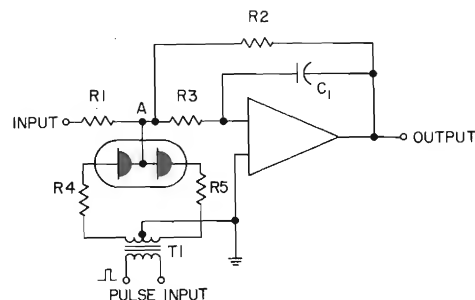



Figure 14.42

This circuit operates as a slideback sensing circuit[50] to give a dc output which is proportional to the positive peak of a repetitive input signal. With proper choice of the tunnel diode and the input circuit layout it is possible to measure the peak amplitude of pulses as narrow as one nanosecond. The circuit is similar to an operational amplifier with a voltage gain determined by the ratio R_{FB}/R_{IN}.

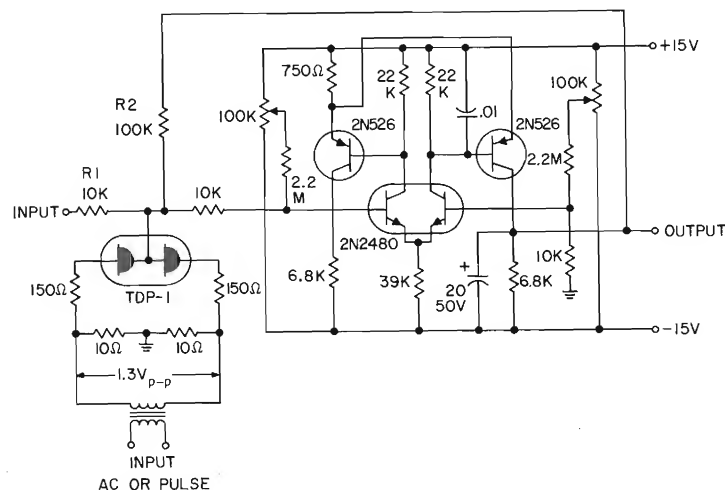
TUNNEL DIODE PEAK SENSING OPERATIONAL AMPLIFIER

Figure 14.43

A simple peak reading voltmeter circuit using a tunnel diode together with a silicon controlled switch to give a dc output proportional to the positive peak of the input signal. Voltage gain is equal to $(R2 + R3)/R1$.

AC OPERATED PEAK READING VOLTMETER

Figure 14.44

A tunnel diode pair used in conjunction with an operational amplifier which functions as a sampling circuit with the output proportional to the input signal at the instant corresponding to the leading edge of the sampling pulse. Effective rise-time can be in the nanosecond range depending on the tunnel diodes used, the rise-time of the sampling pulse and the construction of the input circuitry. Voltage gain is determined by the ratio R2/R1.

OPERATIONAL SAMPLING CIRCUIT USING TUNNEL DIODE PAIR

Figure 14.45

A practical version of an operational sampling circuit using the principles shown in Figure 14.45. Voltage gain of the circuit is 100. Pulse synchronizing and pulse generating circuit details are not shown. This circuit can also be used to measure the differential peak point current of tunnel diode pairs.

PRACTICAL EXAMPLE OF OPERATIONAL SAMPLING CIRCUIT USING TUNNEL DIODE PAIR

Figure 14.46

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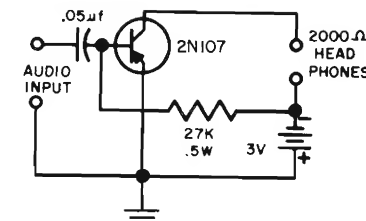
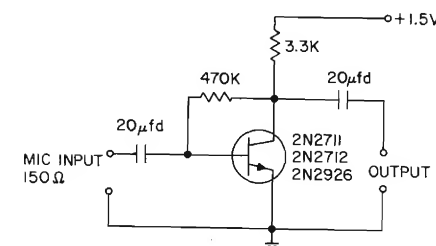
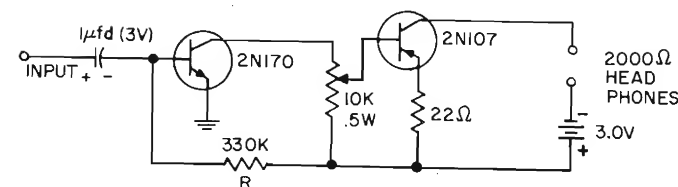
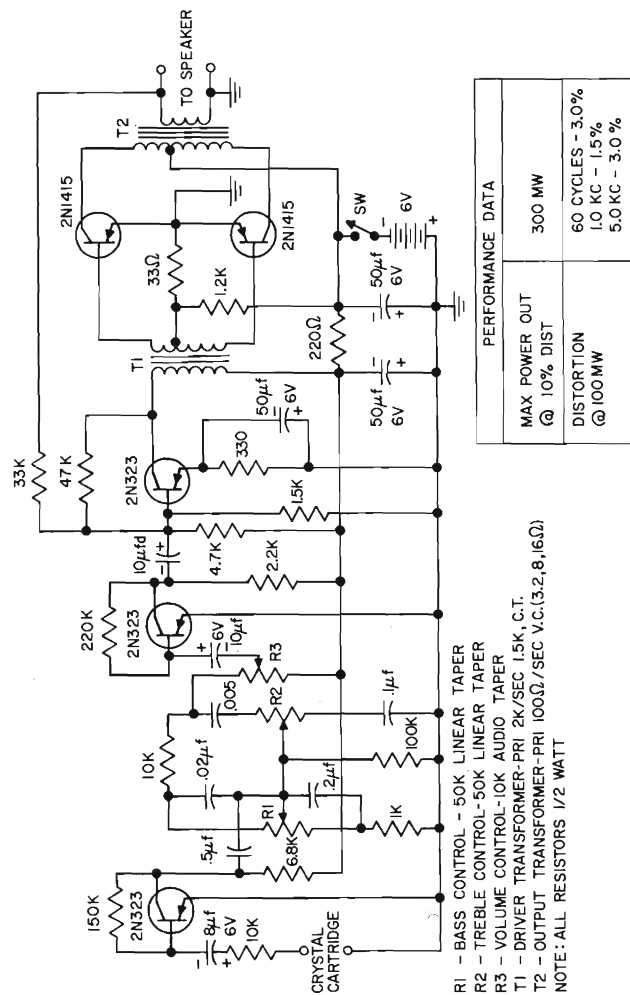
NOTES

EXPERIMENTERS CIRCUITS

SIMPLE AUDIO AMPLIFIER
Figure 15.1

LOW IMPEDANCE MICROPHONE PREAMPLIFIER
Figure 15.2

NOTE: ADJUST R FOR OPTIMUM RESULTS

DIRECT COUPLED "BATTERY SAVER" AMPLIFIER
Figure 15.3

PERFORMANCE DATA	
MAX POWER OUT @ 10% DIST	300 MW
DISTORTION @100MW	60 CYCLES - 3.0% 1.0 KC - 1.5% 5.0 KC - 3.0%

SIX VOLT PHONO AMPLIFIER
Figure 15.4

PERFORMANCE	
MAX POWER OUT @ 10% DIST	400 MW
DISTORTION @100MW	100 CYCLES - 5% 1 KC - 2% 5 KC - 5%

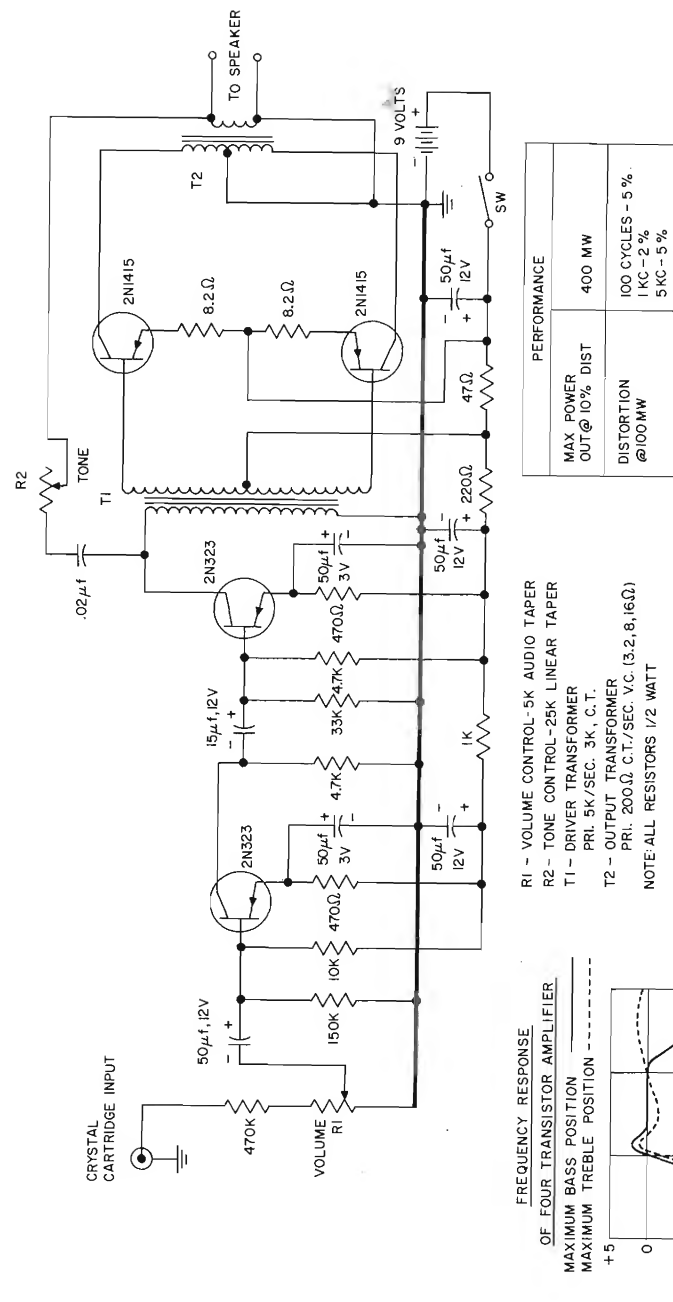



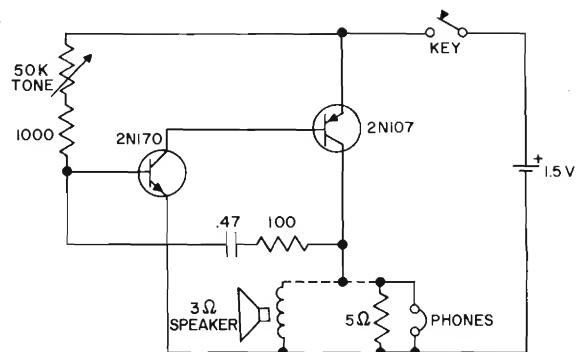
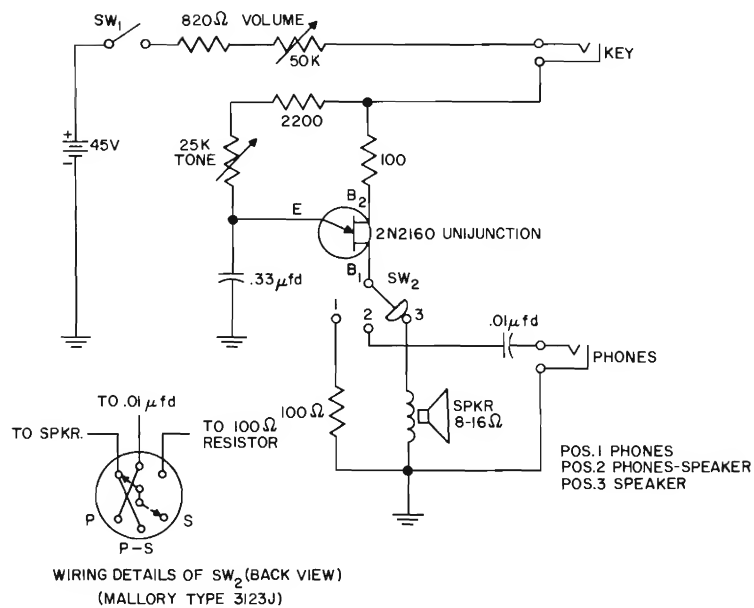
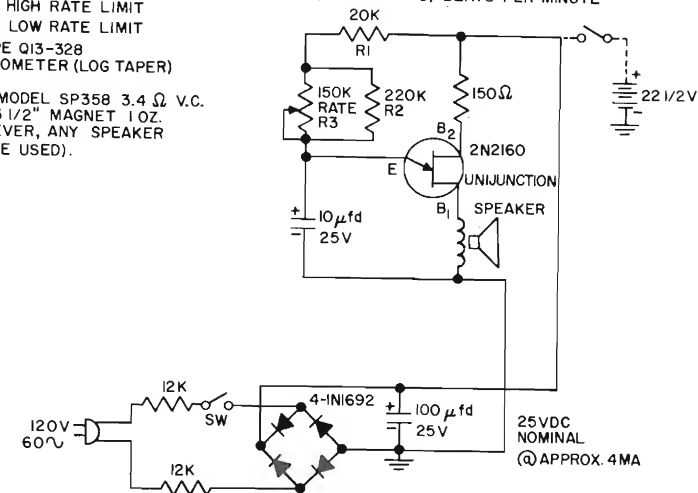
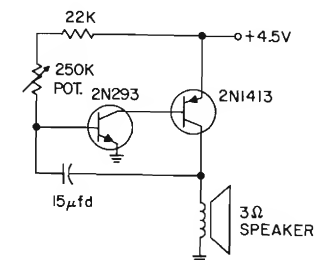
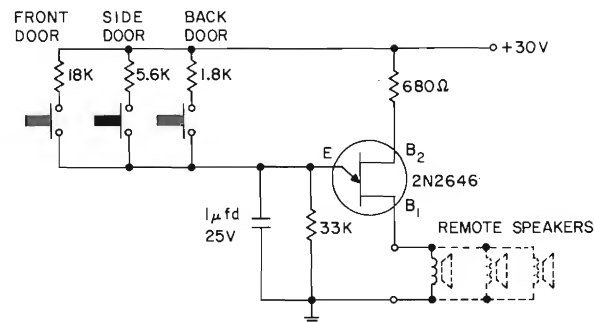
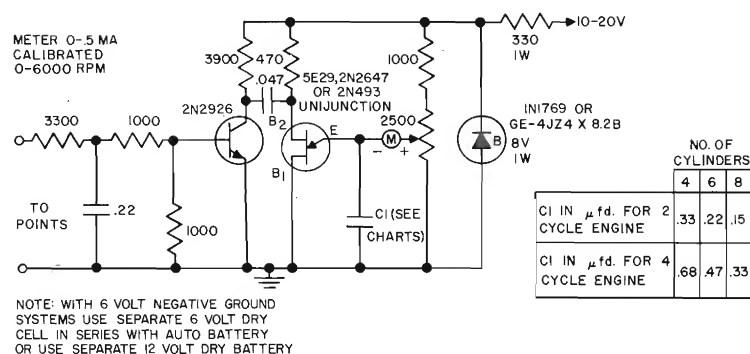
Figure 15.5 NINE VOLT PHONO AMPLIFIER

CODE PRACTICE OSCILLATOR
Figure 15.6

UNIJUNCTION TRANSISTOR CODE PRACTICE OSCILLATOR
Figure 15.7

UNIJUNCTION TRANSISTOR METRONOME
Figure 15.8

METRONOME
Figure 15.9

UNIJUNCTION HOME SIGNAL SYSTEM

Figure 15.10

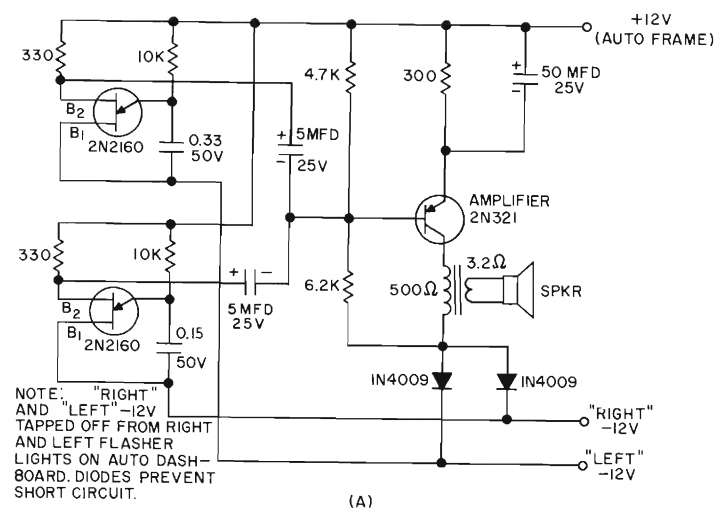
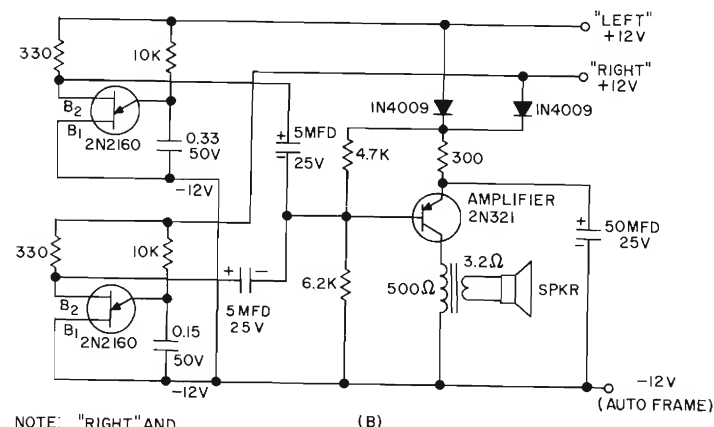
	4	6	8
C1 IN μfd. FOR 2 CYCLE ENGINE	.33	.22	.15
C1 IN μfd. FOR 4 CYCLE ENGINE	.68	.47	.33

NOTE: WITH 6 VOLT NEGATIVE GROUND SYSTEMS USE SEPARATE 6 VOLT DRY CELL IN SERIES WITH AUTO BATTERY OR USE SEPARATE 12 VOLT DRY BATTERY

GENERAL AUTOMOTIVE IGNITION INFORMATION

	TWO CYCLE			FOUR CYCLE		
	4 CYL.	6 CYL.	8 CYL.	4 CYL.	6 CYL.	8 CYL.
SPARKS/REV.	4	6	8	2	3	4
SPARKS/SEC. AT 600 RPM	40	60	80	20	30	40
TIME/SPARK AT 600 RPM	25 MS	16.7	12.5	50	33.3	25
SPARK/SEC. AT 6000 RPM	400	600	800	200	300	400
TIME/SPARK AT 6000 RPM	2.5 MS	1.67	1.25	5.0	3.33	2.5
CAMSHAFT SPEED TO CRANKSHAFT SPEED	EQUAL	EQUAL	EQUAL	HALF	HALF	HALF
CAM DEGREES/SPARK	90°	60°	45°	90°	60°	45°
CRANK DEGREES/SPARK	90°	60°	45°	180°	120°	90°

ULTRA-LINEAR HIGH PRECISION TACHOMETER

(For Automotive Type Ignition Systems with 12 Volt Negative Ground)

Figure 15.11

AUDIBLE AUTO SIGNAL MINDER

(Not Adaptable to 6.0 Volt Operation)

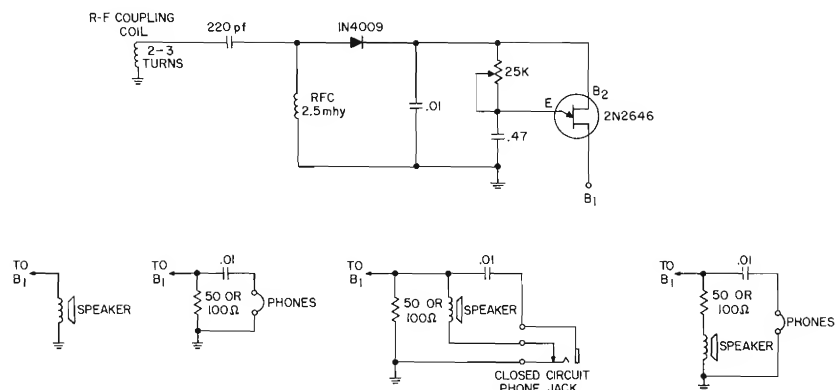
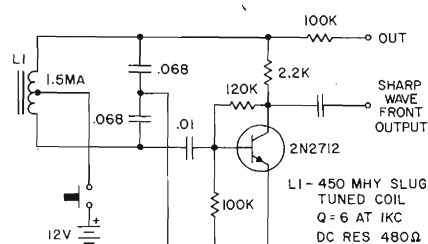
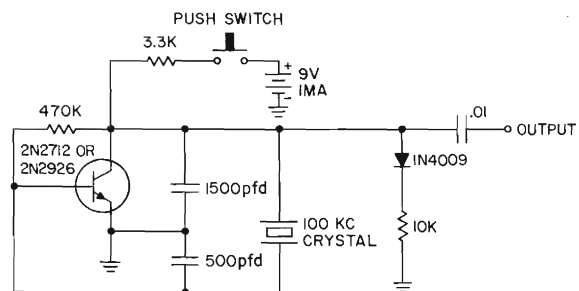
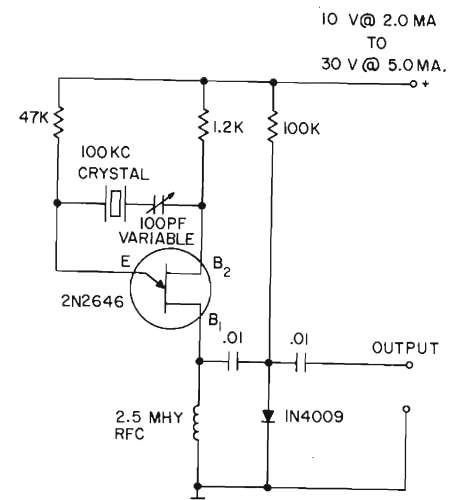
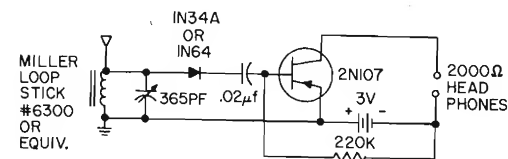
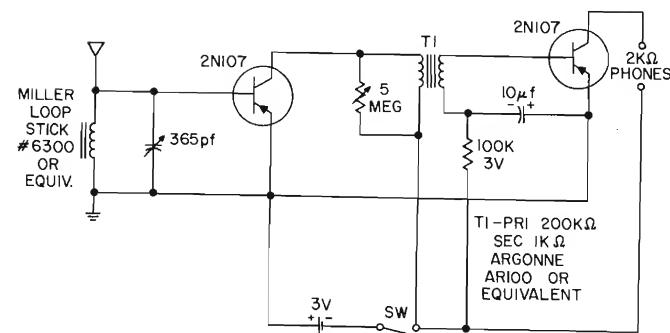



Figure 15.12

UNIJUNCTION CW MONITOR
Figure 15.13

1 KC OSCILLATOR
Figure 15.14

100 KC CRYSTAL STANDARD
Figure 15.15

UNIJUNCTION 100 KC CRYSTAL STANDARD
Figure 15.16

ONE TRANSISTOR RECEIVER
(AM Broadcast Band)
Figure 15.17

TWO TRANSISTOR RECEIVER
(AM Broadcast Band)
Figure 15.18

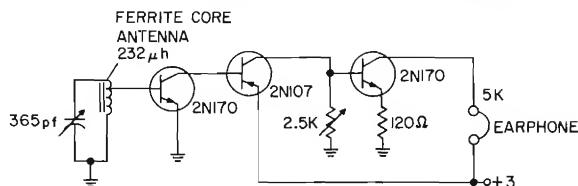
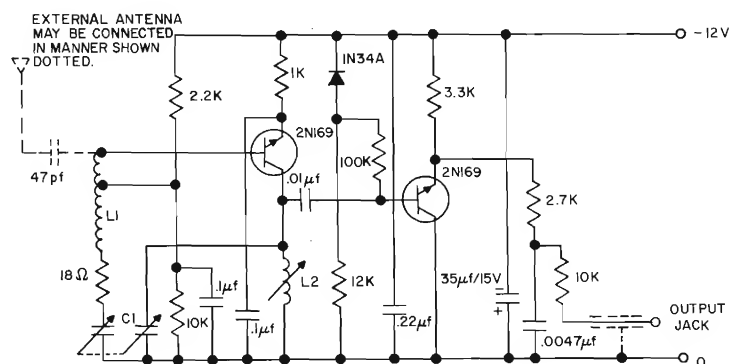
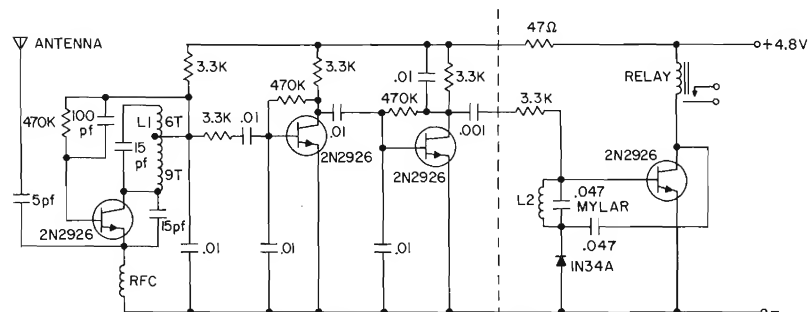



Figure 15.19 THREE TRANSISTOR RECEIVER (AM Broadcast Band)

C1 – 2 GANG CAPACITOR BOTH SECTIONS 10pf-365pf MILLER CAT. NO. 2112, OR EQUIVALENT

L1 – LOOPSTICK MILLER CAT. NO. 2000, OR EQUIVALENT

L2 – ADJUSTABLE 220μH-275μH MILLER PART NO. 42A224 CBI, OR EQUIVALENT

Figure 15.20 AM BROADCAST BAND TUNER

L1 - 15 TURNS #24 AWG TAPPED AT 6 TURNS, PROPORTIONED AS SHOWN 6 TURNS/9 TURNS ON CTC #SPC11-4L (CAMBRIDGE THERMIONICS CORPORATION)

L2 - 180 TURNS AWG ON FERROXCUBE 1408-FID BOBBIN, IN 1408-P100-3B5 CUPCORE, HELD BY 1408 BRACKET ASSEMBLY. (FERROXCUBE CORPORATION OF AMERICA, SAUGERTIES, NEW YORK)

RELAY - OMEGA SALES HR300 REED RELAY

RFC - 22μHENRY DELAVAN TYPE #1537-44 (DELAVAN ELECTRIC CORPORATION, 270 QUAKER ROAD, EAST AURORA, NEW YORK)

SUPERREGENERATIVE 27 MC RECEIVER

Figure 15.21

AUDIO

DEMODULATOR

LIMITER

2ND I.F. AMPLIFIER 200KC/S CENTER FREQUENCY

1ST I.F. AMPLIFIER 200KC/S CENTER FREQUENCY

CONVERTER OSCILLATES AT ONE-HALF SIGNAL FREQUENCY

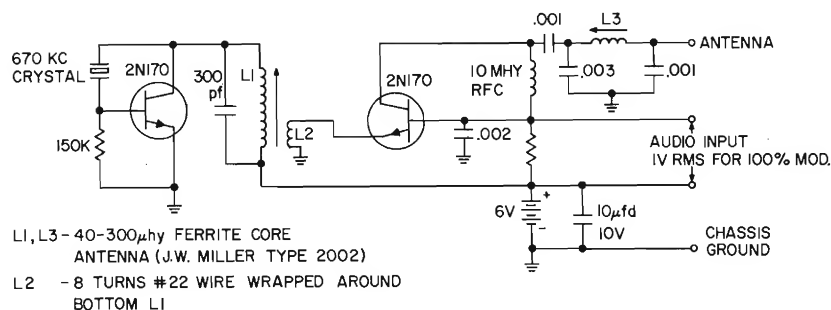
POWER-SUPPLY—12 VOLTS

NOTE: DOTTED LINES INDICATE SUGGESTED MODULAR BREAKDOWN
L1 – 4 TURNS #18 3/8" I.D., APPROX. 1/2" LONG
L2 – 4 TURNS #18 3/8" I.D., APPROX. 1/2" LONG
(L1 & L2 COUPLED END TO END, SPACED APPROX. 1/8")
L3 – 8 1/2 TURNS #18 3/8" I.D. CENTER TAPPED, APPROX. 3/4" LONG

FM BROADCAST BAND TUNER
(88 to 108 MC)
Figure 15.22

L1, L3 - 40-300μhy FERRITE CORE ANTENNA (J.W. MILLER TYPE 2002)

L2 - 8 TURNS #22 WIRE WRAPPED AROUND BOTTOM L1

Courtesy *Electronics World*

LOW POWER AM BROADCAST BAND TRANSMITTER
(670 Kc Crystal Controlled—400 Microwatts)

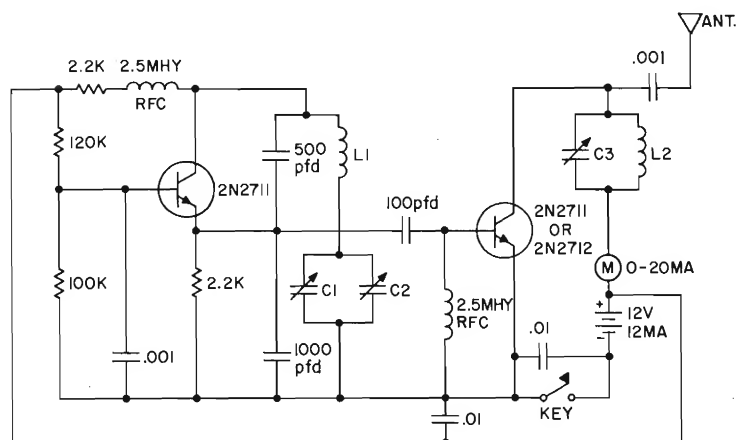
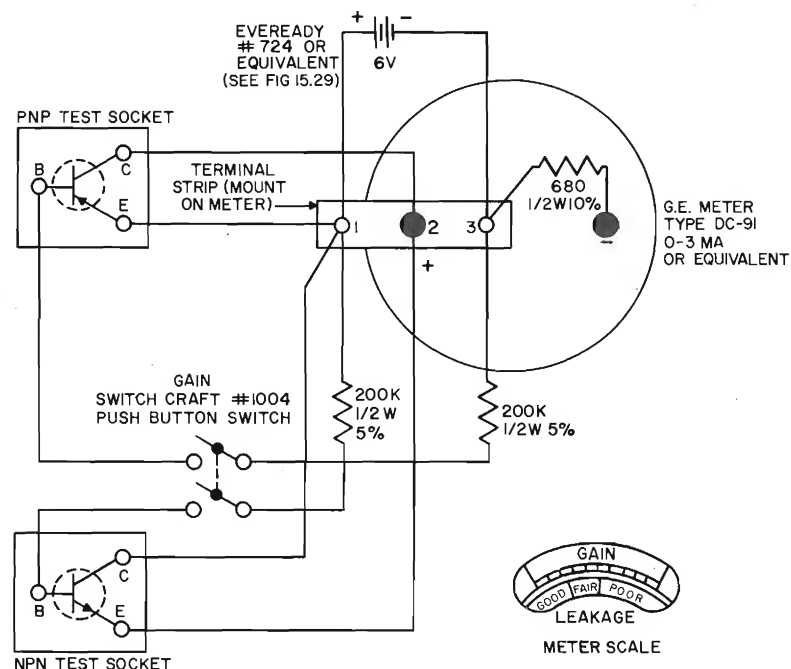



Figure 15.23

C1 5-15pf BANDSPREAD VARIABLE
C2 5-55pf BANDSET VARIABLE
C3 6-80pf FINAL TUNING VARIABLE

L1 57T, L2 35T — B & W NO. 3016 MINI-DUCTOR COILS 1" DIA 32T/INCH

LOW POWER VFO CW TRANSMITTER
(80 Meter Amateur Band—100 Milliwatts)

Figure 15.24

INSTRUCTIONS FOR TRANSISTOR TEST SET

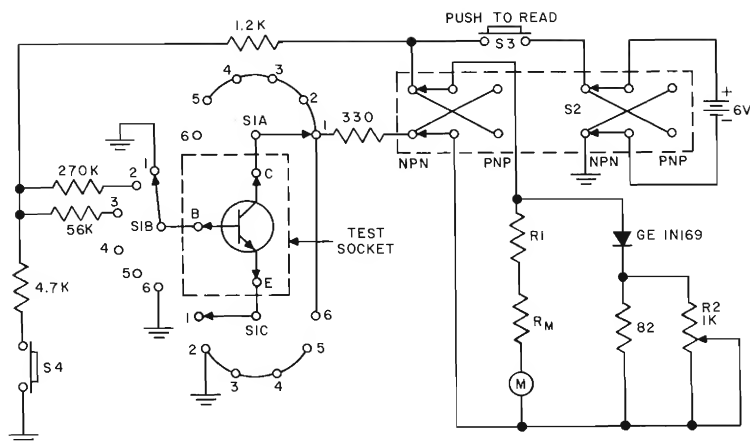
BATTERY CHECK: INSERT 560 OHM RESISTOR BETWEEN E AND C (EITHER SOCKET). IF METER DOES NOT READ FULL SCALE, REPLACE BATTERY (EVEREADY TYPE 724 OR EQUIVALENT)

LEAKAGE TEST: INSERT TRANSISTOR IN APPROPRIATE SOCKET. METER READING INDICATES CONDITION WITH RESPECT TO LEAKAGE.

GAIN TEST: DEPRESS GAIN BUTTON AND NOTE INCREASE IN METER DEFLECTION. AN INCREASED DEFLECTION TO THE RIGHT EQUAL TO AT LEAST ONE DIVISION ON THE GAIN SCALE COMPARED TO THE DEFLECTION DURING LEAKAGE TEST INDICATES ACCEPTABLE CURRENT GAIN.

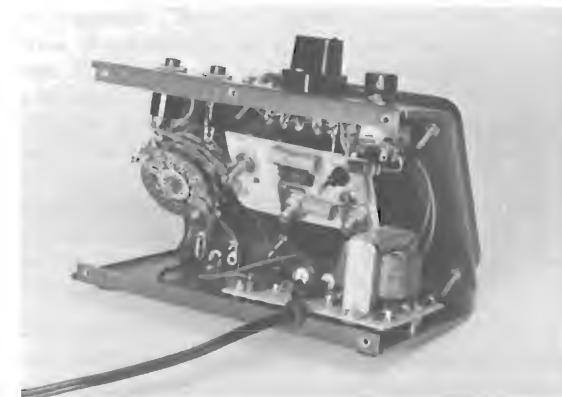
OPENS AND SHORTS TEST: A SHORTED TRANSISTOR WILL BE INDICATED BY A FULL SCALE METER DEFLECTION IN LEAKAGE TEST. AN OPEN TRANSISTOR WILL BE INDICATED BY NO METER DEFLECTION IN BOTH LEAKAGE AND GAIN TESTS.

TRANSISTOR TEST SET

Figure 15.25

PARTS
S1-3 POLE 6 POSITION NON-SHORTING SELECTOR SWITCH
S2-4 POLE 2 POSITION SWITCH
S3-S4 NORMALLY OPEN PUSH SWITCHES
M-100μA FULL SCALE METER
R_M-METER S INTERNAL RESISTANCE

TO TEST	WHEN	ADJUST SELECTOR SWITCH S1 TO POSITION	RESULT
I_{CO}	$V_{CB} = 6V$	1	READ METER DIRECT
I_C	$I_B = 20\mu A$	2	READ METER DIRECT
I_C	$I_B = 100\mu A$	3	READ METER DIRECT
I_{CEO}	$V_{CE} = 6V$	4	READ METER DIRECT
I_{CES}	$V_{CE} = 6V$	5	READ METER DIRECT
I_{EO}	$V_{EO} = 6V$	6	READ METER DIRECT
h_{FE}	$I_B = 20\mu A$	2	CALCULATE: $h_{FE} = \frac{I_C}{I_B} = \frac{\text{METER READING}}{20\mu A}$
h_{FE}	$I_B = 100\mu A$	3	CALCULATE: $h_{FE} = \frac{I_C}{I_B} = \frac{\text{METER READING}}{100\mu A}$
h_{fe}	$I_B = 20\mu A$	2	CALCULATE: $h_{fe} = \frac{I_{C1} - I_{C2}}{4 \times 10^{-6}}$ WHERE: I_{C1} = METER READING; I_{C2} = METER READING WITH S_4 CLOSED
h_{fe}	$I_B = 100\mu A$	3	CALCULATE $h_{fe} = \frac{I_{C1} - I_{C2}}{20 \times 10^{-6}}$
6V. BATTERY	——	4	WITH 150Ω RESISTOR CONNECTED TO C-E OF TEST SOCKET, FULL-SCALE METER DEFLECTION WILL RESULT WHEN S3 IS PRESSED.

TRANSISTOR TESTER
Figure 15.26

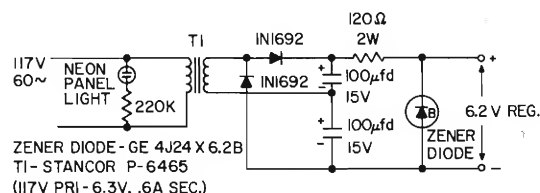
TRANSISTOR TESTER SHOWING READOUT CHART
Figure 15.27

INTERNAL VIEW OF TRANSISTOR TESTER
Figure 15.28

The 100 μa meter is in a network which results in a nearly linear scale to 20μa, a highly compressed scale from 20 μa to 1 ma and a nearly linear scale to full scale at 10 ma as shown in the photograph. The network permits reading I_{CO}, I_{EO}, I_{CES}, and I_{CEO} to within 10% on all transistors from mesas to power alloys without switching meter ranges or danger to the meter movement.

By making $R_M + R1$ equal to 12K the scale will be compressed only 1 μa at 20 μa. Potentiometer R2 should be adjusted to give 10 ma full scale deflection. The scale can then be calibrated by comparison with a standard conventional meter. By placing selector switch in position 4 and connecting a second meter and a decade box in series with C-E of test socket both meters will track.

If the NPN-PNP switch is in the wrong position, the collector and emitter junctions will be forward biased during the I_{CO} and I_{EO} tests respectively. The high resulting current can be used as a check for open or intermittent connections within the transistor.

The test set also measures h_{FE} with 20 μa and 100 μa base current. Depressing the h_{fe} button decreases the base drive 20% permitting h_{fe} to be estimated from the corresponding change in collector current. The tests are done with a 330 ohm resistor limiting the collector current to approximately 12 ma and maximum transistor dissipation to approximately 20 mw. Therefore, this test set can not harm a transistor regardless of how it is plugged in or how the switches are set.

"Battery test" has been designed to give full scale meter deflection of 10 ma when the battery voltage is 6 volts. This is achieved by connecting 150 ohms from **C** to **E** of the test socket. This test assumes precision resistors.

REGULATED POWER SUPPLY
(For Use With Fig. 15.25 & Fig. 15.26 Testers)
Figure 15.29

NOTES

SILICON CONTROLLED SWITCHES

CHAPTER 16

Part 1 — Understanding PNPN Devices

INTRODUCTION

The silicon controlled switch, SCS, is a PNPN structure with all four semiconductor regions accessible, rather than only three as is customary with silicon controlled rectifiers (SCR).* Accessibility of the fourth region greatly expands circuit possibilities beyond those of conventional transistors or SCR's.

In fact, the wide usage of the SCS since its introduction two years ago has warranted the development and introduction of new types based on planar technology. The reasons for its wide acceptance are varied.

To some, it is an integrated circuit consisting of a PNP and an NPN transistor in a positive feedback configuration. As such, it offers fewer connections, few parts, lower cost, and better characterization than is available from two separate transistors. To others it is an SCR with an "extra lead" by which they can completely eliminate *rate effect* problems. Some prefer to use it as a complementary SCR being triggered by negative going pulses. Many find the high triggering sensitivity ideal for timing and level sensing applications. By viewing the SCS as a transistor with an additional "latching" junction, some have developed very useful bistable circuits with high turn-on and turn-off gains.

Underlying these technical values are the inherent high temperature capabilities of silicon, the ruggedness and reliability of a design for military usage, and the low cost due to existing high volume transistor facilities which proved readily adaptable to SCS manufacture.

This chapter cannot cover fully the wealth of device and application data available. Instead it endeavors to give the circuit designer a "feel" for the SCS so that he can quickly design and evaluate circuits. To this end the construction techniques and the characteristics resulting from them will be discussed. Qualitative equivalent circuits will be derived from several points of view. Circuits for measuring SCS characteristics will be suggested. "Rules of thumb" to speed circuit design are included, but detailed device characteristics are not included since these are found on the specification sheets. Finally, groups of circuit configurations are shown to illustrate how the SCS can be used.

For a device to be useful it must be understood. In turn, the more versatile a device is, the harder it is to thoroughly understand but the greater the rewards once the effort is made. As in the early days of transistors, PNPN devices are still primarily discussed in terms of mathematical models to advance device design. These, however, do not give a circuit designer an easy intuitive familiarity with the device that he needs. The following discussion derives PNPN characteristics from currently well-understood transistor behavior.

THE EQUIVALENT CIRCUIT

Converting the PNPN into familiar equivalent circuits aids in understanding it.

Figure 16.1 shows a variety of symbols and equivalent circuits appropriate to PNPN's. The basic structure in Figure 16.1(A) can be considered an NPN transistor with a diode in series with the collector as shown in Figure 16.1(B). By grouping the

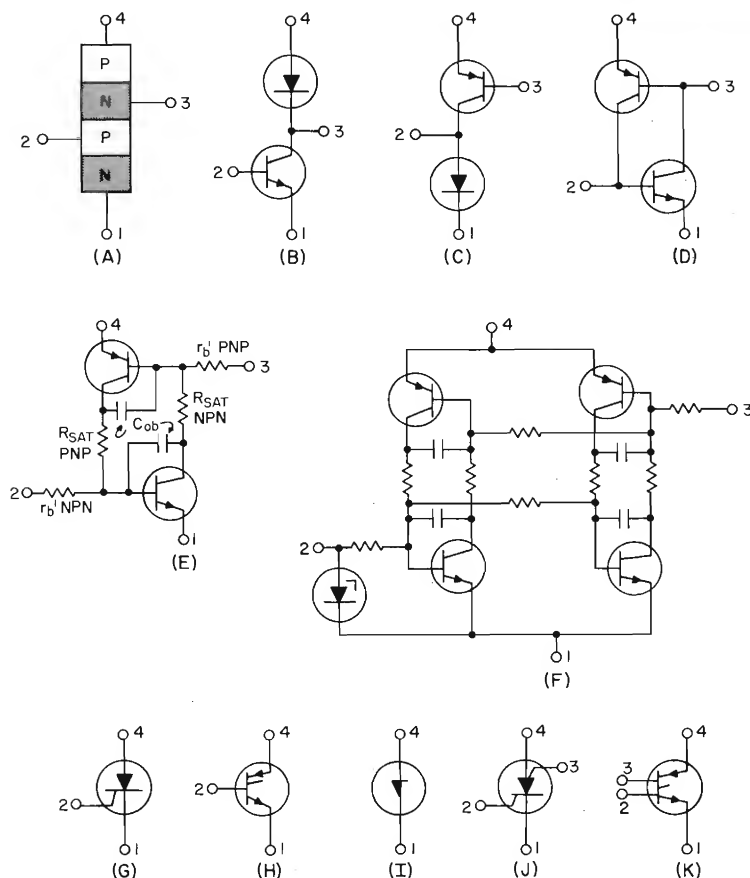
*See Reference 4 at end of Chapter 1.

SYMBOLS AND EQUIVALENT CIRCUITS

Figure 16.1

top three regions together the device resembles a PNP transistor with a series diode as shown in Figure 16.1(C). Neither of the circuits suggests the *regeneration* inherent in a PNPN, and thus the two transistor circuit as shown in Figure 16.1(D) is a more accurate representation. To these transistors we can add the R_{sat}, r_b' and C_{ob} parasitics, Figure 16.1(E), which are inherent in all semiconductors. This circuit in turn leads to a distributed circuit of several transistor pairs joined by the *sheet resistance* of each semiconductor layer. While this final complex circuit is most versatile, it generally can be avoided. The common SCR symbols in Figures 16.1(G) and 16.1(H) ignore the central N-region; the Shockley diode in Figure 16.1(I) has leads to the outside regions only; while the silicon controlled switch in Figures 16.1(J) and 16.1(K) has leads to all four regions. The best choice of equivalent circuit depends on the specific parameters of interest and the geometry of the device.

PNPN GEOMETRY

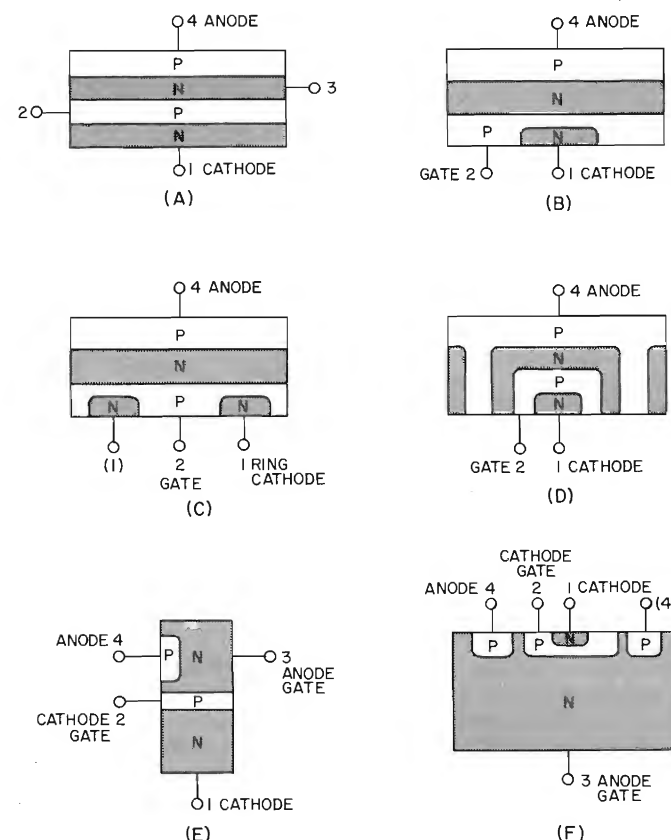
The details of the PNPN geometry determine which elements of an equivalent circuit are significant. The sectional view in Figure 16.2(A) leaves little area for

SECTIONAL VIEWS OF PNPN GEOMETRIES

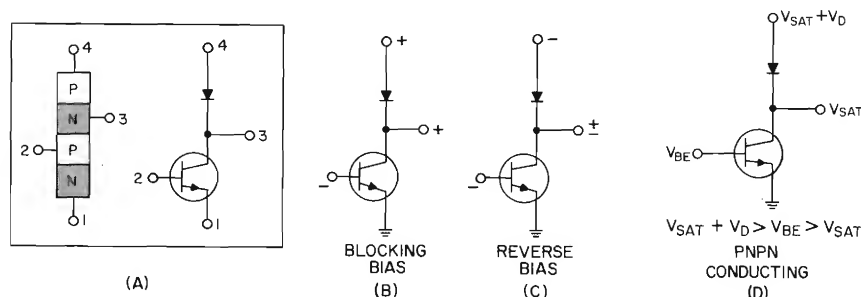
Figure 16.2

connections to the central junctions, therefore is only suitable for a four layer diode. Its equivalent circuits can ignore r_b' but must include C_{ob} and the collector breakdown voltage since the latter two determine the maximum blocking voltage under transient and dc conditions, respectively. Figures 16.2(B) and 16.2(C) show common SCR structures which add an N-region to a PNP transistor. The gate lead can be attached at one side (Figure 16.2(B)) or in a hole at the center of the N-region (Figure 16.2(C)).

A planar SCR version is shown in Figure 16.2(D). The anode region can be brought out to the surface along with the other regions by a number of different processes. The silicon controlled switch series 3N58, 3N59, and 3N60 has the structure as shown in Figure 16.2(E). It is basically an NPN transistor to which has been added an additional P-junction so located that a PNP transistor is formed. A new planar SCS structure is shown in Figure 16.2(F). It is also basically an NPN transistor surrounded by a P diffused ring to form a PNP transistor across the surface. Since the P-base and P ring-anode can be diffused simultaneously this structure is no more difficult or costly to manufacture than a planar transistor. Yet it makes all four layers readily accessible to leads and concentrates the current near the surface where cooling by radiation is optimum, while enjoying the parameter stability inherent in oxide

passivated planar structures. As can be expected, such varied geometries yield equivalent circuits which quantitatively are quite different.

BIASING VOLTAGES

The simplest equivalent circuit, shown in Figures 16.1(B) and 16.3(A) shows how the biases on all regions are interrelated.

PNPN BIASING
Figure 16.3

To start with, NPN transistor action can only occur if the collector is positive with respect to the emitter. This is illustrated in Figure 16.3(B). Referring to Figure 16.3(A), if current is to flow through the anode (4), it in turn must be positive with respect to the collector. When the anode is returned to a positive voltage, collector current is controlled by the base (2). Reverse biasing the emitter junction keeps the transistor cut off. The voltage across the PNPN is sustained across the collector-to-base junction. This description shows that the center junction breakdown determines the maximum blocking voltage, which is defined as the maximum permissible positive anode voltage. Generally the emitter junction has a low voltage breakdown to enhance emitter efficiency and therefore beta. If the anode is returned to a negative voltage the diode becomes reverse biased and the transistor's emitter and collector interchange roles (Figure 16.3(C)). The maximum reverse voltage, i.e. the maximum negative anode voltage that can be applied is limited to the diode breakdown voltage plus the breakdown voltage of the inverted transistor. The latter is the transistor's emitter breakdown voltage. The common manufacturing processes result in the collector and diode breakdowns being equal and in the emitter breakdown being much lower. Therefore PNPN specifications show equal blocking and reverse ratings.

This equivalent circuit provides further insight. If the emitter junction is reverse biased the collector, or anode, cannot conduct as long as the collector junction breakdown is not exceeded. In lieu of reverse biasing, the base can also be left disconnected or connected to the emitter through a resistor or a short. This leads to lower collector breakdown corresponding to BV_{CEO}, BV_{CER}, and BV_{CES}, respectively.

To turn the PNPN *on* the base is forward biased, the base current increasing about ten fold for each 0.1 volt increase in base voltage. This is true until regeneration occurs as will be shown later. Once the PNPN is on, it is seen that the collector and anode differ in potential only by the diode forward voltage.

The above discussion, based on the equivalent circuit of Figure 16.1(B), applies equally well to the circuit of Figure 16.1(C) if polarities appropriate to the PNP

transistor are substituted. In this case, however, the PNP emitter breakdown is equal to the collector breakdown while the diode breakdown is less than 15 volts. This results in the blocking voltage being substantially higher than the reverse voltage.

BASIC TWO TRANSISTOR EQUIVALENT CIRCUIT

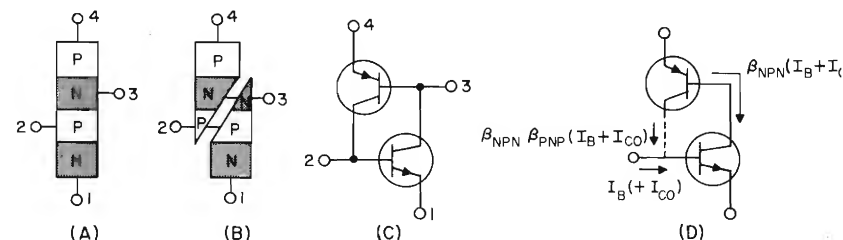
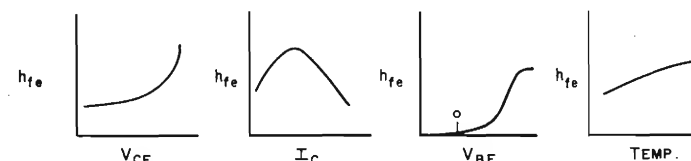
PNPN devices designed for very high holding currents or for gate turn-off resemble the transistor-diode circuit in Figure 16.3(B) at low currents. In general, however, the PNPN is important because it behaves like two complementary transistors in a regenerative feedback configuration.

TWO TRANSISTOR EQUIVALENT CIRCUIT OF PNPN
Figure 16.4

Figure 16.4 shows how the two transistor circuit is derived. The diode in Figure 16.3 is now the emitter junction of the PNP transistor. Base current into the NPN is multiplied by the NPN beta and becomes base current for the PNP. After being multiplied by the PNP beta it reinforces the initial NPN base current. If the reinforcing current exceeds the initial base current, i.e. if $(\beta_{NPN})\ (\beta_{PNP}) \geq 1$ the currents build up regeneratively driving both transistors into saturation. Therefore the product $(\beta_{NPN})\ (\beta_{PNP})$ is the critical factor which determines if the PNPN will switch on.

To keep the PNPN non-conducting the betas must be kept sufficiently low so that $(\beta_{NPN})\ (\beta_{PNP}) < 1$. To do this it is necessary to realize that beta (h_{fe}) is a function of V_{CE}, I_C, V_{BE}, and temperature as shown in Figure 16.5. These parameters will be analyzed in detail in the next few paragraphs.

PARAMETERS CONTROLLING h_{fe}
Figure 16.5

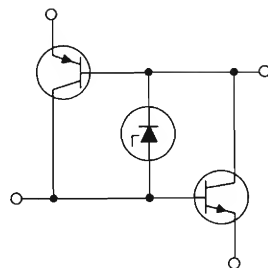
Beta increases as the collector junction breakdown voltage is approached, in turn causing the collector current to increase. Therefore, raising the anode near the collector breakdown voltage can trigger the device. Figure 16.6 shows a suitable equivalent circuit.

EQUIVALENT CIRCUIT OF PNPN TRIGGERED BY COLLECTOR BREAKDOWN
Figure 16.6

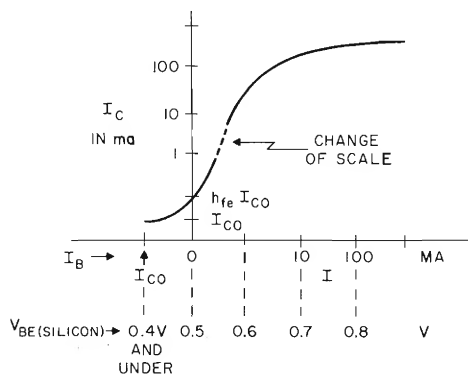
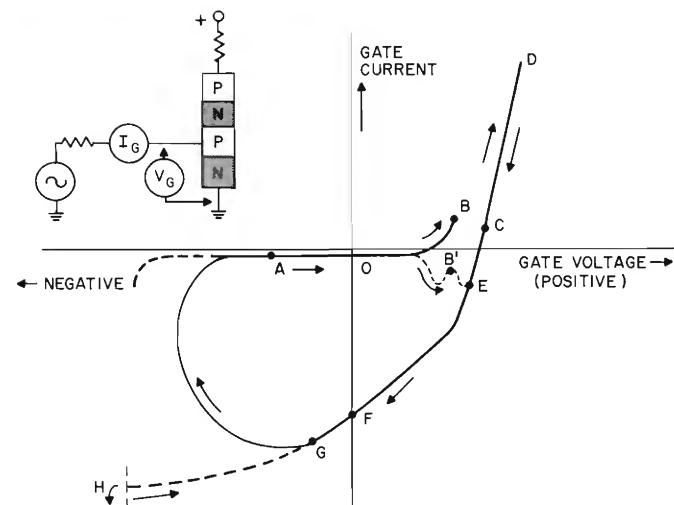
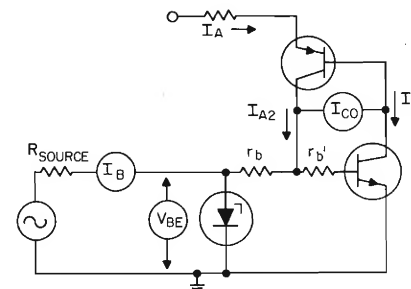
Figure 16.7 plots I_C as a function of I_B, V_{BE}, and I_C for a typical silicon transistor. When the base is reverse biased I_B is very nearly I_{CO}. When open circuited the base will float at a potential of about 0.5 volt and the collector current will rise as I_{CO} takes on the role of base current. The slope of the curve, by definition h_{fe}, continues to increase until reduced emitter efficiency reverses it.

COLLECTOR CURRENT VS. I_B, V_{BE} AND I_{CO}
Figure 16.7

Figure 16.7 shows that reverse biasing the base, or at least keeping it below 0.4 volt makes the base current very nearly I_{CO}, and h_{fe} very nearly zero ensuring that $(\beta_{NPN})(\beta_{PNP}) < 1$. With the base forward biased between 0.4 and 0.5 volts, beta may increase sufficiently to cause triggering. Since leakage current flows out of the base, this would be defined as triggering with a negative input current. If triggering occurred at 0.5 volts, this corresponds to zero input current. Generally, specifications will show the maximum forward current required to trigger.

The above discussion ignores the interaction between the two transistors, the presence of parasitic resistors, and the impedance of the measuring instruments. Figure 16.8 shows a typical curve tracer plot at the cathode gate of a PNPN as an ac voltage is applied to it. Starting at point A the device is blocking and I_{CO} is being diverted by the base. As the base becomes forward biased, base current may increase as would be expected for a normal transistor. The device triggers on when point B is

CATHODE GATE (NPN BASE) CHARACTERISTICS
Figure 16.8

reached. Immediately the base voltage jumps to point C and traces out curve C D E F G. From E to F current is being pulled out of the base tending to turn off the device. If the anode current is low enough, the device turns off at point G, rapidly returning to point A to complete the cycle.

If the curve tracer source impedance is low, it acts as a shunt for the feedback current from the PNP collector. This permits the loop gain to approach unity very closely yet not trigger the PNPN. This is illustrated by the negative current leading to B′, where switching occurs. The point B′ may lie above or below the axis for different devices.

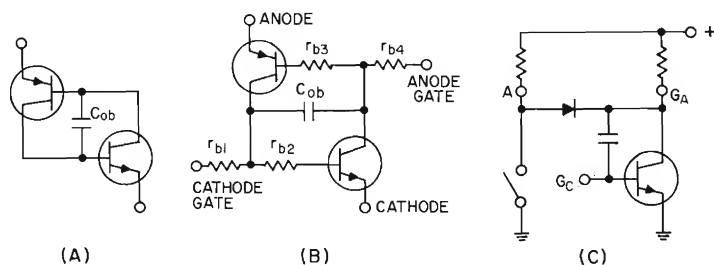
If the anode current is too large to be turned off by the base (i.e. the gate) the base is driven negative to H where it is clamped by the emitter junction zener breakdown. Curve H G E D will continue to be retraced until the device is turned off when the cycle can begin at A again.

CATHODE GATE EQUIVALENT CIRCUIT
Figure 16.9

This locus can be interpreted using the equivalent circuit of Figure 16.9. The base resistance is shown in two portions to better represent its distributed nature. The zener represents the emitter junction breakdown voltage. At point A of Figure 16.8, I_B is only I_{CO} as the zener and NPN transistor are both cut off and PNP beta is generally very low. At point B the product of betas results in triggering. The load current I_A now divides into I_{A1} and I_{A2}. I_{A2} causes the base voltage to increase to C. The amplitude of the jump is proportional to I_A. V_{BE} continues to rise to D as the ac source supplies more current. Since the base resistance is modulated downward when the PNPN is on, r_b and r_b' decrease as current is increased.

As the ac source drops in voltage, I_{A2} is partially diverted into the source via r_b in the region E to F of Figure 16.8. In this case r_b is modulated upward becoming a much higher impedance. At G enough of I_{A2} has been diverted that the NPN transistor cannot stay in saturation and turn-off begins. It is obvious that if the device did not turn off the zener clamps the negative excursion of the base with r_b determining the maximum base current.

Now if R source is zero and r_b is also low it is seen that the shunting effect on the feedback current is much greater resulting in the locus to B .

Qualitatively the same curves are seen when the triggering input is to the base of the PNP. Since r_b and r_b' are much lower the jump from B to C is smaller. Since the PNP emitter breakdown voltage is much higher than the NPN emitter breakdown, much higher anode currents can be turned off.

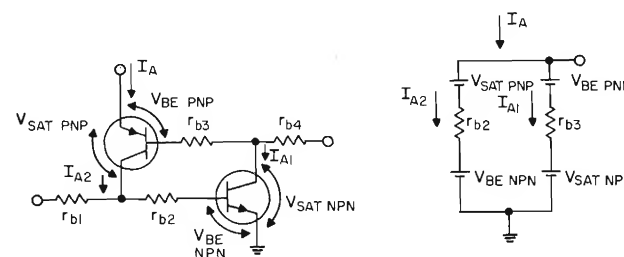
RATE EFFECT

RATE EFFECT EQUIVALENT CIRCUIT
Figure 16.10

PNPN devices may be triggered on if anode voltage is applied suddenly or if they are subjected to high frequency transients. This phenomenon, called *rate effect*, is readily explained by the equivalent circuit of Figure 16.10. Figure 16.6 shows how the zener breakdown of the center junction supplies the base currents necessary to trigger the PNPN. For high frequencies, the C_{ob} capacitance of Figure 16.10(A) is a low impedance resulting in substantial base currents and triggering. The base currents are $I_B = C_{ob}\ dV/dt$ where V is the increasing anode voltage. The equivalent circuit in Figure 16.10(B) suggest ways of suppressing rate effect. By shorting the cathode gate to cathode r_{b1} diverts the C_{ob} charging current, preventing its forward biasing the NPN transistor. Similarly the anode gate can be shorted to the anode to advantage. If it is desired to maintain dc triggering sensitivity, the shorts may be capacitors. Reverse biasing a gate will only be effective if a low impedance bias source is used. Again, a capacitor can be used to generate the low impedance.

A far more elegant solution is shown in Figure 16.10(C). While the anode is reverse biased (the switch closed) C_{ob} charges up via the collector resistor. The switch may now be opened as rapidly as desired.

It is obvious that if a highly rate sensitive device is required, for example, for detecting transients, the addition of an interbase capacitor creates one by effectively increasing C_{ob}. Appropriate circuitry for minimizing rate effect is shown in Figure 16.20.

FORWARD CONDUCTING VOLTAGE

The anode-to-cathode voltage during conduction, i.e. the forward voltage, can be evaluated using the equivalent circuit of Figure 16.11. The resistors r_{b2} and r_{b3} can be considered as base or collector resistors, but since they carry minor carriers they are strongly modulated and are much lower in resistance than their doping level and geometry would predict. The currents I_{A1} and I_{A2} are determined by the transistor betas as well as by r_{b2} and r_{b3}.

FORWARD CONDUCTING VOLTAGE EQUIVALENT CIRCUIT
Figure 16.11

Forward voltage does not change much with temperature. At high temperatures the resistors increase while V_{SAT} and V_{BE} decrease. At low temperatures the resistors decrease while V_{SAT} and V_{BE} increase to compensate.

HOLDING CURRENT AND VALLEY POINT

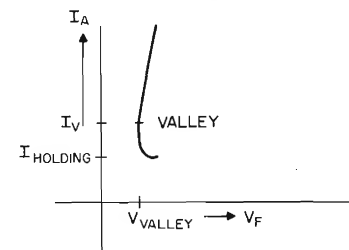
As I_A is reduced the transistors are forced to operate in their low current, low beta region. Eventually the betas become so low that $(\beta_{NPN})\ (\beta_{PNP}) < 1$ and the PNPN switches *off*.

HOLDING CURRENT AND VALLEY POINT
Figure 16.12

Figure 16.12 shows a typical forward characteristic. The devices start to turn off at the valley point i.e. where the forward voltage is lowest. But as the anode voltage rises, the transistors come out of saturation raising beta, and the PNPN remains conducting. At the holding current increasing voltage cannot raise beta enough and the device switches off. If the gates are left open in the equivalent circuit of Figure 16.11, loop gain is high; the valley current and holding current are very low and nearly equal. If, however, the cathode gate is shorted to the cathode, r_{b1} will divert part of I_{A2} lowering loop gain, and raising both the valley current and holding current. These currents now are separated considerably since the valley point is reached while the transistor betas are high. As a result of the high betas a slight change in anode voltage can change the ratio of I_{A1} to I_{A2} to sustain conduction.

It is important to differentiate between holding current and valley current. If the anode, while at the valley point, sees an ac short circuit load i.e., a capacitive load, the device will turn off. The reason for this is thoroughly developed for applications based on the unijunction* transistor and will not be discussed here. With a resistive load, however, the PNPN will conduct until the holding current is reached. Where the load characteristics are uncertain, the anode current should exceed the valley point current to assure conduction.

TRANSIENT RESPONSE TIME

Figure 16.4 indicates how an input base current is amplified by both transistors and fed back to the input. Each transistor introduces a delay which depends on its frequency response (f_α or f_T) and the input current. Once regeneration starts, however, the "input current" is only limited by the maximum anode current and the PNPN turns on rapidly.

Two limiting cases are of interest. If the input current is small, there is substantial delay followed by a rapid turn-on. With large inputs and low anode currents the NPN transistor can be driven into saturation before regeneration is fully established. The equivalent circuit resembles that in Figure 16.3(A).

RECOVERY TIME

The circuit in Figure 16.13(A) assumes the PNPN is turned *off* at the cathode

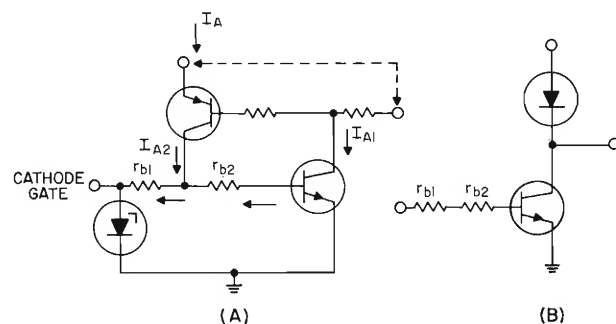



Figure 16.13 RECOVERY TIME EQUIVALENT CIRCUITS

gate. This is achieved by diverting all of I_{A2} and pulling current out of the NPN transistor base. Following the NPN storage and fall time the PNP is deprived of base drive and in turn stops conducting. To shorten recovery time it is seen that the

*See Chapter 13.

turn-off current should be as large as possible. By not overdriving the NPN prior to turn-off, storage-time can be shortened. In other words I_{A2} should be reduced or diverted. Returning r_{b1} to ground prior to turn-off partially diverts I_{A2}. An anode-to-anode gate short would also aid recovery by reducing I_{A2}.

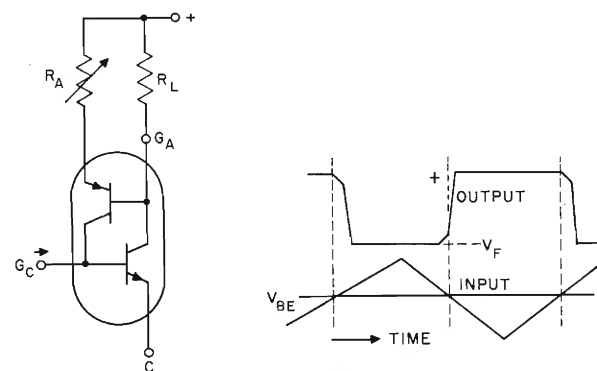
The turn-off input should be maintained until the anode rises to its maximum voltage, least the PNPN retrigger due to rate effect or residual charge in the PNP during its fall-time.

Turning off the PNPN by reverse biasing the anode requires the equivalent circuit of Figure 16.13(B). Rapidly reverse biasing the anode causes the anode junction to recover isolating the anode from the rest of the device which now behaves as an NPN transistor. If its base is open, eventually the base charge will recombine and the transistor turns off. Connecting r_{b1} to ground or a negative bias helps turn off the NPN more rapidly.

During recovery, there is a spike of anode reverse current while the anode junction recovers, after which the device appears to have recovered. However, once the anode rises above ground it will conduct again unless the NPN transistor has recovered. Therefore proof of recovery is the anode's ability to withstand full voltage.

BASIC CIRCUIT CONFIGURATIONS

CIRCUIT CONFIGURATIONS BASED ON NPN TRANSISTOR

Since the SCS is basically an NPN transistor with an anode junction added, circuit configurations based on its transistor characteristics can be developed. Figure 16.14 indicates that ignoring the anode makes the SCS a conventional NPN transistor. Current into the base (G_c) results in collector current through R_L. Connecting a large resistor from the supply to the anode allows regeneration which in effect raises the NPN beta.

SCS AS A VARIABLE GAIN TRANSISTOR
Figure 16.14

As the waveforms show, when the base is forward biased (above V_{BE}) the output current is β_{NPN} I_B. As soon as the anode-gate voltage drops anode current starts to increase beta as indicated by the steeper turn-on towards saturation. As the transistor begins to cut-off, the collector is not driven as hard into saturation, hence rises slightly before turning off completely. The amount of regeneration can be varied by changing the anode resistor. Variability from unit to unit and with temperature makes the

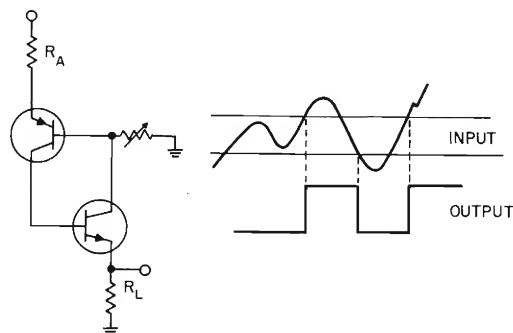
circuit more suitable for feedback applications such as AGC rather than for fixed gain amplifiers.

SCHMITT TRIGGER

Figure 16.15

The circuit in Figure 16.15 can be considered a PNP transistor operated common base, driving a common collector NPN. With the variable resistor shorted out only linear amplification occurs. As the resistor is increased regeneration makes the circuit perform as a Schmitt trigger. The 3N58 series SCS has sufficient built-in NPN saturation resistance to ensure regeneration.

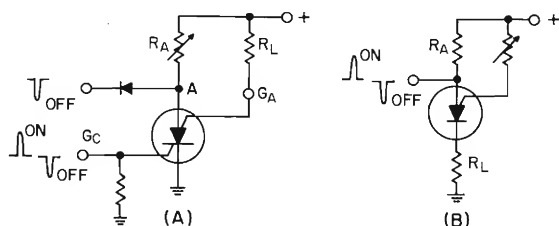
R_A in Figure 16.14 can be decreased sufficiently that although base drive is removed, the feedback via R_A is sufficient to keep the NPN transistor saturated. If the feedback is not excessive the PNPN can be turned off with a negative pulse at the base as shown in Figure 16.16(A). Alternately very little energy is required for turn-off from the anode. This is referred to as the *latching mode* of operation.

LATCHING MODE

Figure 16.16

Figure 16.16(B) shows a bistable circuit resulting from the Schmitt trigger of Figure 16.15 when regeneration is increased. The output is in phase with the input. The cathode gate may be left open for maximum sensitivity or connected to the cathode for faster recovery.

Decreasing R_A still further in Figure 16.14 prevents turn-off from the cathode gate. The PNPN can now be considered to have two parallel loads isolated by the anode junction diode. (Thus, for example, they may be returned to different voltages.) The PNPN is switched on and off just as a conventional SCR but the load R_L is not subjected to the switching transients.

Finally R_A may be used alone, and the SCS considered an SCR. In circuits operating from dc, however, rate effect is suppressed if the anode gate is returned to the supply voltage via a large resistor.

CIRCUIT CONFIGURATIONS USING HIGH TRIGGERING SENSITIVITY

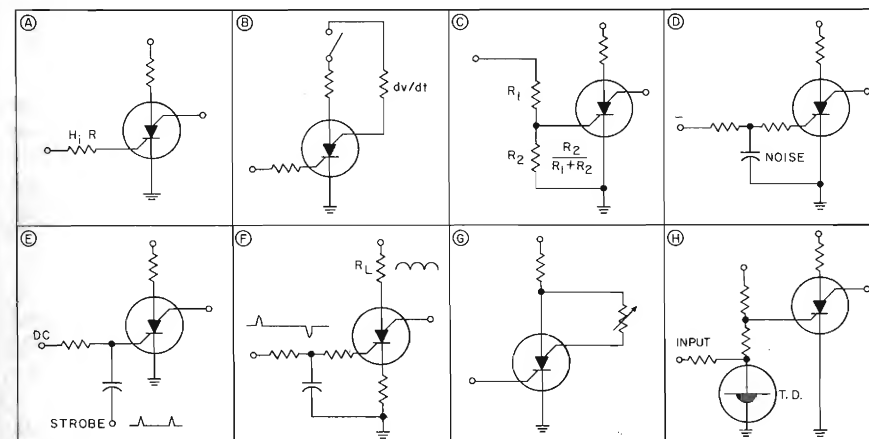
One of the unique features of the SCS is its high triggering sensitivity. This sensitivity can be used in many ways as suggested in Figure 16.17. At moderate temperatures where leakage current is not excessive sensitivity permits using high triggering source impedances with minimal loading as in Figure 16.17(A).

SENSITIVITY

Figure 16.17

If anode transients as in mechanical resetting give rise to rate effect, an anode gate resistor suppresses it as shown in Figure 16.17(B) but decreases gate sensitivity somewhat. High sensitivity initially, allows suppressing rate effect with ample sensitivity remaining.

Noise on the triggering input can be attenuated by a resistor divider as in Figure 16.17(C). If the noise is frequency sensitive a capacitor across R1 attenuates only low frequencies, while a capacitor across R2 attenuates high frequencies. High triggering sensitivity allows R1 and R2 to be large permitting the use of small inexpensive capacitors to shape frequency response. Figure 16.17(D) shows an alternate circuit for suppressing high frequency noise.

As the triggering point is approached, the PNPN becomes more sensitive to noise, temperature, or voltage transients. The circuit in Figure 16.17(E) avoids these problems if the sensed dc input is below ground. To the dc level a precise amplitude strobe pulse is added. The dc level determines whether the strobe pulse reaches the triggering voltage. This circuit offers a high input impedance over a wide temperature range.

Indicator lamps, solenoids, and relays represent a class of loads which will operate from ac to dc. Ac cannot be used with transistors and neither transistors nor SCR's exhibit latching without significant circuit complexity. In Figure 16.17(F) a positive pulse triggers the SCS on. The emitter resistor raises both the cathode and cathode

gate potentials. This causes the capacitor to charge by current out of the cathode gate. As the full wave rectified ac anode supply drops to zero the SCS turns off and the capacitor discharges into the cathode gate. While the discharge current is still in excess of the triggering current the anode voltage rises retriggering the SCS for the next half cycle. Therefore, once the SCS is triggered on, it continues to retrigger itself. To turn off the SCS a negative input pulse is used to discharge the capacitor breaking the retriggering cycle. If desired the cathode resistor may be the load, eliminating one component.

By adjusting the anode to anode-gate resistance as shown in Figure 16.17(G) it is possible to set the cathode gate triggering current to a precise value. Since triggering current is temperature sensitive this factor should be taken into consideration. Once the SCS triggers, its temperature rises due to increased dissipation. This in turn reduces the triggering current. In feedback control systems this phenomenon results in a built-in hysteresis that eliminates erratic triggering.

While the triggering voltage level can be used as a threshold detector better precision is possible with tunnel diodes. The SCS is useful in amplifying the low level output as shown in Figure 16.17(H). The anode waveform can be used to reset the tunnel diode if desired. If large anode currents are required ac coupling from the tunnel diode will prevent leakage current from changing the tunnel diode threshold.

THRESHOLD CIRCUITS

A variety of threshold circuits are feasible offering a wide range of characteristics. Positive or negative inputs can be sensed, with either polarity output. In Figure 16.18(A) the SCS triggers on when the anode voltage rises above approximately VR1/R1 + R2. The threshold can be set by the resistors anywhere within the breakover voltage rating. Since this SCS circuit resembles the unijunction transistor a capacitor from anode to ground generates large positive pulses across the cathode resistor.

If the anode is ignored for a moment, the rather similar circuit in Figure 16.18(B) is really a bias stabilized NPN transistor. When the anode voltage exceeds the stabilized collector voltage the transistor saturates. The voltage divider of Figure 16.18(A) may be replaced by a single resistor as in Figure 16.18(C) if an appropriate supply voltage is available. The anode rising above +V triggers the SCS. Note that a resistor must be used in series with the anode gate.

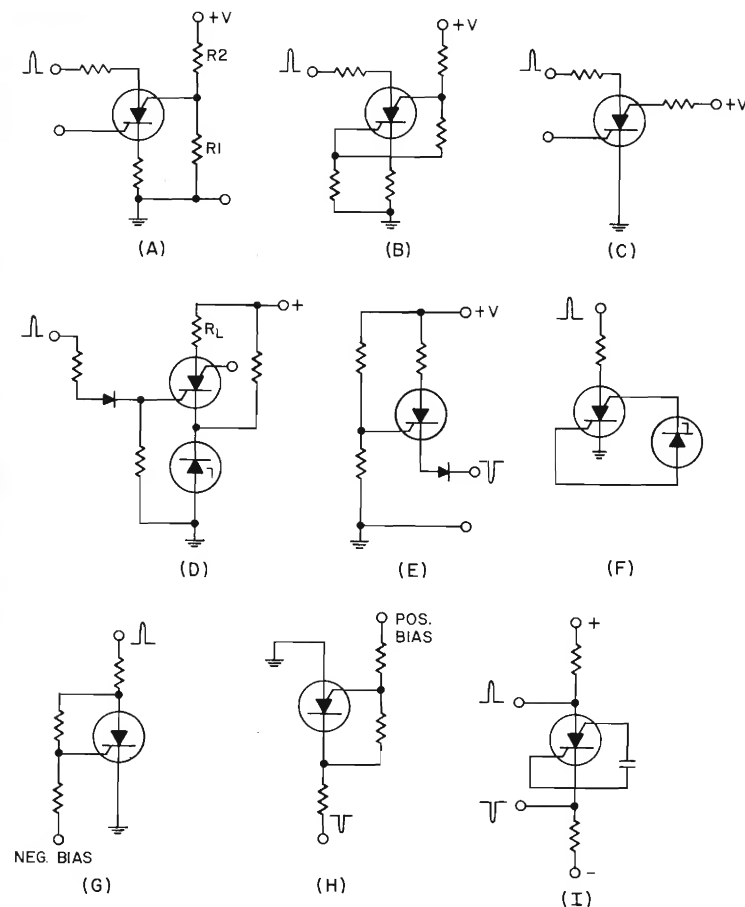
In some applications it may be preferable to apply the input to the cathode gate as in Figure 16.18(D). The zener diode sets the threshold voltage, the diode protecting the gate from excessive current while the input is near ground. The gate resistor is for diverting leakage.

To trigger on a negative waveform the circuit in Figure 16.18(E) can be used. Unless the maximum cathode waveform voltage does not exceed the cathode to gate breakdown the diode is necessary to avoid loading the input.

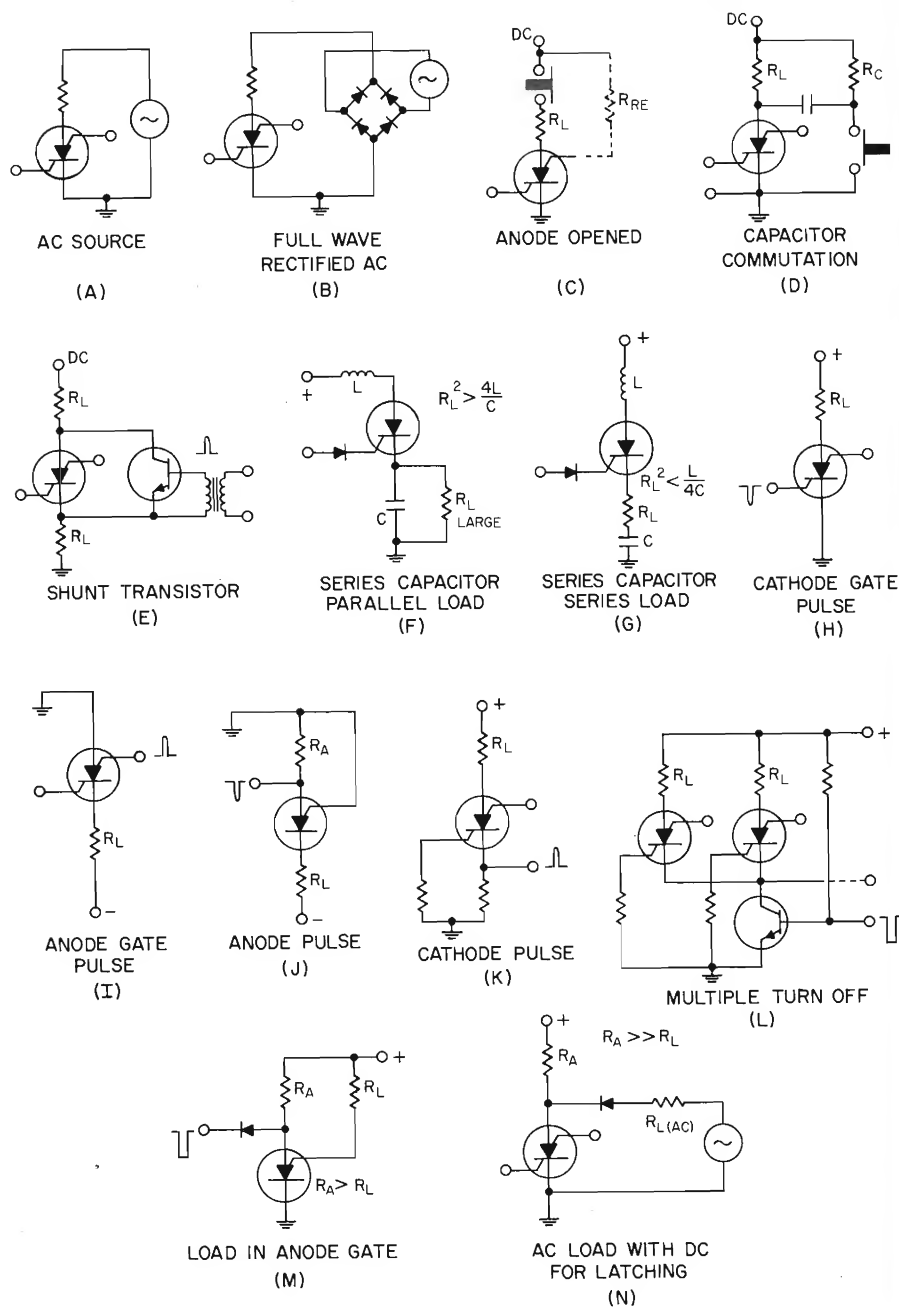
Where "two terminal" threshold devices are required the circuit in Figure 16.18(F) breaks over just above the zener voltage. The zener may also be connected from anode gate to cathode or cathode gate to anode, thus freeing one gate for control of sensitivity or recovery time if desired.

Figures 16.18(G) and 16.18(H) replace the zener with a resistance divider. In Figure 16.18(I) the SCS will allow any arbitrary dc voltage across it but is made rate sensitive by the capacitor. It therefore triggers when a "rate threshold" is exceeded.

CIRCUIT CONFIGURATIONS FOR TURNING OFF THE SCS

PNPN devices readily turn on but are much more difficult to turn off. This had led to jokes such as: First engineer, curiously, "How long did it take that PNPN to

THRESHOLD CIRCUITS
Figure 16.18

turn off?" Second engineer, frustratedly, "I don't know; I've been trying to get it off since 9 this morning without success!" Thus it is important to consider carefully the available means for turning off the SCS when closing a circuit configuration.

The simplest turn off is achieved by operating from ac as in Figure 16.19(A), the SCS turning off when the anode becomes negative. Figure 16.19(B) shows full wave rectified ac can be used provided the anode voltage drops to zero each half cycle, i.e., provided no filtering capacitance or inductive load is used. When operating from a dc supply, the anode can be opened as in Figure 16.19(C). A resistor to the anode gate suppressed rate effect when the switch is reclosed. Figure 16.19(D) turns off the SCS by reverse biasing the anode when the switch is closed. The capacitor charging current through R_L minimizes rate effect. R_C should be as large as possible to avoid rate effect when the switch is opened. Figure 16.19(E) uses a shunt transistor to divert the SCS current permitting recovery. By transformer coupling the turn-off pulse, the load may be in series with either the cathode or anode. Inductive loads can

TURN-OFF METHODS
Figure 16.19

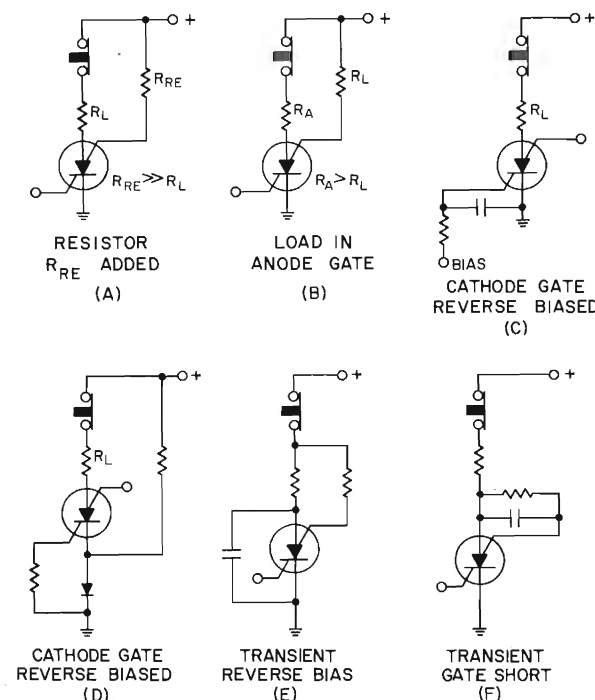
be made to ring to turn off the SCS, or inductance may be added to turn off resistive loads. Figures 16.19(F) and 16.19(G) illustrate this for high and low resistance loads, respectively. The equations shown indicate the practical limits for R_L and C. Figures 16.19(H) and 16.19(I) indicate that the gates can be used to turn off the SCS. The range of anode current that can be turned off and the "turn-off gain" are quite different for the 3N58 series and the 3N80 series. Just as a positive pulse to the anode gate turns off the SCS, a negative pulse to the anode as in Figure 16.19(J) achieves the same result. The resistor R_A is a function of R_L. Moving the load into the anode results in Figure 16.19(K). Where a number of devices are to be turned off simultaneously a transistor can be used with the preceding circuit as shown in Figure 16.19(L).

Often it is desirable to have the load connected to the anode gate. The anode current to hold the device on is substantially less than the load current permitting turn-off gain and rate effect suppression in Figure 16.19(M).

Substantial ac loads can be controlled by small turn-off inputs in the circuit of Figure 16.19(N). The dc current exceeds the holding current to keep the SCS on, once it is triggered. On negative half cycles the ac load disconnects preventing turn off. While the diode is reverse biased the SCS can readily be turned off by several of the methods above.

CIRCUIT CONFIGURATIONS FOR MINIMIZING RATE EFFECT

When a PNPN device appears to take milliseconds to recover, it is found that while recovery in fact occurs within a few microseconds, rate effect turns the device back on when voltage is reapplied. Figure 16.20 suggests several ways of suppressing

MINIMIZING RATE EFFECT
Figure 16.20

rate effect. The simplest, in Figure 16.20(A), consists of adding an anode gate resistor which charges the center junction capacitance while the anode is open. Figure 16.20(B) transfers the load to the anode gate so that the switch carries less current and rate effect is eliminated. Figures 16.20(C) and 16.20(D) illustrate two methods of reverse biasing the cathode gate to decrease rate effect. In Figure 16.20(D) the diode in effect generates a bias voltage which may be shared by other devices, if desired.

Often a reverse bias can be generated during the voltage transient. In Figure 16.20(E), the anode rises more slowly than the anode gate.

Loop gain can be suppressed by using a capacitor as shown in Figure 20(F). The capacitor shorts out the anode junction on a transient basis; the shunting resistor allowing the capacitor to discharge when the switch is open. Shorting the anode gate to the anode can be considered a variation of this circuit.

CIRCUIT DESIGN "RULE OF THUMB"

It is often handy to be able to check the feasibility of a circuit at a glance. This can be done readily with the help of a few basic ideas.

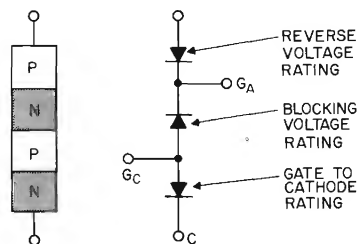
1. When the PNPN is blocking make sure the voltage ratings are not exceeded. While blocking, there is no transistor action and the device can be considered to be three interconnected diodes as shown in Figure 16.21. Figure 16.21 also indicates which SCS rating determines each diode breakdown.

VOLTAGE RATINGS

Figure 16.21

2. The SCS cannot be turned on unless both end junctions are forward biased. If a gate is open circuited it may be considered forward biased. Generally it is necessary to forward bias only one junction, the second becoming forward biased by the resulting transistor action.
3. Consider power supply and noise transients which may cause inadvertent triggering.
4. Check the circuit for rate effect. Be sure the gates are shunted or reverse biased while the anode voltage is rising. Generally, it is sufficient to control one gate only.
5. The effects of capacitors connected from anode to cathode must be carefully evaluated since extremely high peak currents and consequent high junction temperatures may result. The junction thermal mass and transient thermal resistance allow calculation of the maximum junction temperature.
6. A simple but useful equivalent circuit of the SCS while conducting is shown in Figure 16.22. Using the cathode as a reference, the anode appears as an approximate 1 volt battery with an ohmic series resistance. The anode gate

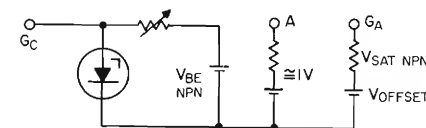
can be considered the collector of a saturated NPN transistor. The saturation offset voltage can generally be ignored and the saturation resistance is modulated over about a 2:1 range, inversely with anode current. The cathode gate or base of the NPN exhibits the conventional $V_{BE\,(SAT)}$ of a saturated transistor. The variable resistor represents r_b', which is modulated over a range of 10:1 by the magnitude and direction of gate current. The zener, i.e., emitter-base breakdown limits the maximum gate reverse voltage.

SIMPLIFIED EQUIVALENT CIRCUIT DURING CONDUCTION

Figure 16.22

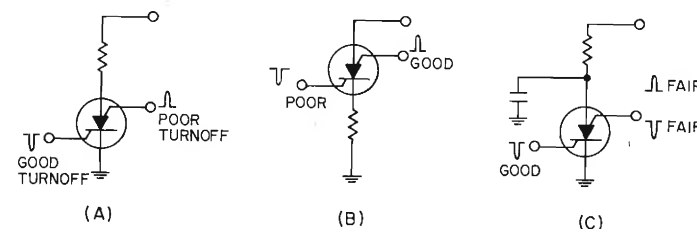
7. It is easy to overlook some of the more subtle aspects of turning off a PNPN by means of reverse biasing a gate. Figure 16.23(A) shows that a cathode gate input is effective in turning off the SCS. In effect the cathode is reverse biased preventing PNPN action. What remains is a saturated PNP transistor which turns off as carriers recombine. A positive input to the anode gate is much less effective since it cannot reverse bias the anode junction.

GATE TURN-OFF POSSIBILITIES

Figure 16.23

When the load is moved to the cathode as in Figure 16.23(B), the cathode junction can no longer be reverse biased but the anode gate becomes more effective in turn-off.

Figure 16.23(C) modifies the above discussion if the anode is shunted by a capacitor. The cathode gate is as effective as before, possibly more so since rate effect is also suppressed. A positive input to the anode gate, however, tries to raise the forward voltage across the SCS. The capacitor holds it down forcing the anode current below the holding current and the SCS turns off. A negative input to the anode gate is coupled by the forward biased anode junction to the capacitor pulling the anode below ground. On releasing the anode gate the SCS can recover while the anode is reverse biased.

MEASUREMENT

The test conditions given in defining and specifying the electrical characteristics suggest appropriate test circuits. While many of the tests can be performed on a Tektronix 575 Curve Tracer care is required both in setting the CRO and in interpreting the waveforms. Furthermore, the settings and waveforms often change considerably with operating point making interpretation more difficult. Suitable settings for the Tektronix 575 Curve Tracer are beyond the scope of this chapter and are discussed in a separate General Electric Application Note.

DC MEASUREMENTS

The junction breakdown voltages are readily measured using techniques identical to those for diodes or transistors. Measurements with the SCS forward biased (either blocking or conducting) require special care. First, it is essential that the conditions existing at all four leads be specified. Second, the test circuitry must avoid voltage transients or rate effect. Since hum or noise pick up can trigger the SCS, circuit layout should take appropriate precautions. Anode to cathode capacitance must be avoided unless its effect on holding current, peak anode current, and temperature are considered.

Several methods of specifying triggering parameters are possible. In the interests of measurement precision, the triggering voltage range is measured using a low impedance voltage source at the gate. The triggering current, however, is derived from a current source.

Figure 16.24 shows a simple test set for measurement of 3N58 characteristics. Push buttons are used throughout. With no buttons depressed, the SCS has an 800 ohm anode load resistor and 10K from gate to ground. The voltmeter primarily monitors whether the SCS has triggered. Pressing the V_{GTC} MIN button should not trigger the SCS. Pressing the V_{GTC} MAX button should. On releasing the button, V_F can be read. The RESET button allows the SCS to recover. Pressing the I_{GTC} button should again trigger the SCS. Pressing the I_H button should result in the anode voltage remaining at approximately one volt. The zener triggers the SCS in case it inadvertently turned off prior to this test. Figure 16.25 shows a comparable circuit for a 3N59.

DC PARAMETER TEST SET FOR 3N58

Figure 16.24

DC PARAMETER TEST SET FOR 3N59

Figure 16.25

TRANSIENT MEASUREMENT

Recovery Time

As with dc measurements it is essential that conditions at all four leads be specified for meaningful measurement. The definition of recovery time generally used for PNPN devices applies to the SCS also. The defining waveform is shown in Figure 16.26. Initially the device is conducting. A capacitively coupled negative transient equal to the anode supply voltage reverse biases the anode. The device is said to have recovered if the anode voltage rises to the anode supply voltage without the unit retriggering. The recovery time is defined as the time from the initiation of the negative transient until the anode voltage crosses through zero.

Figure 16.26 ANODE WAVEFORM DEFINING RECOVERY

Figure 16.27 RECOVERY TEST SET

A suitable circuit for measuring recovery time is shown in Figure 16.27. Whenever the mercury relay contacts open a positive pulse appears at the anode which results in the 2N1711 shorting the gates together. This is a most effective way of triggering the SCS. It also permits shorting the cathode gate to cathode as is required by the 3N59 specification. Once the SCS turns on, the triggering circuitry is completely isolated. Closure of the mercury relay contacts supplies the prescribed negative transient to the anode. The capacitor is increased until the SCS just recovers and the recovery time is recorded. The capacitor value will, of course, depend on the load resistance R_A.

Turn-On Time

By considering the SCS as an NPN transistor with an additional diode in series it is obvious that at least all the factors affecting transistor turn-on time are also applicable here. Gate biases prior to the turn-on transient, control delay-time. The magnitude of gate current also determines how rapidly regeneration will start. A suitable test circuit for the 3N58 is shown in Figure 16.28. A mercury relay of the make before break variety is used. The anode load resistor, the initial impedance from gate to cathode and the triggering current resistor are chosen. When the upper relay contact opens, trigger current is applied. Eventually the contact recloses and the bottom contact opens. This permits the capacitor to charge, shorting out the SCS with the 2N1711. As soon as the zener clamps the capacitor the anode is permitted to rise to the supply voltage. The bottom contact recloses discharging the capacitor. The cycle now repeats. The zener is primarily for limiting the 2N1711 emitter reverse voltage. A similar circuit for the 3N59 is shown in Figure 16.29.

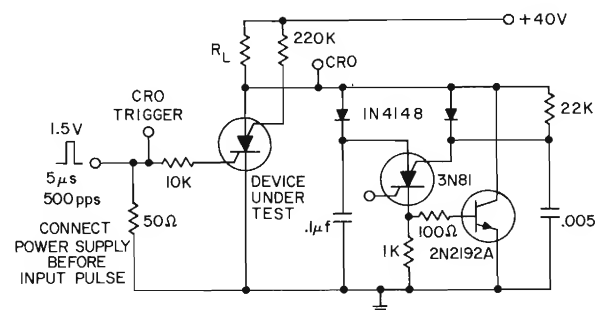



Figure 16.28 3N58 TURN-ON TIME TEST SET

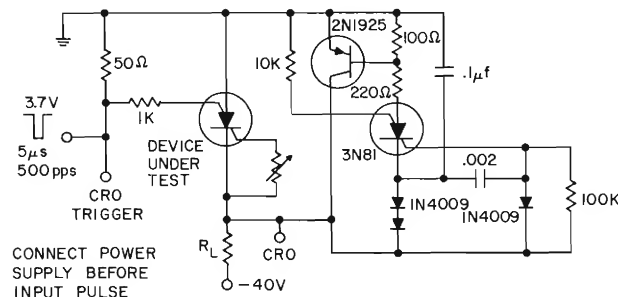
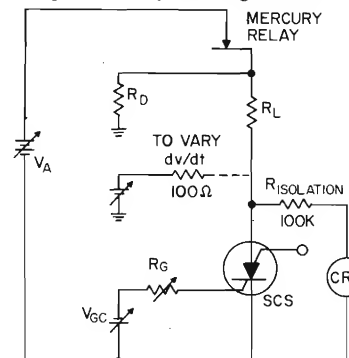



Figure 16.29 3N59 TURN-ON TIME TEST SET

Rate Effect — Dynamic Breakover Voltage

It is a simple matter to apply a fast anode voltage to the SCS. One precaution is necessary, however. Using the circuit in Figure 16.30 it is important that the anode voltage be raised until the SCS triggers and then decreased until the SCS ceases to trigger. The latter is the *dynamic breakover voltage*. The reason for this is as follows: while V_A is increasing the center junction capacitance charges slightly with each closure of the relay, then maintains the charge while the anode becomes reverse biased as the relay opens. Therefore to get the capacitance to charge fully due to a single closure it is necessary to discharge it first by causing the SCS to trigger.

RATE EFFECT TEST SET
Figure 16.30

A capacitor may be used to vary the rate to rise with R_D discharging the capacitor between cycles. The CRO input capacitance must be isolated from the SCS to get the fastest waveforms. The gate impedance and bias voltage can be varied as desired.

Part 2 — SCS Characteristic Curves

Two sets of characteristic curves are shown representing the two different SCS structures. One set of curves pertains to types 3N58 through 3N60 which are grown diffused devices, fixed-bed mounted on a ceramic disc and housed in a TO-12 case. The other set of curves pertains to the more recent types 3N81 through 3N86 which are planar devices housed in a TO-18 size package.

The planar devices offer higher voltage and current ratings at lower cost and are therefore the preferred types for new designs. Care should be exercised in substituting PLANAR devices for the 3N58-3N60 series due to the different gate-to-cathode impedances required for the two products. Particular attention should be given to the differences shown by the curves for anode holding current (I_H) and anode gate current to trigger (I_{GTA}) as a function of gate to cathode impedance.

These differences result from the lower internal resistances inherent with the planar product. The lower resistances give the 3N81-3N86 distinct advantages in gate turn-off and dissipation characteristics but cause a profound effect on I_H and I_{GTA} when the cathode gate is shorted to the cathode as is done in the 3N59 characterization.

Lower internal resistance in the planar product permits substantially higher current ratings for the anode gate. In many cases, this allows placing the load in the anode gate rather than the anode thus improving immunity to noise, eliminating rate effect problems (dv/dt) and presenting circuit possibilities with high turn-off gain.

SCS types 3N81 and 3N82 represent "the center of the line." They are thoroughly characterized and yet manufacturable at high yield to maintain uniformity and low cost. The 3N83, 3N84 and 3N85 are functionally-oriented less demanding types. The 3N86 is a premium high performance type for the most demanding applications.

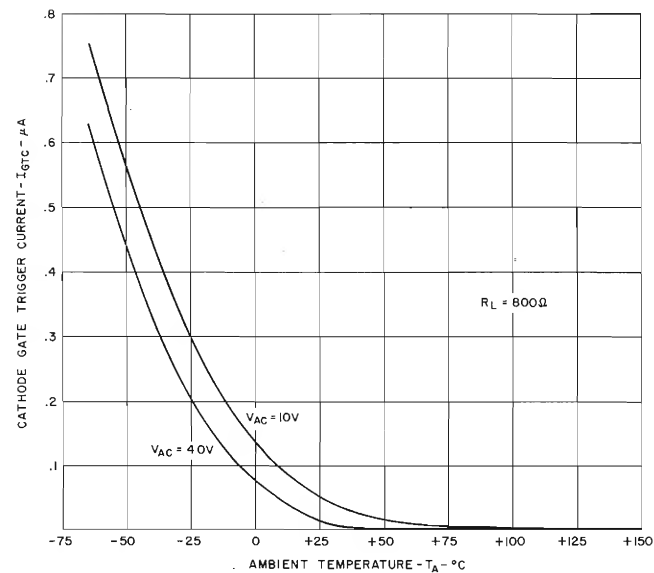
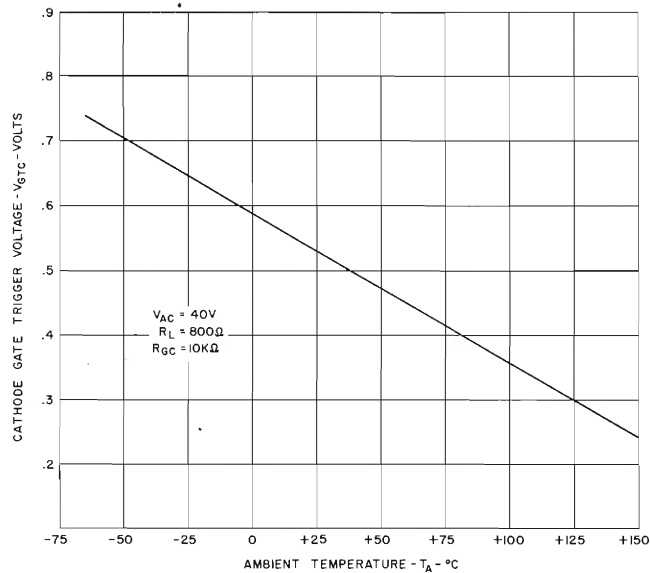
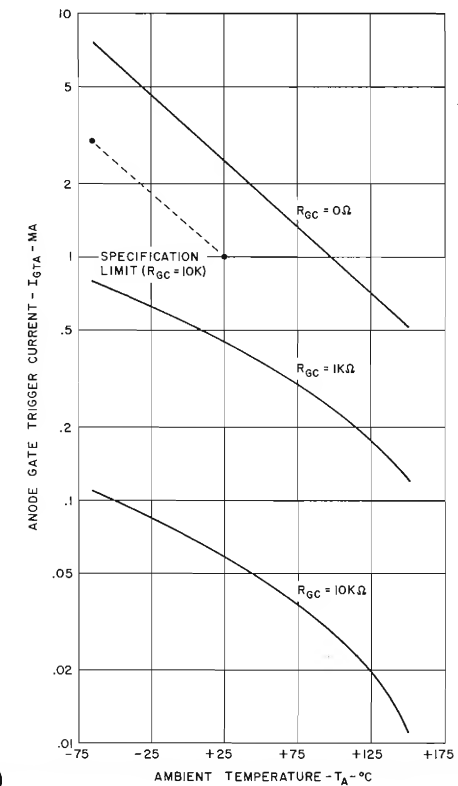
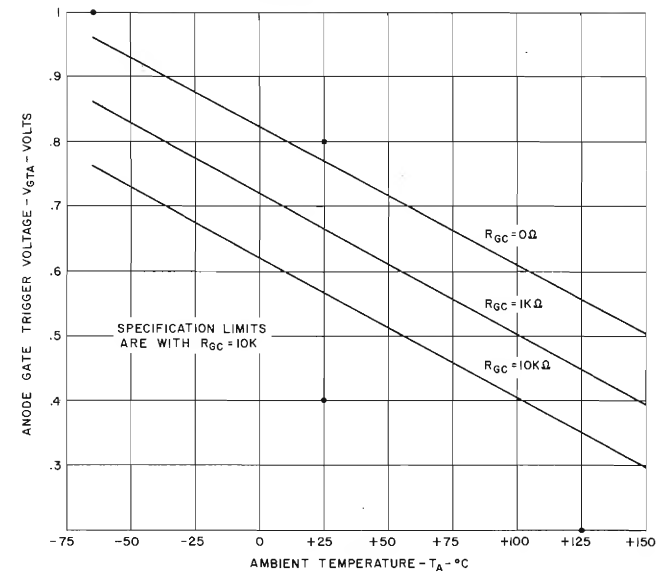



Figure 16.31

TRIGGERING (3N81, 3N82)

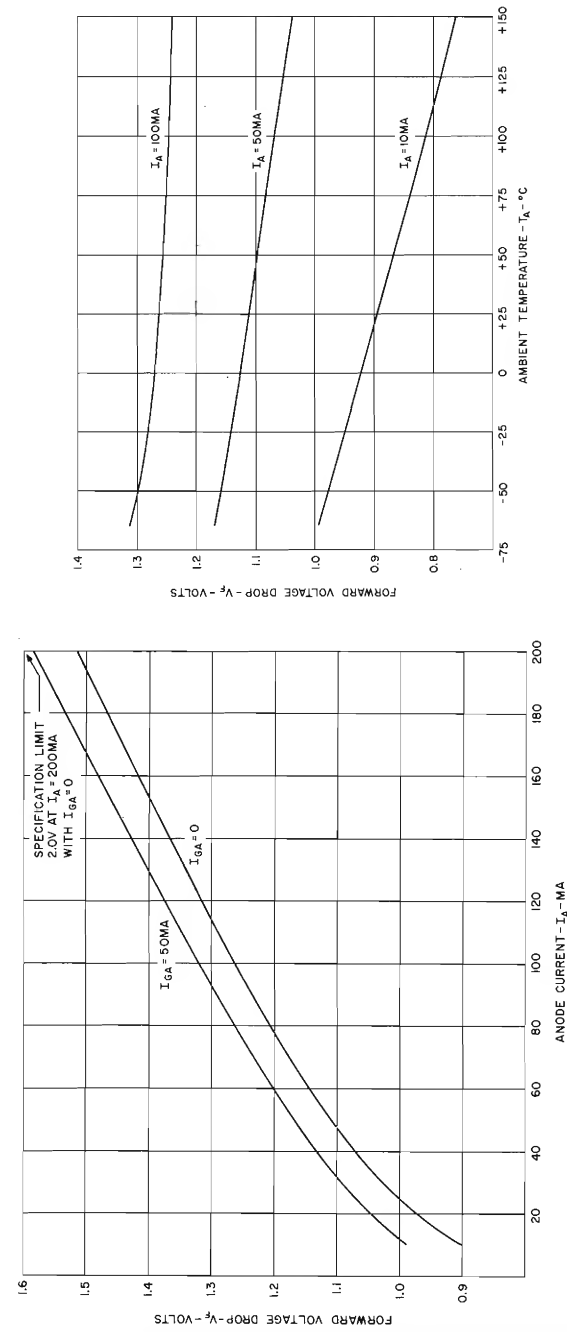
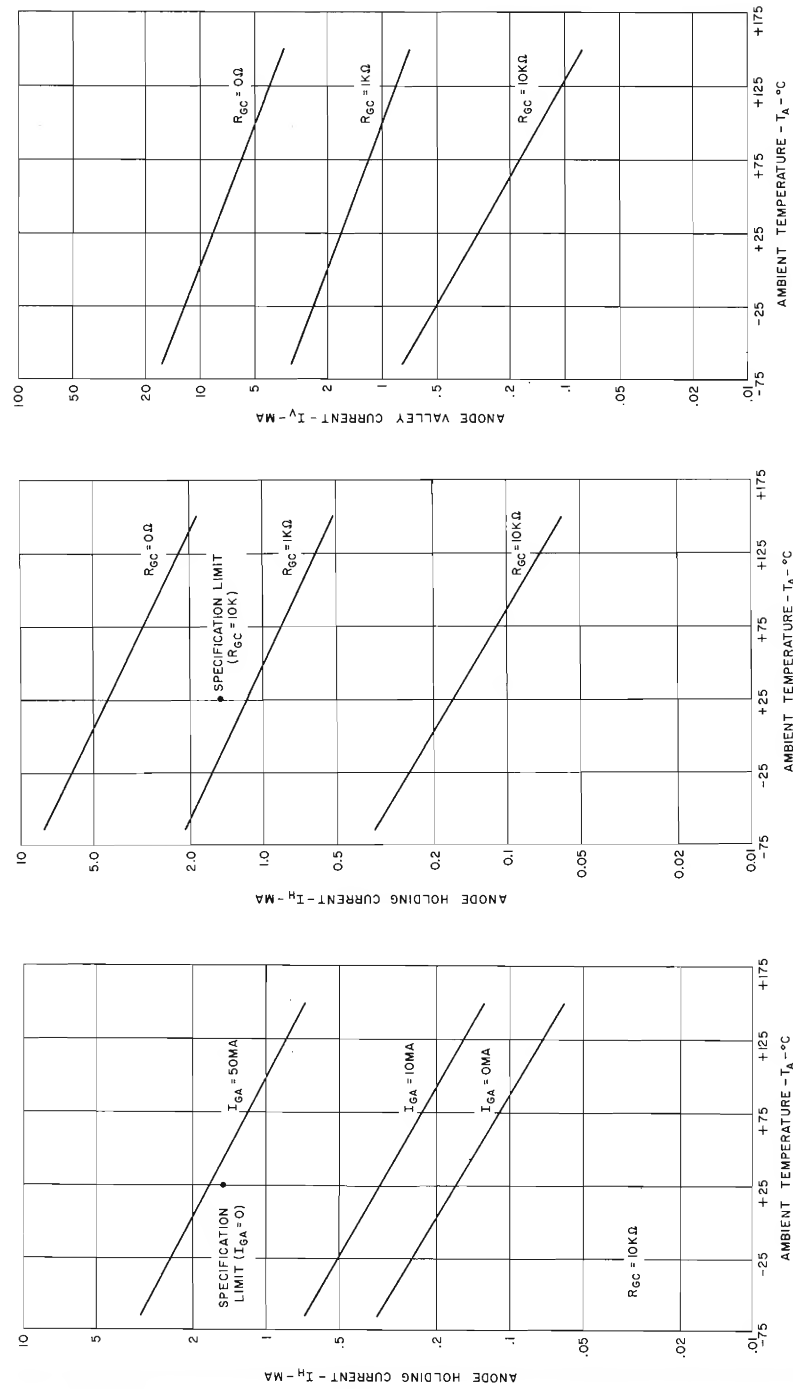



Figure 16.32 FORWARD (3N81, 3N82)

ANODE TURN-ON TIME - t_{on} - μSEC

I_A = 100MA

I_A = 10MA

I_{GA} = 3MA

R_{GC} = 10KΩ

AMBIENT TEMPERATURE - T_A - °C

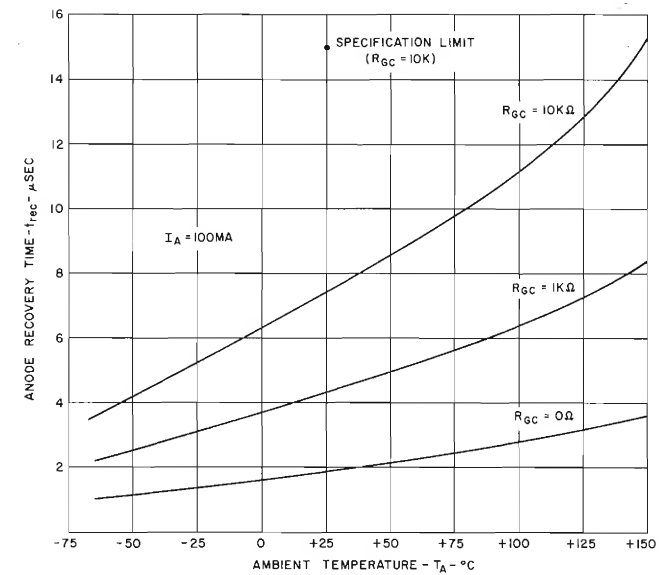
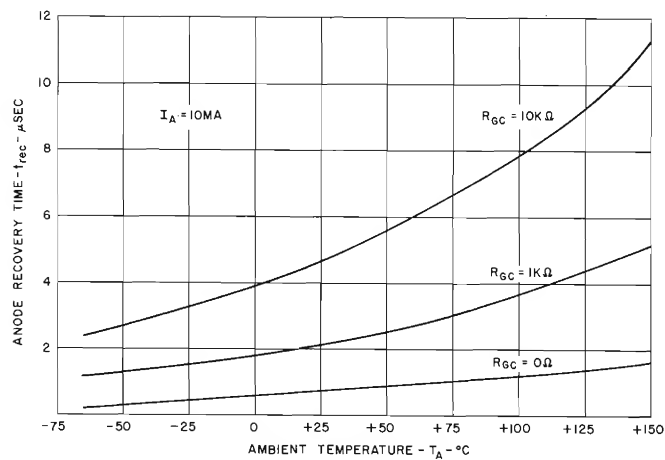
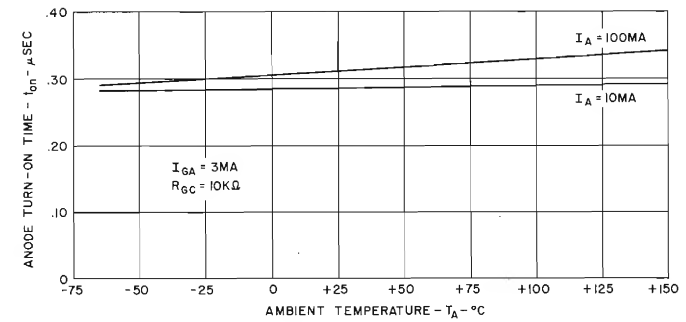
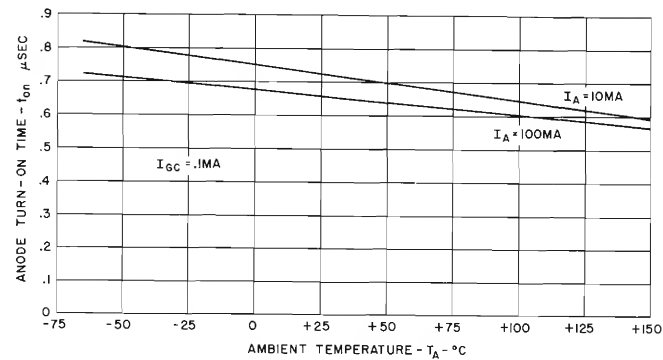



Figure 16.33

TRANSIENT (3N81, 3N82)

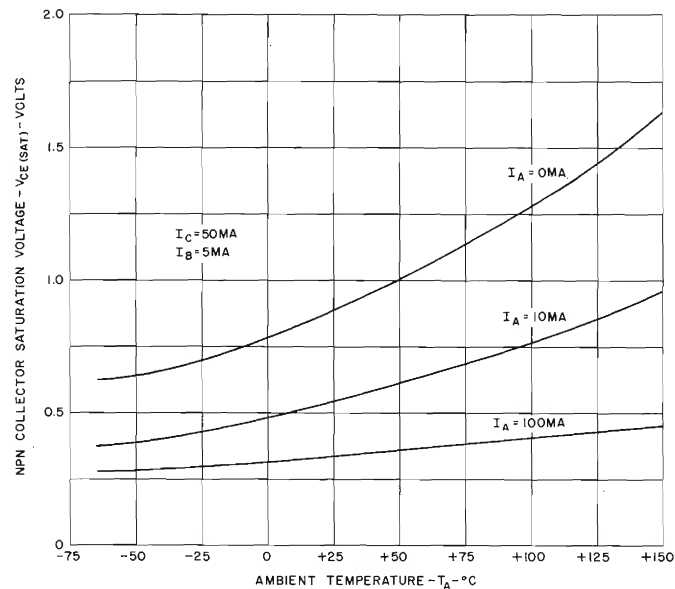
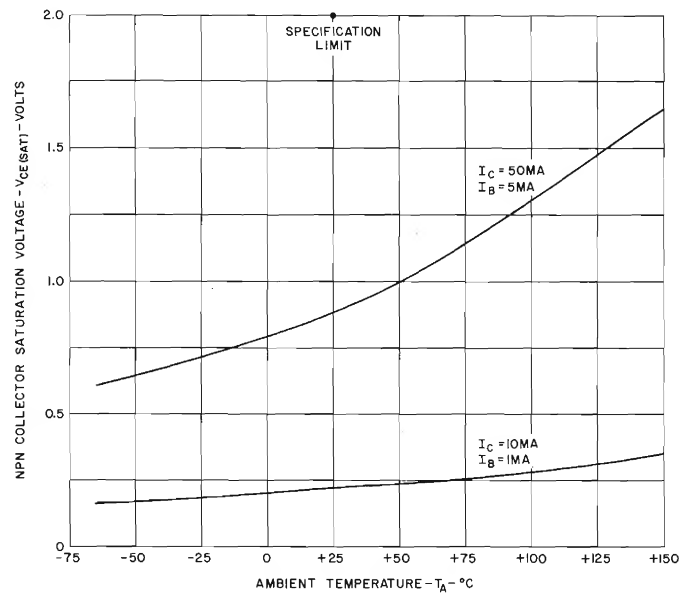



Figure 16.34 COLLECTOR SATURATION (3N81, 3N82)

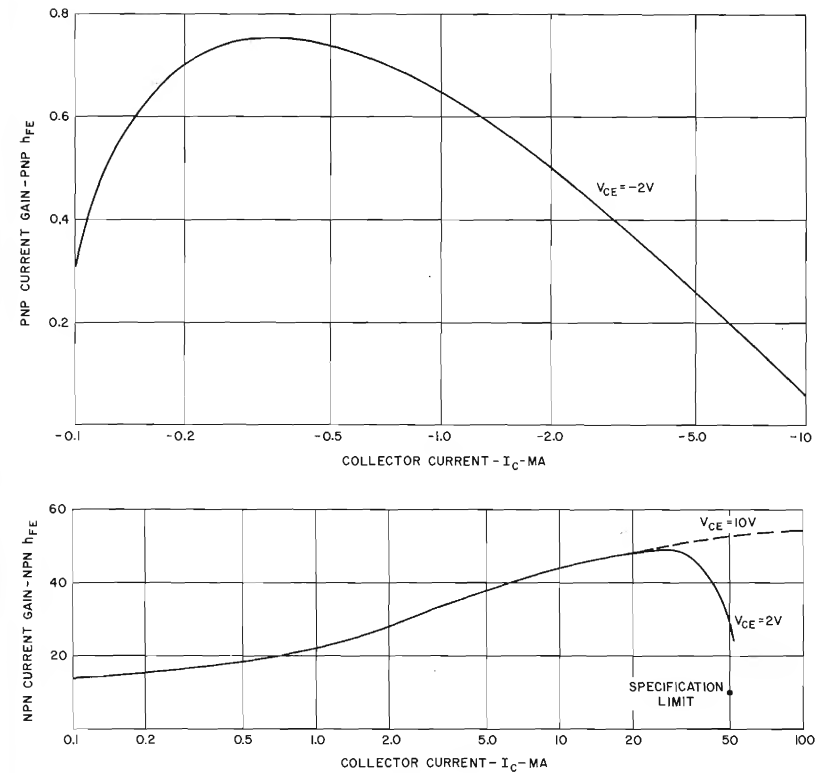



Figure 16.35 CURRENT GAIN (3N81, 3N82)

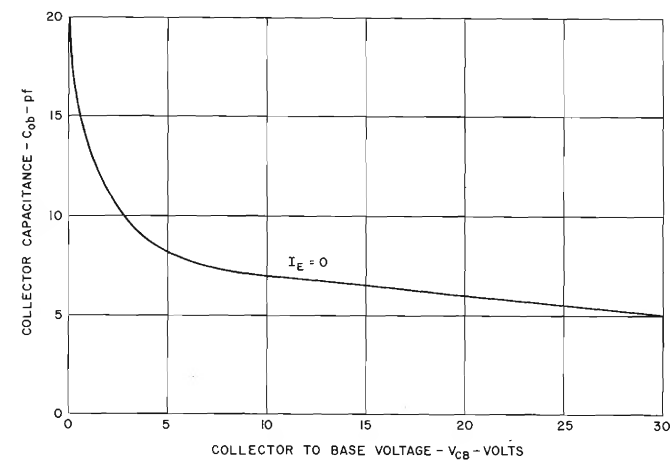
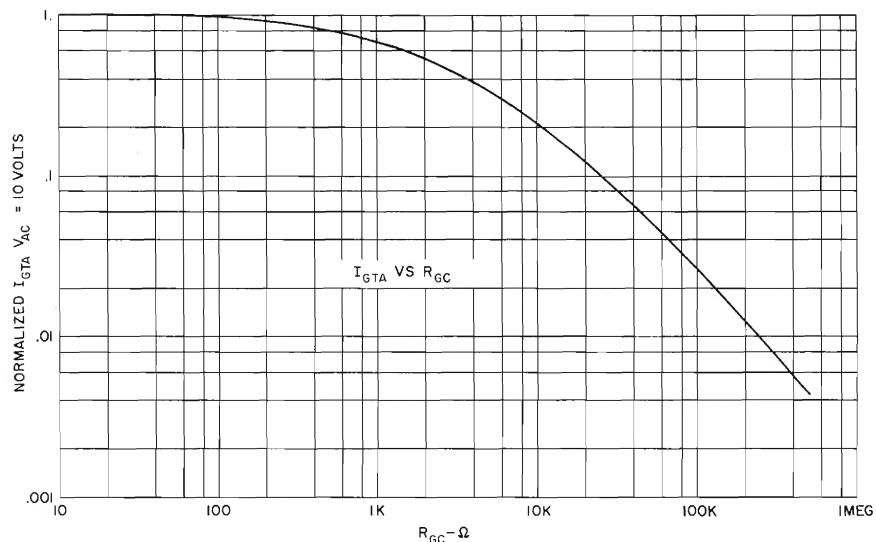
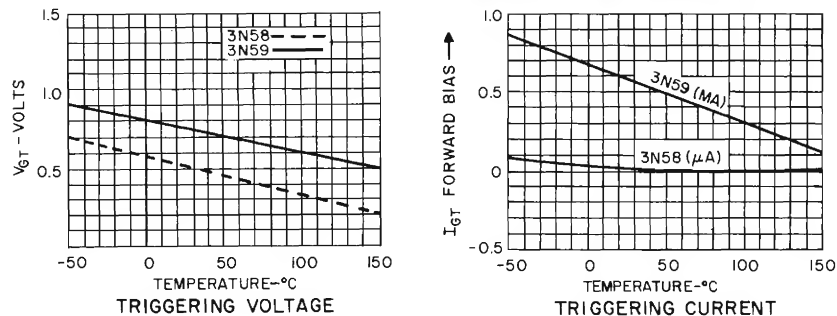



Figure 16.36 COLLECTOR CAPACITANCE (3N81, 3N82)

TRIGGERING VOLTAGE

TRIGGERING CURRENT

NORMALIZED ANODE GATE TRIGGERING CURRENT VS. CATHODE GATE RESISTANCE

NORMALIZED ANODE GATE TRIGGERING CURRENT VS. ANODE TO CATHODE VOLTAGE

TRIGGERING (3N58 TO 3N60)

Figure 16.37

FORWARD VOLTAGE

HOLDING CURRENT

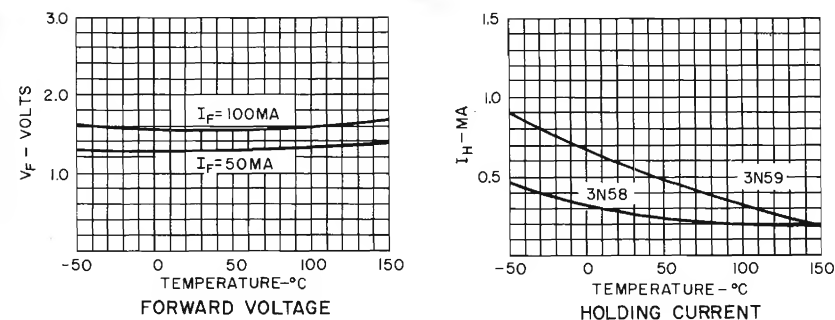
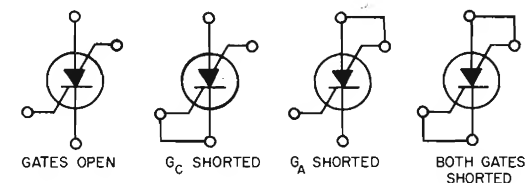



Figure 16.38 FORWARD (3N58 TO 3N60)

	GATES OPEN	G_C SHORTED	G_A SHORTED	BOTH GATES SHORTED
BREAKOVER VOLTAGE V_{BO} VOLTS	0 TO 20	70	50	80
REVERSE VOLTAGE V_R VOLTS	80	80	4	0.5
I_H MA	0	0.5 TO 1	2 TO 3	2 TO 3
I_{BO} MA (TO FIRE)	0	0.5	2	4
I_{GFC} MA (TO FIRE)	–TO 1μA		10 TO 60 μA	
V_{GFC} VOLTS (TO FIRE)	0.4 TO 0.6		0.5 TO 0.8	
I_{GFA} MA (TO FIRE)	0 TO 8μA	0.2 TO 1.0 MA		
V_{GFA} VOLTS (TO FIRE)	0.4 TO 0.6	0.6 TO 0.9		

TYPICAL ANODE CHARACTERISTICS

Figure 16.39 3N58 TO 3N60 SERIES

CENTER JUNCTION CAPACITANCE

Figure 16.40 3N58 TO 3N60 SERIES

	3N58						3N59			
	I_{GC}=20μA			I_{GC}=100μA			I_{GA}=3MA		I_{GA}=1MA (R_{GC}=10K)	
	I_A(MA)			I_A(MA)			I_A(MA)		I_A(MA)	
	1	10	100	1	10	100	10	100	10	100
+125°C	1.00	1.00	.95	.65	.65	.70	.50	.50	.60	.65
+25°C	1.10	1.15	1.05	.70	.70	.70	.45	.50	.60	.60
-65°C	1.40	1.45	1.40	.75	.75	.75	.45	.50	.55	.55

TURN ON TIME

MINIMUM DYNAMIC BREAKOVER VOLTAGE IN	
-3N58 CONFIGURATION	13 V
-3N59 CONFIGURATION	35 V
-3N58 CONFIGURATION WITH V_{GC} = -1V	50 V
-3N59 CONFIGURATION WITH V_{GA} = +1V	80 V
STATIC BREAKOVER VOLTAGE	80 V

DYNAMIC BREAKOVER

RECOVERY TIME

RECOVERY TIME

TRANSIENT (3N58 TO 3N60)

Figure 16.41

Part 3 — SCS Circuit Applications

The circuits chosen for this section are representative of the wide range of applications open to a four terminal SCS. They were selected to illustrate basic principles such as suppression of rate effect and methods of turn off. The SCS is applied as a high gain DC amplifier; an SCR; a complementary SCA; a latching NPN transistor and as a PNP-NPN integrated transistor pair. Additional circuit data is available from the editor on request.

+12V
RESET
100K (FOR RATE EFFECT)
ALARM RELAY 200Ω
ALTERNATE INPUT
Z 100K Y
Y X
3N81 OR 3N84
POSITIVE PULSE TRIGGERS SCS
SET 1K TO 1M
-12V

WHEN R_S DECREASES SUFFICIENTLY TO FORWARD BIAS THE SCS, THE ALARM IS ACTIVATED.

INTERCHANGING R_S AND THE POTENTIOMETER TRIGGERS THE SCS WHEN R_S INCREASES.

TEMPERATURE, LIGHT, OR RADIATION SENSITIVE RESISTORS UP TO 1 MEGOHM READILY TRIGGER ALARM WHEN THEY DROP BELOW VALUE OF PRESET POTENTIOMETER. ALTERNATELY, 0.75V AT INPUT TO 100K TRIGGERS ALARM. CONNECTING SCS BETWEEN GROUND AND -12V PERMITS TRIGGERING ON NEGATIVE INPUT TO G_A.

(A) ALARM CIRCUIT

USE 3N81 FOR HIGHER CURRENT LAMPS

ANY OF SEVERAL INPUTS PULLS IN COMMON ALARM RELAY WITH LAMPS GIVING VISUAL INDICATION OF TRIGGERING INPUT. LOW RESISTANCE LAMPS DECREASE INPUT SENSITIVITY.

(B) MULTIPLE ALARM CIRCUIT

(C) ALARM TRIGGERED BY DEVIATION FROM GROUND

Figure 16.42 VOLTAGE SENSING

SCR REPLACEMENT

NEON DRIVER

BETTER CIRCUIT

(A) NEON

(B) NIXIE TUBE

Figure 16.43

LAMP	RATING		SCS	SEC. VOLTS RMS	
	VOLTS	AMPS		T1*	T2
24	24	.035	3N81	34	24
327	28	.04	3N81	40	28
330	14	.08	3N81	20	14
344	10	.015	3N81	14	10
1829	28	.07	3N81	40	28

*INCREASED VOLTAGE GIVES NORMAL BRIGHTNESS IN HALF WAVE CIRCUIT

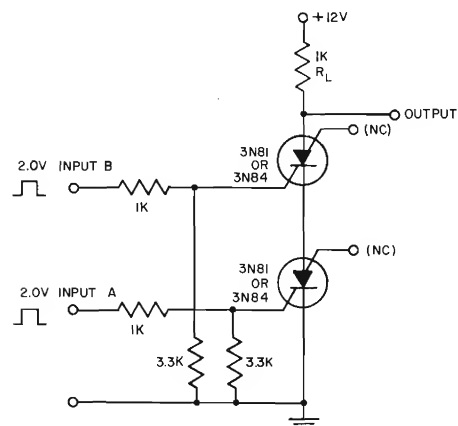
(C) INCANDESCENT LAMP DRIVERS

THE 2N2646 OSCILLATOR TURNS ON THE 2N527 FOR APPROX. 20μSEC AT A 1KC RATE. IF THE INPUT IS AT 0.7 VOLTS THE SCS TURNS ON GENERATING A PULSE TO TRIGGER THE SCR DRIVING THE LAMP. BY USING A BRIDGE RECTIFIER AND A 1KC PULSE RATE THE LAMPS GIVE NORMAL BRILLIANCE. A 0.2V INPUT DOES NOT TURN ON THE SCS AND THEREFORE THE LAMP.

(D) DRIVING 110V INCANDESCENT LAMPS BY LOW LEVEL LOGIC

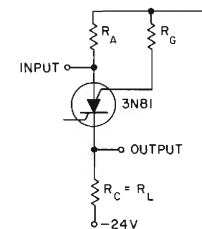
LAMP DRIVERS

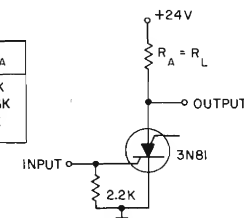
THE RESISTOR DIVIDER CONNECTED BETWEEN Q1 AND Q2 SUPPLIES I_H TO Q1 AFTER INPUT A TRIGGERS IT. IT ALSO PREVENTS INPUT B FROM TRIGGERING Q2 UNTIL Q1 CONDUCTS. CONSEQUENTLY THE FIRST B INPUT PULSE AFTER INPUT A IS APPLIED WILL SUPPLY CURRENT TO R_L.

(A) PULSE SEQUENCE DETECTOR

UNLESS INPUTS A AND B (2 TO 3V AMPLITUDE) OCCUR SIMULTANEOUSLY NO VOLTAGE EXISTS ACROSS R_L. LESS THAN 1 MICROSECOND OVERLAP IS SUFFICIENT TO TRIGGER THE SCS. COINCIDENCE OF NEGATIVE INPUTS IS DETECTED WITH GATES G_A INSTEAD OF G_C BY USING THE SCS IN A COMPLEMENTARY SCR CONFIGURATION.

(B) PULSE COINCIDENCE DETECTOR

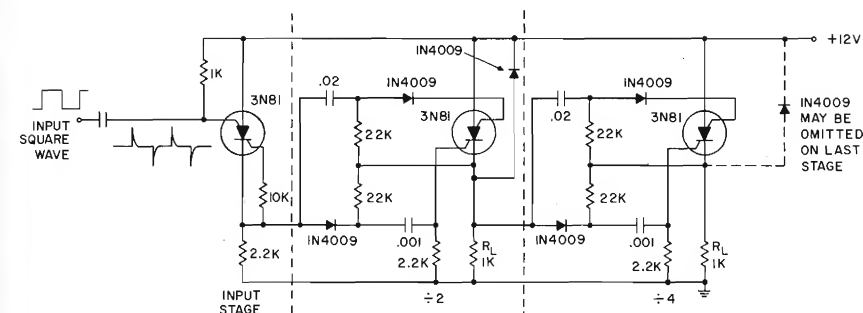
LOGIC
Figure 16.44

V_{ON}	V_{OFF}	R_A	R_G	R_C
+1	−1	100	470	10K
+1	−1	100	100	3.3K
+1	−1	100	0	1K
+1	−3	100	0	330

LOAD IN CATHODE - OUTPUT IN PHASE WITH INPUT

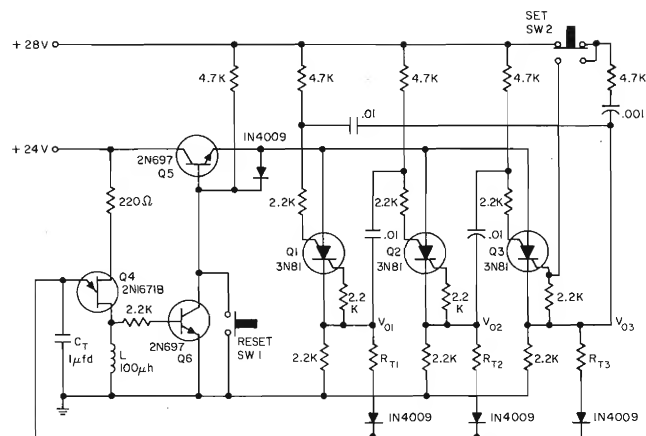
V_{ON}	V_{OFF}	R_A
+.6	0	10K
+.6	−1	3.3K
+.6	−4	1K

LOAD IN ANODE - OUTPUT OUT OF PHASE WITH INPUT

INPUT PULSES OF INDICATED AMPLITUDE WILL TRIGGER BISTABLE CIRCUITS. OPPOSITE PHASE INPUT CAN BE APPLIED TO R_G. FOR DIFFERENT SUPPLY VOLTAGES ADJUST R_L TO KEEP LOAD CURRENT CONSTANT.

BISTABLE MEMORY ELEMENTS

MEMORY ELEMENTS
Figure 16.45

STAGES ARE TRIGGERED BY POSITIVE GOING EDGE. THE SCS IS TURNED ON AT THE CATHODE GATE; TURNED OFF AT THE ANODE GATE. THE ANODE-TO-CATHODE IN4009 SUPPRESSES POSITIVE TRANSIENTS WHILE THE SCS IS RECOVERING. THE INPUT STAGE GENERATES FAST POSITIVE EDGES TO TRIGGER THE COUNTER.

BINARY COUNTER

COUNTERS
Figure 16.46

SHIFT PULSES ARE GENERATED BY THE UNIJUNCTION TRANSISTORS. THE INTERVALS BETWEEN PULSES ARE CONTROLLED BY C_T AND R_T. A DIFFERENT R_T CAN BE SELECTED FOR EACH STAGE OF THE COUNTER AS SHOWN.

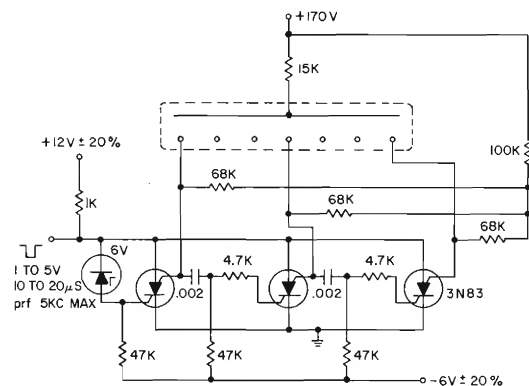
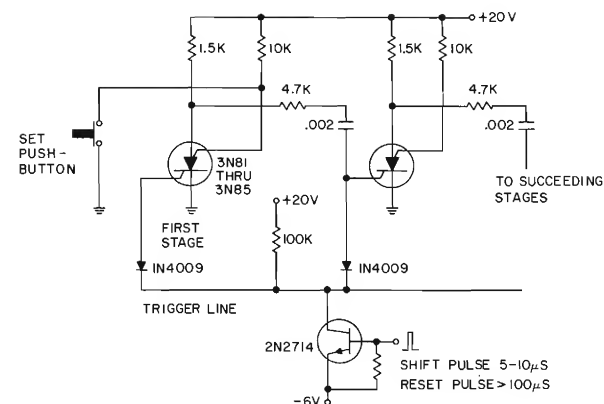
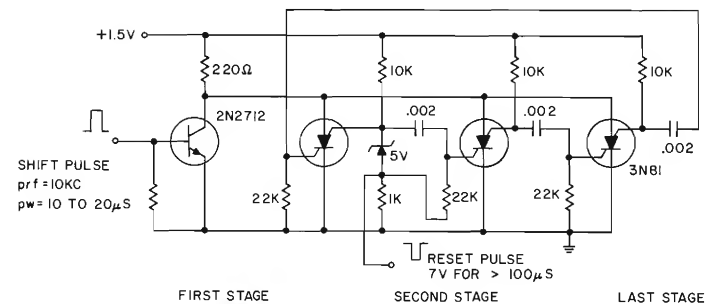
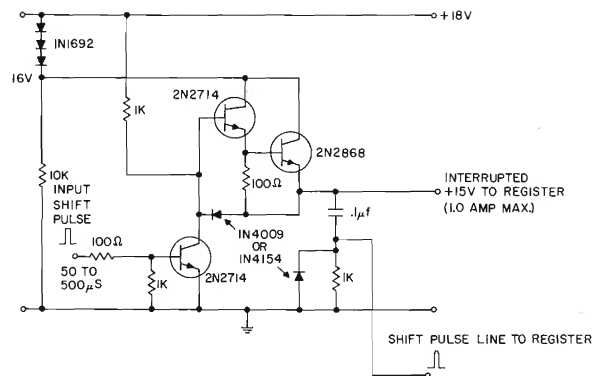
(A) RING COUNTER WITH VARIABLE TIMING

(B) NIXIE TUBE RING COUNTER

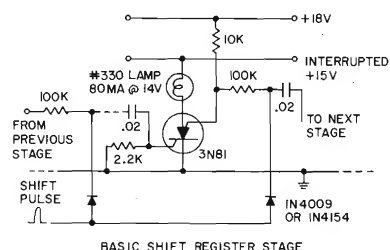
Figure 16.47

THE SHIFT PULSE TURNS OFF THE CONDUCTING SCS BY REVERSE BIASING THE CATHODE GATE. THE CHARGE STORED ON THE COUPLING CAPACITOR THEN TRIGGERS THE NEXT STAGE. AN EXCESSIVELY LONG SHIFT PULSE CHARGES UP ALL THE CAPACITORS, TURNING OFF ALL STAGES. GROUNDING AN ANODE GATE WILL "SET" THAT STAGE.

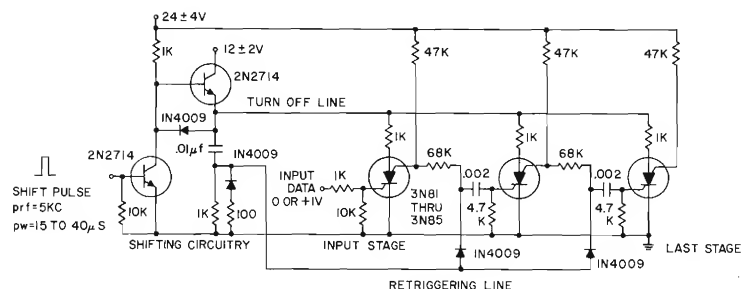
(C) 20 KC RING COUNTER

RING COUNTER OPERATES FROM 1.0 TO 6.0V REQUIRING ONLY 6 MILLIWATTS AT 1.5V. THE RESET PULSE TURNS ON THE FIRST STAGE WITH ITS TRAILING EDGE. MAXIMUM SHIFT PULSE WIDTH INCREASES WITH VOLTAGE AND APPROACHES 70μS FOR A 6.0 SUPPLY. MINIMUM PULSE WIDTH IS 10μS.

(D) EXTREMELY LOW POWER RING COUNTER (LESS THAN 6 MW)

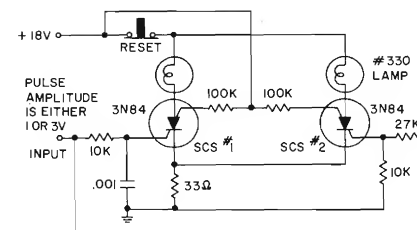
RING COUNTERS

A 16 VOLT POWER SUPPLY CAN BE SYNTHESIZED AS SHOWN USING IN1692 RECTIFIERS. A SHIFT PULSE INPUT SATURATES THE 2N2714 DEPRIVING THE DARLINGTON COMBINATION (2N2714 AND 2N2868) OF BASE DRIVE. THE NEGATIVE PULSE SO GENERATED ON THE 15V LINE IS DIFFERENTIATED TO PRODUCE A POSITIVE TRIGGER PULSE AT ITS TRAILING EDGE.

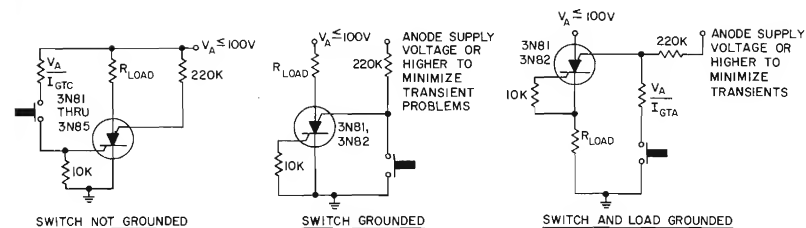
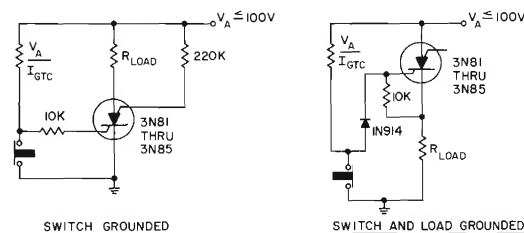
(A) SHIFT REGISTER DRIVER

BASIC SHIFT REGISTER STAGE

THE SHIFT PULSE AMPLITUDE IS LESS THAN 15 VOLTS. IF A STAGE IS OFF, THE SHIFT PULSE WILL NOT BE COUPLED TO THE NEXT STAGE. IF IT IS ON, THE DIODE WILL CONDUCT TRIGGERING THE NEXT STAGE. JUST PRIOR TO THE SHIFT PULSE THE ANODE SUPPLY IS INTERRUPTED TO TURN OFF ALL STAGES. THE STORED CAPACITOR CHARGE DETERMINES WHICH STAGES WILL BE RETRIGGERED.

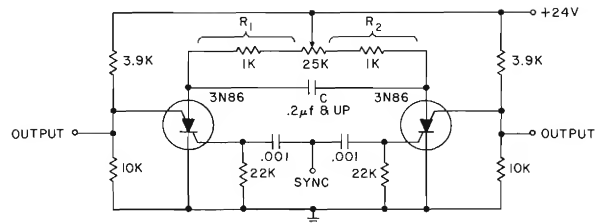
(B) SHIFT REGISTER

THE SHIFT PULSE TURNS OFF ALL SCS'S. THE TRAILING EDGE OF THE TURN OFF PULSE IS DIFFERENTIATED AND TURNS ON THE APPROPRIATE STAGES. THE 2N2714 WILL EASILY DRIVE TEN STAGES.

(C) SHIFT REGISTER

Figure 16.48 SHIFT REGISTERS

A ONE VOLT AMPLITUDE PULSE TRIGGERS SCS #1 BUT HAS INSUFFICIENT AMPLITUDE TO TRIGGER SCS #2. A THREE VOLT INPUT PULSE IS DELAYED IN REACHING SCS #1 BY THE 10K AND .001μf INTEGRATING NETWORK. INSTEAD, IT TRIGGERS SCS #2 THEN RAISES THE COMMON EMITTER VOLTAGE TO PREVENT SCS #1 FROM TRIGGERING. THE 100K RESISTORS SUPPRESS RATE EFFECT.

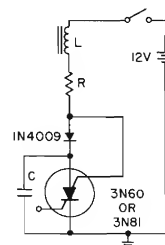
PULSE AMPLITUDE DISCRIMINATOR
Figure 16.49

SWITCH CLOSED TO TRIGGER SCS

SWITCH OPENED TO TRIGGER SCS

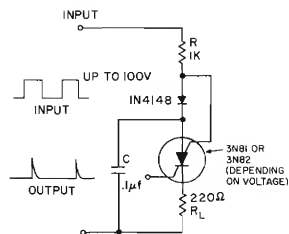
CONTACT ISOLATORS ELIMINATE CONTACT BOUNCE, ISOLATE NOISE ON THE CONTACT LINES AND REDUCE CONTACT CURRENT. THE LOAD CURRENT INCREASES RAPIDLY AND LATCHES ON. THE SCS CAN BE RESET TO THE OFF STATE BY AUXILIARY CIRCUITRY. THE CIRCUITS ARE READILY ADAPTED TO NEGATIVE SUPPLY VOLTAGES.

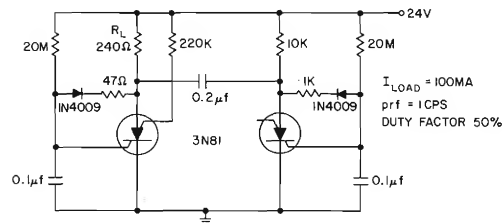
CONTACT ISOLATORS
Figure 16.50

R_1C DETERMINE HALF THE PERIOD; R_2C THE REMAINDER.

$R_1 = R_2$ FOR SQUARE WAVE OUTPUT.

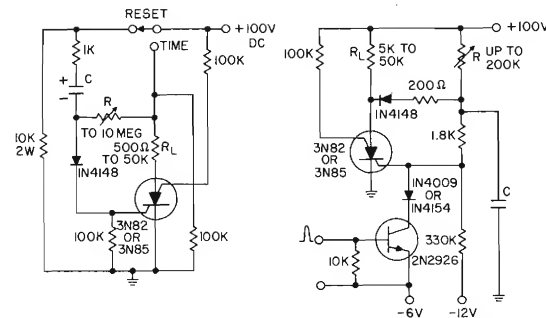
THE POTENTIOMETER VARIES PULSE WIDTH WITHOUT VARYING FREQUENCY. THE OUTPUTS ARE TRANSIENT FREE SQUARE OR RECTANGULAR PULSES, EQUAL AND OPPOSITELY PHASED. SYNCHRONIZATION IS OPTIONAL.

(A) SQUARE WAVE PULSE GENERATOR

A POSITIVE TRANSIENT SUCH AS THE POWER SWITCH CLOSING CHARGES C THROUGH L TO A VOLTAGE ABOVE THE SUPPLY VOLTAGE IF Q IS SUFFICIENT. WHEN CURRENT REVERSES, THE DIODE BLOCKS AND TRIGGERS THE SCS. AS THE CAPACITOR DISCHARGES, THE ANODE GATE APPROACHES GROUND POTENTIAL DEPRIVING THE ANODE OF HOLDING CURRENT. THIS TURNS OFF THE SCS AND C CHARGES TO REPEAT THE CYCLE.

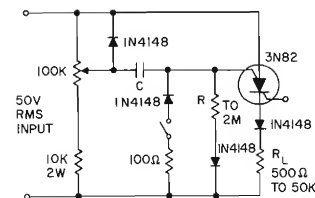
(B) RLC OSCILLATOR

(C) TACHOMETER, SINGLE PULSE GENERATOR, POWER LOSS DETECTOR, PEAK DETECTOR

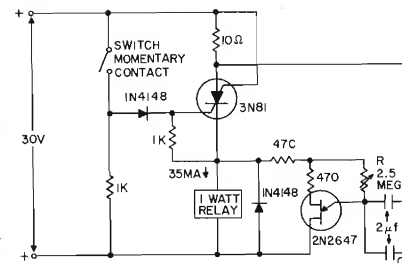
A POSITIVE GOING INPUT CHARGES C THROUGH THE 1N4148 AND R. THE DIODE KEEPS THE SCS OFF. A NEGATIVE GOING INPUT SUPPLIES ANODE-GATE CURRENT TRIGGERING ON THE SCS DISCHARGING C THROUGH R_L.

ELECTROLYTIC CAPACITORS ARE UNNECESSARY TO GENERATE A 1 CPS FREQUENCY. AS AN SCS TRIGGERS ON, THE 0.2µf COMMUTATING CAPACITOR TURNS OFF THE OTHER ONE AND CHARGES ITS GATE CAPACITOR TO A NEGATIVE POTENTIAL. THE GATE CAPACITOR CHARGES TOWARDS 24 VOLTS THROUGH 20M RETRIGGERING ITS SCS. BATTERY POWER IS DELIVERED TO THE LOAD WITH 88% EFFICIENCY. THE 20M RESISTORS CAN BE VARIED TO CHANGE prf OR DUTY FACTOR.

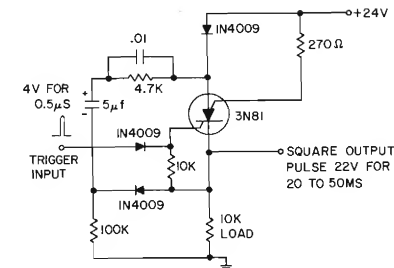
(D) LOW FREQUENCY OSCILLATOR-FLASHER

PULSE GENERATORS
Figure 16.51

LOAD CURRENT STARTS APPROX. 0.5 RC AFTER SWITCH IS THROWN

INPUT PULSE TURNS OFF SCS. SCS TRIGGERS AFTER DELAY OF APPROX. RC

(A) TIMING CIRCUITS

THE SWITCH IS NORMALLY CLOSED CHARGING C AND CAUSING THE SCS TO BLOCK. THE DELAY IS INITIATED BY OPENING THE SWITCH AND DISCHARGING C THROUGH R. SINCE R IS CONNECTED FOR ONLY HALF OF EACH CYCLE THE DELAY IS LENGTHENED BEYOND THE RC TIME CONSTANT. THE DELAY IS VARIED BY R, C, AND THE SETTING OF THE POTENTIOMETER. FOLLOWING THE DELAY THE SCS CONDUCTS ALTERNATE HALF CYCLES.

(B) AC OPERATED TIME DELAY

A POSITIVE PULSE TO THE GATE OF THE SCS TRIGGERS IT ON, SUPPLYING POWER TO THE RELAY LOAD AND UNIJUNCTION TIMING CIRCUIT. AT THE COMPLETION OF THE TIMING INTERVAL BASED ON RC A NEGATIVE PULSE TO THE ANODE TURNS OFF THE SCS.

(C) 10 SECOND TIMER

CAPACITOR (5µf) AND 4.7K DETERMINE STRETCH INTERVAL. CAPACITOR (5µf) AND 100K DETERMINE CIRCUIT RECOVERY TIME. RESISTOR 4.7K SUPPLIES I_H DURING STRETCH INTERVAL. RATIO OF 270Ω TO 10K LOAD CONTROLS I_H OF SCS.

(D) PULSE STRETCHER

TIMING (MONOSTABLE)
Figure 16.52

NOTES

SILICON SIGNAL DIODES & SNAP DIODES

CHAPTER 17

SILICON SIGNAL DIODES

Semiconductor diodes are used extensively in all types of electronic circuitry. Many of the chapters in this manual illustrate applications in which diodes are used, from detectors in radio receivers to gating and logic elements in computer circuits. The first semiconductor diodes, made before the invention of the transistor, were silicon point contact diodes used as detectors in radar receivers. Later, germanium point contact diodes and gold bonded diodes were introduced which could be used in a variety of applications. The demand for high operating temperatures and low leakage currents led to the development of the silicon alloy junction diode and the silicon diffused mesa diode. Reliability and superior electrical characteristics of the silicon diode together with declining prices has caused it to be used in place of germanium diodes in an increasing number of applications.

In addition, by utilizing various properties of silicon diodes several special types of diodes have evolved, i.e., varactor diodes, stabistor diodes, snap diodes, etc. The snap diode is of particular interest because it makes possible highly efficient harmonic generators, and also pulse generators having high repetition rates with extremely short transition times (as low as 0.1 nanoseconds).

PLANAR EPITAXIAL PASSIVATED SILICON DIODE

Silicon diodes can be made using any of the transistor fabrication techniques including alloying, growing, meltback, or diffusion. But on the basis of inherent reliability and overall electrical parameters the *planar epitaxial passivated* (PEP) diode structure has proven superior to all others. Some of the significant advantages of the PEP silicon diode include

1. High forward conductance due to use of epitaxial material.
2. Low, uniform, leakage currents due to passivated surfaces.
3. Low capacitance due to small planar junction.
4. Low reverse recovery time due to accurate control of lifetime with gold doping.
5. High reliability due to passivation and rugged mechanical structure.

Fabrication of the diode starts with a wafer of low resistivity single crystal silicon. A thin epitaxial layer of high resistivity silicon is grown on the wafer. A layer of silicon oxide is formed over the entire wafer and the oxide is removed from small circular "windows" by means of photographic techniques. The planar junctions are then diffused through the windows in the oxide. Gold is plated on the back of the wafer and diffused into the wafer at a temperature determined by the required reverse recovery time. The wafer is cut into pellets each forming a complete diode, and contacts are made to the front and back of the pellets. Each pellet is then mounted in a glass package and the package is sealed.

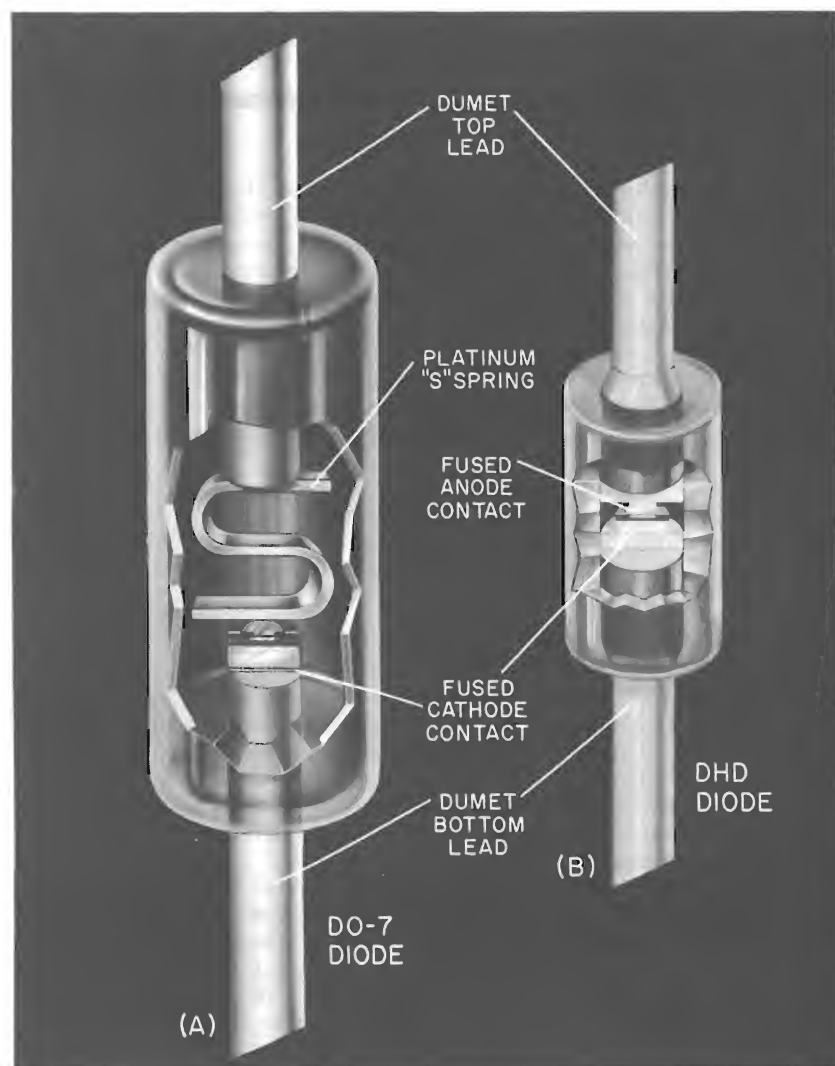
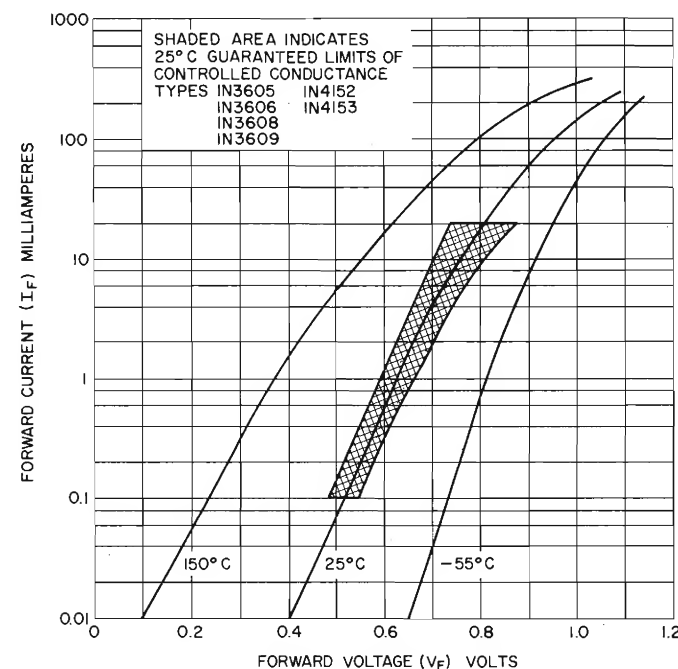
Formation of the junction under a stable silicon oxide layer results in a *passivated* diode which is immune to contaminants which plague other types of silicon diodes. The effectiveness of the passivation is substantiated by a tight distribution of reverse leakage current, a parameter which is usually very sensitive to surface conditions, and by the close correlation between the measured values of the electrical parameters and the theoretical values. The use of an epitaxial structure reduces the bulk resistance of the diode and thus makes it possible to achieve simultaneously a high conductance together with a low capacitance and a low reverse recovery time.

CUT-AWAY VIEW OF PEP SILICON DIODES
Figure 17.1

Figure 17.1 shows the cross section and mechanical structure of the two popular diode glass packages. The *double heat sink* (DHD) diode is smaller than the *conventional* (DO-7) glass diode, yet it has a higher dissipation and greater reliability. These are due to the elimination of the "S" spring and fusion of the pellet directly to the Dumet leads. The heat generated in the pellet is dissipated via the leads. This is brought out by Table 17.1 which gives the thermal resistance and power dissipation as a function of the spacing between the heat sink and the end of the diode body.

HEATSINK SPACING FROM END OF DIODE BODY	STEADY STATE THERMAL RESISTANCE °C/MW		POWER DISSIPATION AT 25°C/MW	
	DO-7	DHD	DO-7	DHD
.062"	.389	.250	450	700
.250"	.500	.319	350	550
.500"	.700	.438	250	400

DIODE THERMAL RESISTANCE AND POWER DISSIPATION
Table 17.1

DC Characteristics

The characterization of the PEP silicon diode is greatly simplified by the close correlation between the theoretical and the actual parameters. The dc characteristics are generally specified by means of the following parameters and characteristic curves.

TYPICAL FORWARD DC CHARACTERISTICS OF PEP SILICON DIODES
Figure 17.2

1. Forward Voltage. The maximum value of the forward voltage, V_F, is generally specified at one or more values of forward current, I_F. For *controlled conductance* diodes such as the 1N3605, 6, 8, 9, 1N4152, and 3 both the minimum and maximum

values of forward voltage are specified at six values of forward current. The relationship between the forward voltage and forward current for a typical PEP silicon diode is shown in Figure 17.2 at three values of ambient temperature. The shaded area indicates the guaranteed range of forward characteristics for the controlled conductance types at 25°C junction temperature. The tight control of forward conductance is very desirable in the design of diode logic circuits where it permits greater design margins or additional logic stages.[1]

Forward dc characteristics of the PEP silicon diodes closely follow the theoretical equation

$$I_F = I_S\left[\exp\frac{q\,(V_F - I_F R_S)}{\eta KT} - 1\right] \qquad (17a)$$

where

I_S = diode saturation current
R_S = diode series ohmic resistance
q = electronic charge (1.60×10^{-19} coulomb)
K = Boltzmanns constant (1.38×10^{-23} watt sec/°K)
T = absolute temperature (°K)

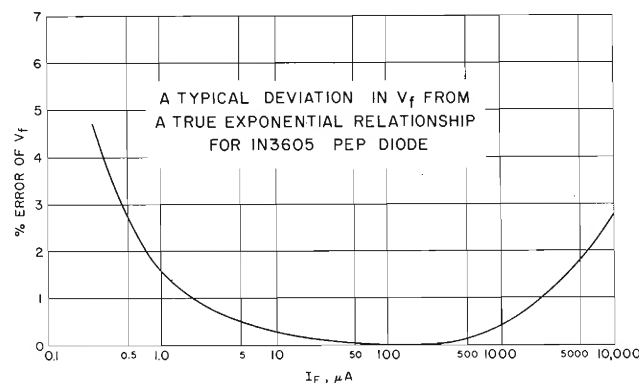
NOTE: $I = I_S\,[\exp(x)] = I_S\,(e^x)$.

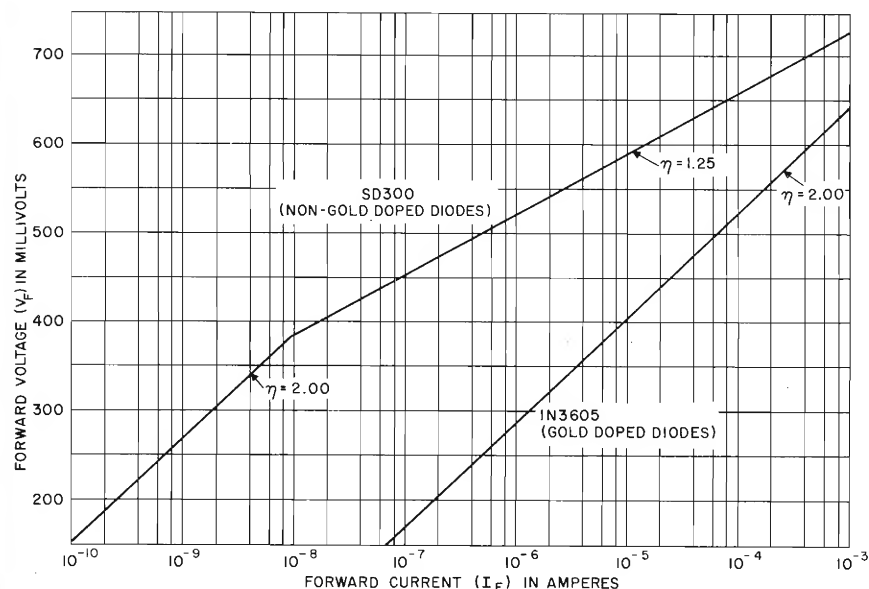
At low forward currents where $I_F R_S << V_F$, and with the exponential term much larger than one, then 17(a) becomes

$$I_F = I_S \exp\frac{qV_F}{\eta KT} \qquad 17(b)$$

or

$$V_F = \frac{\eta KT}{q}\ln\left(\frac{I_F}{I_S}\right) \qquad 17(c)$$

Figure 17.3 shows[5] the deviation of the forward characteristic of a silicon PEP diode from the true exponential equation as given by 17(c). The error is less than 1% from 2μa to 2 ma. At low currents the error increases because the exponential term in 17(a) approaches one. At high currents the increase in error is due to the effect of the $I_F R_S$ term in 17 (a).

A TYPICAL DEVIATION IN V_f FROM A TRUE EXPONENTIAL RELATIONSHIP FOR 1N3605 PEP DIODE
Figure 17.3

Parameter η in the above equations is dependent upon the impurity gradient in the junction and the carrier lifetime in the semiconductor material. At low values of forward current, carrier recombination in the junction depletion layer is the predominant factor in determining the relationship between forward voltage and current, and $\eta \cong 2$. At high values of forward current the relationship between forward current and voltage is determined primarily by minority carrier diffusion, and $\eta \cong 1$ for non-gold doped diodes. The characteristics of the normal gold doped PEP silicon diode can be approximated with reasonable accuracy by assuming that $\eta = 2$ over the entire current range. (At 25°C this gives $\eta KT/q = .052$ volt). η is shown in Figure 17.4 for both gold doped and non-gold doped diodes.

η FOR TWO TYPES OF PEP DIODES
Figure 17.4

Dynamic resistance, r_D, of the diode at a forward current, I_F, is given by the equation

$$r_D = \frac{\eta KT}{q\,I_F} + R_S \qquad 17(d)$$

Since R_S is typically 1 to 2 ohms for a PEP diode, the dynamic impedance is inversely proportional to the current up to about 10 ma.

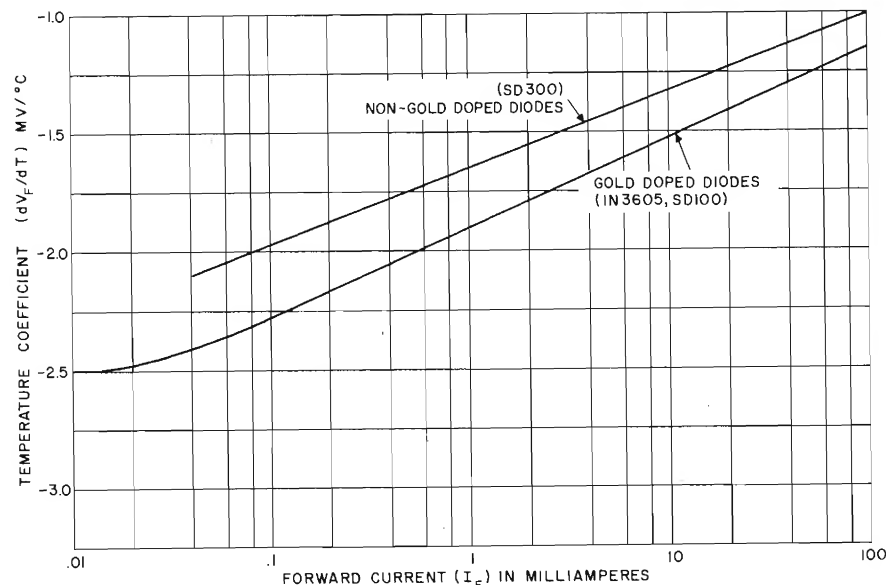
Forward voltage-temperature coefficient can be determined by taking the voltage differential of 17(a) with respect to temperature (remembering that I_S is a function of temperature). Figure 17.5 shows that for a 1N3605, 1N4152, and SD300, (dV_F/dT) is a strong function of forward current.

V_F TEMPERATURE COEFFICIENT AS A FUNCTION OF FORWARD CURRENT

Figure 17.5

The empirical equations which describes these relations are: for the 1N4152 and 1N3605 series-gold doped diodes

$$\frac{dV_F}{dT} = -1.92 + 0.6 \log_{10} I_F \qquad (17e)$$

and for SD300 non-gold doped diodes

$$\frac{dV_F}{dT} = -1.66 + 0.33 \log_{10} I_F \qquad (17f)$$

where I_F is in milliamperes and dV_F/dT is mv/°C. The constant terms in 17(e) and 17(f) are functions of I_S, η, and T (the absolute temperature), while the coefficients of the $\log_{10} I_F$ terms are proportional to $\eta K/q$. For germanium the constant term is larger than for silicon, while the coefficient of the log term is small. Thus, dV_F/dT for germanium is not as strong a function of I_F as it is with silicon.

2. Breakdown Voltage. The breakdown voltage, B_V, is normally specified at a reverse current of 5 μa. The breakdown voltage increases with temperature up to the point where the reverse leakage current becomes comparable with the current at which the breakdown voltage is measured. The breakdown characteristic of a PEP diode may not be as sharp as that of a non-epitaxial diode. The shape of the breakdown characteristic can be explained theoretically, and life tests have shown that this is not as indicative of reliability as it is with other types of diodes.

3. Reverse Current. The reverse current, I_R, is specified at a voltage below the breakdown voltage. The magnitude of the reverse current is dependent on the area of the junction and upon whether the diode has been gold doped or not. Thus, for a given area the I_R of a non-gold doped unit (SD300) will be two to three orders of magnitude less than the I_R of a gold doped unit (1N3605). Typical leakage currents

of these two types of diodes at 30 volts and 25°C are 0.02 and 20 nanoamperes respectively. Reverse current increases exponentially with temperature as indicated by the equation

$$I_R = I_{RO} \exp \delta (T - T_o) \qquad (17g)$$

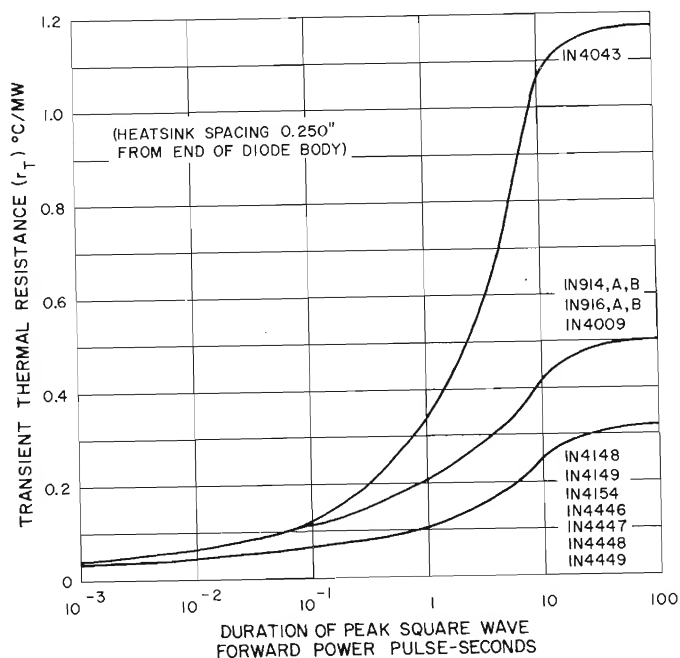
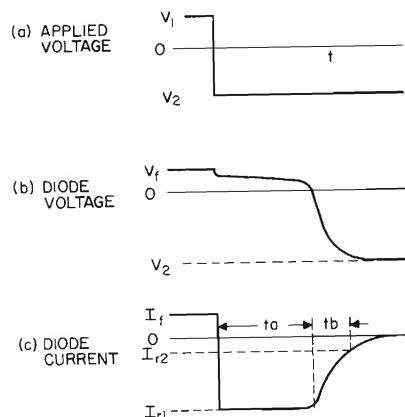
where I_R is the reverse current at temperature T, I_{RO} is the reverse current at temperature T_o, and δ is the fractional increase of I_R with temperature. For the PEP silicon diodes (1N3605, 1N4152) $\delta \cong 0.055/°C$. The reverse current will increase by a factor of ten when the temperature is increased by $2.30/\delta = 42°C$. At low values of reverse voltage the reverse current is proportional to the square root of the voltage owing to the spreading of the depletion layer. At values of reverse voltage comparable to the breakdown voltage, the reverse current increases rapidly due to avalanche multiplication and localized breakdown effects.

AC Characteristics

1. Capacitance. The capacitance normally specified for a diode is the total capacitance which is equal to the sum of the junction capacitance and the fixed capacitance of the leads and the package. The capacitance, C_o, is specified at a frequency of 1 mc with zero applied bias. Since the typical capacitance of some PEP silicon diodes is less than 1.0 pf it is necessary to use a three terminal bridge configuration to achieve an accurate measurement. The junction capacitance is inversely proportional to the square root of the reverse voltage and increases linearly with temperature.

2. Rectification Efficiency. The rectification efficiency, R_E, is defined as the ratio of dc load voltage to peak rf input voltage to the detector circuit, measured with 2.0 volts rms, 100 mc input to the circuit. Load resistance is 5K and the load capacitance is 20 pf. The rectification efficiency is determined primarily by the conductance, reverse recovery time, and capacitance, and provides an indication of the capabilities of the diode as a high frequency detector.

3. Transient Thermal Resistance. The transient thermal resistance of a diode is presented by a curve such as Figure 17.6 showing the instantaneous junction temperature as a function of time with constant applied power. This curve permits a determination of the peak junction temperature under any type of pulsed operation. By means of a simple analytical procedure, described in Reference 2, this curve can be used to determine the peak junction temperature under any type of transient operation and hence provides a valuable method of insuring the reliable operation of diodes in pulse circuits.[2]

4. Forward Recovery Time. If a large forward current is suddenly applied to a diode, the voltage across the diode will rise above its steady state value and then drop rapidly, approaching the steady state value in approximately an exponential manner. This effect is caused by the finite time required to establish the minority carrier density on both sides of the junction. The forward recovery time is the time required for the diode voltage to drop to a specified value after the application of a step of forward current. The forward recovery time increases for a given area device as the breakdown voltage increases and the capacitance decreases (increasing resistivity), and as the reverse recovery time decreases (decreasing lifetime). Under some extremes of resistivity and lifetime, the forward recovery time can be longer than the reverse recovery time. For a given diode the forward recovery time also increases as the rate of rise of the forward current is increased, and decreases as the forward current flowing prior to the current step is increased. If the amplitude of the forward current step is sufficiently small the effect of the junction capacity will predominate and prevent the diode voltage from overshooting its steady state value.

MAXIMUM TRANSIENT THERMAL RESISTANCE
Figure 17.6

TYPICAL DIODE REVERSE TRANSIENT WAVEFORMS
Figure 17.7

5. Reverse Recovery Time. When a forward biased diode is subjected to a reverse voltage step, a large reverse current will flow for a short time as a result of the stored charge consisting of the minority carriers on both sides of the junction. The typical

voltage and current waveforms involved as shown in Figure 17.7. Initially, a current I_F is flowing in the diode and a voltage V_F appears across it. When the reverse voltage step occurs at $t = 0$ a reverse current I_{r1} flows which is determined by the magnitude of the applied voltage and the loop impedance of the circuit. At the same time the forward voltage decreases by an amount approximately equal to $R_S\ (I_F + I_{r1})$ due to the reversal of the current through the diode. The reverse current remains constant at I_{r1} for a time t_a (the constant current phase) and then rapidly decreases, approaching the dc reverse current value. At the same time the diode voltage goes negative and approaches the value of the applied reverse voltage.

The reverse recovery time of a diode, t_{rr}, is specified as the time between the application of reverse voltage and the point where the reverse current has dropped to a specified value, I_{r2}. The specification must also include the forward current, I_F, the initial reverse current, I_{r1}, and the loop impedance of the test circuit. The specification of the reverse recovery time of diodes is difficult to use for circuit design purposes because the recovery time is given only for one arbitrary test circuit and bias condition. Due to the wide variety of possible circuit arrangements and bias conditions encountered in diode applications, it is impossible for the manufacturer to control and specify the reverse recovery time corresponding to each special condition encountered. However, for most design requirements an accurate estimation of the reverse recovery time can be obtained by use of a quantity called the *effective lifetime*, τ, and the ratio of the forward and reverse currents. Figure 17.8 can be used for this purpose together with Figure 17.9 which gives the typical effective lifetime of the PEP silicon diode as a function of temperature for various values of forward current.

The use of Figure 17.8 and 17.9 in estimating the reverse recovery time of a PEP silicon diode can be best described by means of the following design example.

Problem: Estimate the typical recovery time to 5 ma reverse current (I_{R2}) when the forward current is 20 ma (I_F) and the initial reverse current is 15 ma (I_{r1}) at a temperature of 75°C.

Solution: Enter the left side of Figure 17.8 at $I_{r1}/I_f = 15/20 = 0.75$ and follow horizontally (dotted line) until the t_a vs. I_{r1}/I_f line is reached. From the t/τ scale on the horizontal axis, it is seen that $t_a = 0.31\tau$. The t_b portion of the curve is estimated by moving downward parallel to the general contour lines until reaching the line corresponding to $I_{r2}/I_f = 5/20 = 0.25$. The total switching time is thus 0.44τ. From Figure 17.9 the effective lifetime at $I_F = 20$ ma and $T_J = 75$°C is 6.0 nsec, hence the calculated values are

constant current phase $t_a = (0.31)\ (6.0) = 1.86$ nsec.
reverse recovery time $t_{rr} = (0.44)\ (6.0) = 2.64$ nsec.

For additional material on the reverse recovery time of diodes see References 3 and 4.

6. Stored Charge. Increasing use is being made of stored charge, Q_S, as a parameter for characterizing the reverse recovery time of diodes. For a given diode type and structure there is a direct correlation between the reverse recovery time in a given circuit to a given set of conditions and the stored charge so that the two measurements are equivalent. However, the use of stored charge as the specified parameters offers a number of significant advantages over the use of reverse recovery time.

1. Stored charge is a single unambiguous figure of merit for a diode which can be specified without an elaborate set of test conditions and test jig construction details. It is generally sufficient to specify only the forward current at which the stored charge is measured.
2. The test circuit for measurement of stored charge is simple and relatively inexpensive. A direct meter readout is possible even with high speed diodes, and the use of an expensive sampling scope is avoided.

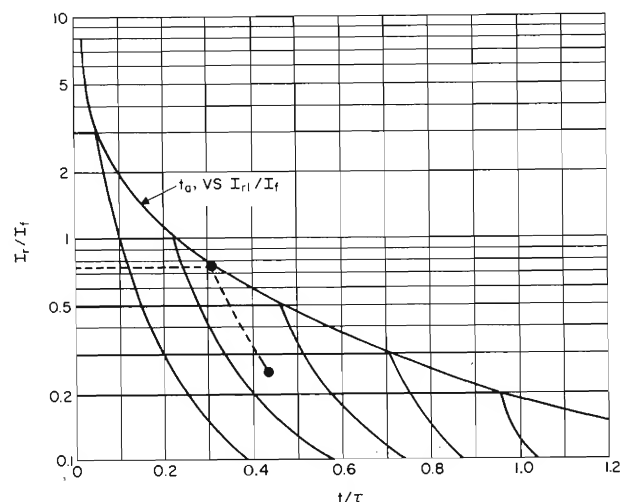
3. Reproducibility of stored charge measurements are better than the reproducibility of reverse recovery time measurements.
4. Comparative reading of stored charge can be made even on ultra-fast recovery diodes which can not be measured on the fastest sampling scopes.

CURVE FOR DETERMINING REVERSE RECOVERY TIME UNDER VARIOUS DRIVE CONDITIONS

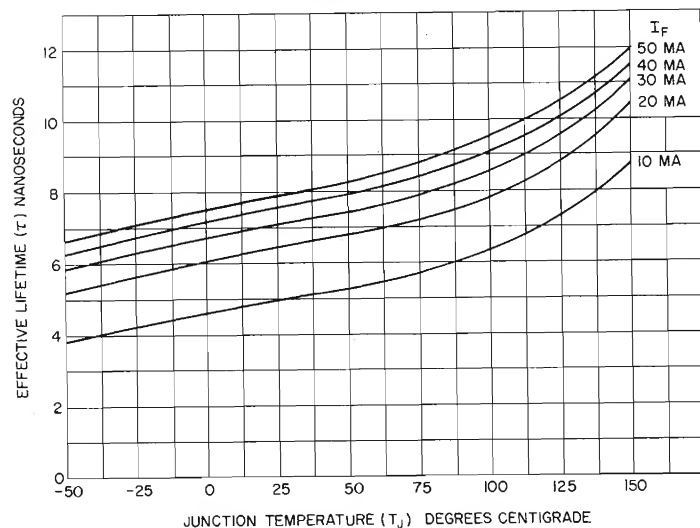
Figure 17.8

EFFECTIVE LIFETIME OF PEP SILICON DIODES VS. TEMPERATURE AND FORWARD CURRENT

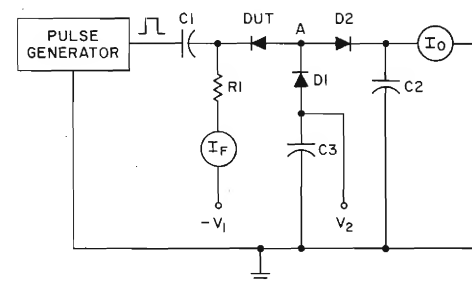
Figure 17.9

BASIC DIODE STORED CHARGE TEST CIRCUIT

Figure 17.10

The basic circuit for measurement of stored charge is shown in Figure 17.10. In this circuit the diode under test (DUT) is biased by a forward current which flows through D1, the DUT, R1, and the bias current meter I_F. A short positive pulse at a known frequency, f, is coupled from the pulse generator through C1 to the DUT. This pulse reverse biases the DUT and forces the charge stored on the DUT through D2 into the output current meter I_o. The current through the meter I_o will be proportional to the charge stored on the DUT. If the forward voltage across the DUT is set to zero by adjusting V_1, an output current I_1 will flow which is proportional to the capacitance of the DUT.

$$I_1 = f\,V_P\,C_{avg} + f\,t_p\,I_r \qquad (17h)$$

where f is the pulse frequency, V_p the amplitude of the pulse, C_{avg} the average capacitance of the diode over the range of reverse voltage from 0 to V_p, t_p the pulse width, and I_r the reverse leakage current of the DUT measured at a reverse voltage equal to V_p. The storage charge is defined by the equation

$$Q_S = \frac{I_2 - I_1}{f} \qquad (17i)$$

where I_2 is the output current at the specified value of forward current, and I_1 the output current with a zero bias voltage across the DUT. Inasmuch as the above definition of Q_S involves the difference between two bias conditions it reduces the dependance of the measurement on the pulse voltage and the reverse current of the DUT, and thus provides a more significant parameter for characterizing the diode. Effects of leakage current, junction capacitance, pulse amplitude and pulse width can be considered separately by the designer when estimating the performance of a diode in a given circuit.

Certain precautions must be observed when building and using the test circuit of Figure 17.10 for measurements on high speed diodes. The pulse generator must have a fast rise-time. It is particularly important that the 0 to 10% rise-time of the pulse be short to prevent losing part of the stored charge before the voltage has reached the level required to forward bias D2. The pulse generator should have a high output voltage and a low output impedance so that a large reverse current can be forced through the DUT resulting in a minimum amount of stored charge being lost through recombination. Diode D1 should be an ultra-fast recovery type since any charge store on D1 will subtract from Q_S of the DUT. However, the reading for Q_S of the DUT can be corrected if Q_S of D1 is known. Diode D2 must be a diode with fast turn-on, low leakage, a moderately low Q_S, and a high conductance and pulse current capability

to permit the flow of the large reverse current of the DUT. The voltage V_2 should be adjusted at the different measurement condition to maintain the voltage at point A constant. If this is not done a portion of Q_S will be lost owing to the capacitance between point A and ground together with the difference in voltage required at point A to forward bias D2. Likewise the output current meter must have a sufficiently low resistance to avoid an appreciable change in voltage across C2 at the different measurement conditions. In the construction of the test circuit particular care should be taken in minimizing the inductance through C1, the test clips, the DUT, D2, C2, D1, and C3. Typical test conditions for measurement of high speed diodes would be: $f = 100$ kc, $V_p = 10$ volts, $t_p = 100$ nanoseconds, $t_r = 0.3$ nanoseconds, and $I_F = 10$ milliamperes.

The test circuit, the definition of stored charge, and the measurement precautions given above are essentially equivalent to those given in the JS-2 proposed standard on stored charge, and in method 4062 of MIL-STD-750.

For a given type of diode the stored charge is directly related to the effective lifetime, τ, and to the reverse recovery time in a given test circuit with a given set of test limits. The relationship between stored charge and effective lifetime for the 1N3605, 1N4152 family of diodes is given by $\tau \cong 1.5\ (Q_S/I_F)$, where I_F is the current at which Q_S is measured or specified. Using this relationship and the curves given in Figure 17.8 it is possible to predict the reverse recovery time from the stored charge value. For example, assume a 1N3605 diode has a stored charge of 35 picocoulombs measured at $I_F = 10$ ma and it is desired to determine the reverse recovery time, t_{rr}, for $I_f = 10$ ma, $I_{r1} = 10$ ma, and $I_{r2} = 1$ ma. The effective lifetime is

$$\tau = 1.5\ (35/10) = 5.25 \text{ nanoseconds}$$

and from Figure 17.8

$$t_{rr} = 0.57\tau = 3.0 \text{ nanoseconds}$$

Diode Comparisons and Trade-Offs

As in all designs, the design of a diode to perform a given function requires a series of compromises. An improvement in one parameter is usually accompanied by the deterioration of another parameter. This can be seen in Table 17.2 where the important parameters are shown for a series of diodes with different areas, levels of gold doping, and resistivities. Junction areas of the SD100, SD300, and SD500 are the same, while the junction area of the SD600 and SD800 are twice and fourteen times the area of the SD100, respectively. Gold doping levels for the SD100, SD500, and SD600 are approximately the same, while the SD400 has less; the SD800 is only lightly doped and the SD300 has none. Resistivities of all the diodes are about the same with the exception of the SD500. It has a higher resistivity which increases the breakdown voltage and reduces the capacitance of the diode. This, however, is accomplished at the expense of the reverse recovery time.

Notice that the SD300 which has no gold doping has a much lower leakage current than the SD100 and a higher conductance; however, it has a slightly larger capacitance and a much higher reverse recovery time.

The increasing conductance of the SD600, SD400, and SD800 is due to the increasing areas of these diodes. The price paid for this is an increase in capacitance and recovery time. Because of the successive lighter levels of gold doping used as the device area is increased, the leakage current of these devices does not increase in proportion to the increase in area.

A parameter not shown in Table 17.2 is forward recovery time. However, as was pointed out earlier in this chapter, the forward recovery time may increase as the level of gold doping is increased (reverse recovery lowered) and as the resistivity is increased (breakdown voltage increased).

DEVICE	SD100	SD500	SD300	SD600	SD400	SD800	UNITS
Junction Area	A	A	A	2A	5.7A	14A	
Gold	Yes	Yes	No	Yes	Yes	Yes*	
Resistivity	Mod.	High	Mod.	Mod.	Mod.	Mod.	
Breakdown Voltage	60-90	90-160	60-90	60-90	60-90	60-90	volts
Max. Leakage Currents @ 30 volts, 25°C	30	30	0.1 at 10V	50	50	50	nano-amps
Capacitance at 0 volts	1-2	0.6-1.4	2-4	2-5	4-9	15-30	pico-farads
Reverse Recovery Time t_{rr} ($I_R = I_F = 10$ ma, recovery to 1 ma)	2-4	3-5	100	2-4	6-10	10-18	nano-seconds
Conductance I_F at $V_F = 1$ volt @ 25°C	100	100	150	250	500	900	milli-amperes
JEDEC Registered Types	1N3604-68 1N4009 1N4154	1N914 1N914B 1N916		1N3600 1N4150			

*Lightly doped

COMPARISON OF DIODE CHARACTERISTICS
Table 17.2

DIODE ASSEMBLIES

PEP silicon diodes are available in matched pairs and matched quads for use in applications where close matching in the forward characteristics is required. These units are sealed in small epoxy packages to preserve the identity of the diodes and minimize temperature differentials between diodes. The diodes used in these assemblies have all of the high performance capabilities of the standard PEP silicon diodes, and in addition are matched within very tight limits for V_F over a range of forward currents and over a wide temperature range. V_F's are matched to better than 10 mv (3 mv typical) from 100 μa to 10 ma and to better than 20 mv from 10 ma to 50 ma over the entire temperature range of $-55°$C to $+125°$C. Further, diode pellets can be assembled into any configuration in multi-leaded TO-5, TO-18, and flat packages. The degree of matching V_F for pairs or quads of pellets can be as good or better than obtained with the diode assemblies already discussed.

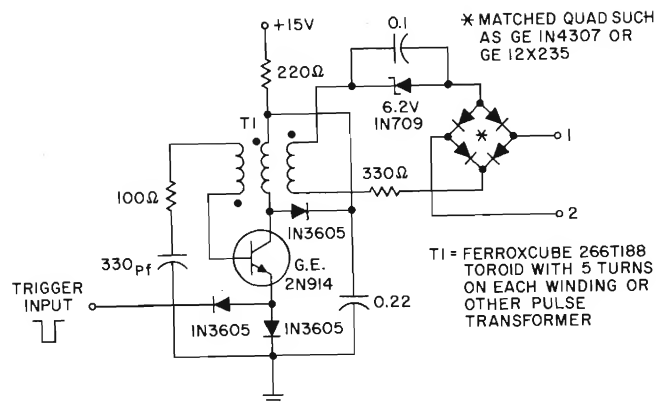
An example of the application of a diode matched quad in a sampling bridge circuit is shown in Figure 17.11. A negative pulse at the input will trigger the blocking oscillator generating a pulse approximately 100 nanoseconds wide. The pulse at the output winding will forward bias the diodes in the bridge with a current of approximately 20 milliamperes. This produces the effect of a closed contact between terminals 1 and 2 with a typical impedance of 5 ohms, and a typical offset voltage of less than 2 millivolts. Between pulses the bridge diodes are reverse biased by the charge on the 0.1 μfd capacitor, and the equivalent impedance between terminals 1 and 2 is typically 1000 megohms.

DIODE SAMPLING BRIDGE WITH BLOCKING OSCILLATOR DRIVING CIRCUIT

Figure 17.11

STABISTORS

Stabistors are single or multi-pellet diodes which have tightly controlled forward voltage characteristics and which are always used in a forward biased condition. Two examples of the multi-pellet stabistor (or low voltage reference diode) are the 1N4156 and 1N4157. The 1N4156 contains two diode pellets in a single glass package while the 1N4157 contains three diode-pellets in a single glass package. Both have a tightly controlled V_F characteristic over an I_F range of .01 to 100 ma. Stabistors are used as low voltage regulator diodes, as amplifier non-linear bias elements, and as a level shifting diode in diode-transistor logic circuits such as shown in Figure 17.12. When the multi-pellet stabistor is used as a low voltage regulator, the temperature coefficient of the stabistor will be larger than a breakdown diode of comparable voltage. However, this is offset by the stabistor's tighter initial tolerance, lower dynamic impedance, and absence of noise at low currents.

DC LEVEL SHIFTING DIODE IN DIODE TRANSISTOR LOGIC

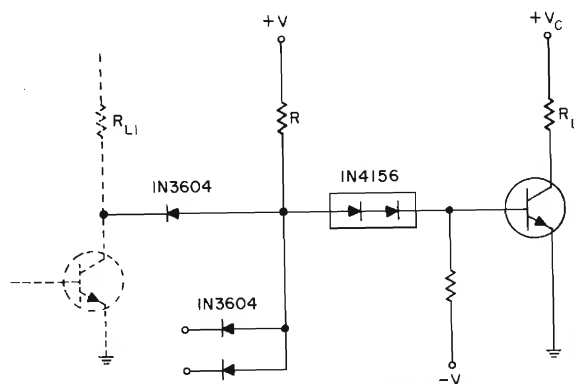



Figure 17.12

SNAP DIODES

The normally undesirable recovery characteristics of a conventional diode are improved and controlled in the snap diode. This results in a device ideally suited for highly efficient harmonic generators and pulse generators with extremely short transition times.

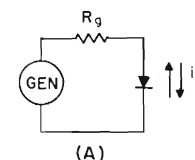
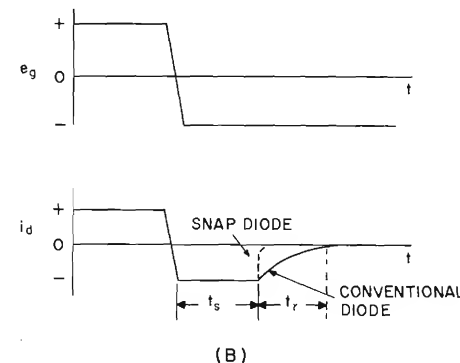
Under conditions of forward bias the diode will store a finite amount of charge. The amount stored is primarily dependent upon the lifetime of the material and the magnitude of the forward current. If the diode is suddenly reverse biased, after having been forward biased, it will conduct in the reverse direction for a finite time until all carriers stored in the diode have been removed as shown in Figure 17.13. The length of time the reverse current flows (storage time) is a function of the initial charge stored, the diode lifetime, and the amount of reverse current. As soon as the stored charge at the junction goes to zero, the diode begins to turn off. A well designed snap diode will turn off linearly as shown in Figure 17.13. This is in contrast to the complex error function turn-off characteristic of a conventional high-speed planar epitaxial diode.

REVERSE RECOVERY OF A DIODE

Figure 17.13

Turn-off or snap-off time is a function of carrier gradient at the junction, diode capacitance, package inductance, initial charge stored, and loop impedance. It is therefore difficult for the circuit designer to calculate the turn-off time. Circuit and package inductances and capacitances should be minimized, however, and the loop impedance adjusted to minimize the turn-off time. (If the impedance is too low, the L/R time constant becomes too large, while if it too large, the RC time constant predominates.)

Turn-off time is generally given on the specification sheet for a particular set of forward and reverse currents. Thus, the SSA550 and SSA551 snap diodes have a maximum snap-off time of 0.5 nanoseconds for a forward current of 1 ma and a reverse current of 20 ma. Snap-off time may be limited by the package, circuit, or test

equipment. For example, the SSA552 and SSA553 have a typical snap-off time given as 0.2 nanoseconds. This figure is probably limited by the package inductance and test equipment available at the time of measurement. For extremely short snap-off times, the SSA556 and SSA557 should be used since these units have a "pill" package construction with only 0.15 nanohenries of inductance. They have been tested in strip line circuits where the snap-off time has been measured as 0.1 nanoseconds using a sampling scope of 0.1 nanosecond rise-time.

While it is difficult to predict the snap-off time, the charge stored during forward bias and the storage-time under reverse bias conditions are easily calculated. The charge stored can be obtained by solving the charge continuity equation

$$\frac{dQ}{dt} = i_d - Q/\tau \qquad (17i)$$

where i_d is the conduction current across the junction and τ is the recombination lifetime.

For the case of a rectangular supply voltage with the shunt and series circuit of Figure 17.14, the stored charge becomes.

$$Q_f = \tau\left(i_f - \frac{V_d}{R}\right)\left(1 - e^{-t_f/\tau}\right) \qquad (17j)$$

where

$$i_f = \frac{e_g}{R_g}$$

and

$$R = \frac{R_g R_L}{(R_g + R_L)} \text{ for the shunt circuit;}$$

and

$$i_f = \frac{e_g}{R_g + R_L}$$

and

$R = R_g + R_L$ for the series circuit. If $t_f >> \tau$ the stored charge becomes

$$Q_f = \left(i_f - \frac{V_d}{R}\right)\tau \qquad (17k)$$

The storage-time, t_s, is also obtained by solving equation (17i) for the charge recovered under reverse bias conditions.* The charge thus recovered is

$$Q_r = \tau\left(i_r + \frac{V_d}{R}\right) - Q_f e^{-t/\tau} \qquad (17l)$$

where

$$i_r = \frac{e_r}{R_g} \text{ for the shunt circuit;}$$

and

$$i_r = \frac{e_r}{(R_g + R_L)} \text{ for the series circuit.}$$

When Q_r goes to zero the diode snaps off so that the storage-time t_s is obtained from equation (17l) as

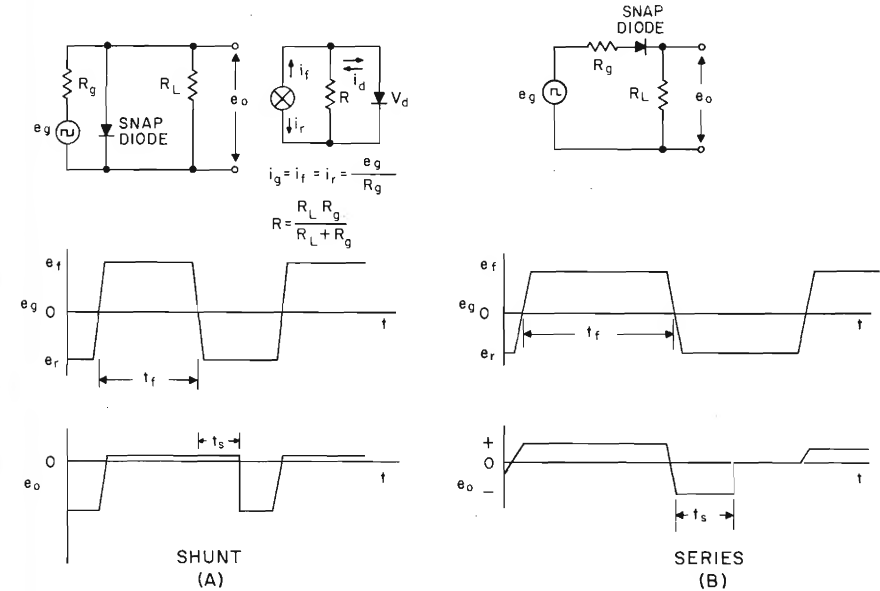
$$t_s = \tau \ln\left[\frac{Q_f}{\tau\left(i_r + \frac{V_d}{R}\right)}\right] \qquad (17m)$$

The series circuit provides a convenient method of measuring the diodes lifetime. If the forward bias current is applied for a time much larger than the diodes lifetime, and the reverse current is of sufficient amplitude that the storage-time is much less

*Because of the method of manufacture, over 95% of the charge is recovered during the storage time. This is not true for a conventional diode.

than the lifetime, then the lifetime can be calculated to be

$$\tau = \left(\frac{i_{Lr}}{i_{Lf}}\right) t_s \qquad (17n)$$

Thus it is only necessary to measure the two currents and the storage-time to calculate the lifetime.

SHUNT (A)

SERIES (B)

SERIES AND SHUNT CIRCUIT WITH RECTANGULAR SUPPLY
Figure 17.14

If a sinusoidal supply is used with a rectangular and dc current, then the charge stored for the series and shunt circuit of Figure 17.15 is

$$Q_f = \tau\left(i - \frac{V_d}{R}\right)\left(1 - e^{-\pi/\omega\tau}\right) + \frac{\omega I_{Mf}}{\left(\frac{1}{\tau}\right)^2 + \omega^2}\left(1 + e^{-\pi/\omega\tau}\right) \qquad (17o)$$

where

$$R = \frac{R_g R_L}{(R_g + R_L)}$$

and

$$I_{Mf} = \frac{E_{Mf}}{R_g} \text{ for the shunt circuit;}$$

and

$$R = R_g + R_L$$

and

$$I_{Mf} = \frac{E_{Mf}}{R_g + R_L} \text{ for the series circuit.}$$

For the case where $\pi/T << \omega$, then the charge stored becomes

$$Q_f = 2\, I_{Mf}/\omega \qquad (17p)$$

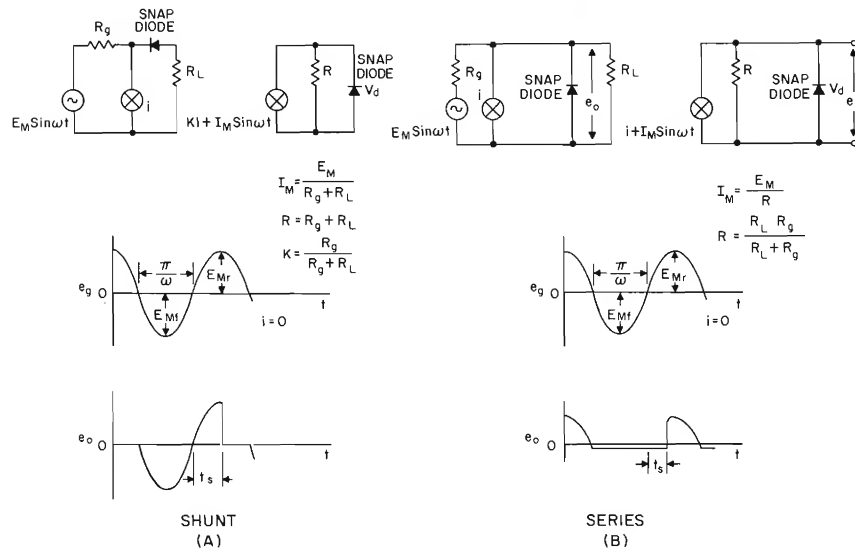
SHUNT (A) SERIES (B)

SERIES AND SHUNT CIRCUITS WITH SINEWAVE SUPPLY

Figure 17.15

The charge recovered during the half cycle of reverse bias becomes

$$Q_R = \left(\tau K i_r + \frac{\tau V_d}{R} + Q_f - \frac{\omega I_{Mr}}{(1/\tau)^2 + \omega^2}\right) e^{-t/\tau} - \tau K i_r - \frac{\tau V_d}{R}$$

$$- \frac{I_{Mr}\sin\omega t}{\tau\left[\left(\frac{1}{\tau}\right)^2 + \omega^2\right]} + \frac{\omega I_{Mr}}{\left(\frac{1}{\tau}\right)^2 + \omega^2}\cos\omega \qquad (17q)$$

where

$K = 1$ for the shunt circuit and

$K = \frac{R_g}{(R_L + R_g)}$ for the series circuit. If $\pi/\omega << \tau$ then

$$Q_R = Q_f - I_{Mr}/\omega\ (1 - \cos\omega t) \qquad (17r)$$

Equations (17p) and (17r) can be combined to give the snap off angle

$$\theta = \cos^{-1}(1 - 2\, I_{Mf}/I_{Mr})$$

If the peak forward and reverse currents are equal, $\theta = 180°$. Some form of self bias or different values of current must be used if the diode is to snap off before reaching 180°. On the other hand if the above inequality does not hold, then the diode will snap off at some angle before 180° even if the forward and reverse peak currents are equal.

Because of a larger lifetime (20-100 nanoseconds) the SSA550, SSA551, SSA554, and SSA555 should be used when the frequency is roughly below 100 mc. The reason is that a larger charge can be stored during the half cycle of forward bias which in turn allows a larger reverse peak current. Above about 100 mc it is desirable to use the SSA552, SSA553, SSA556 and SSA557 with lifetimes of 1-5 nanoseconds, otherwise all the stored charge might not be removed during the time of reverse bias without an excessively high peak reverse current.

Figure 17.16 shows a simple pulse generator which utilizes a sinusoidal supply and a shunt-series circuit. The pulse width and its phase relationship with the 50 mc

source are adjustable by means of the dc voltages. The rise and fall times are probably inductance limited. The construction details, together with other configurations are given in Reference 6.

H = 2 nsec/CM
V = 0.5 V/CM

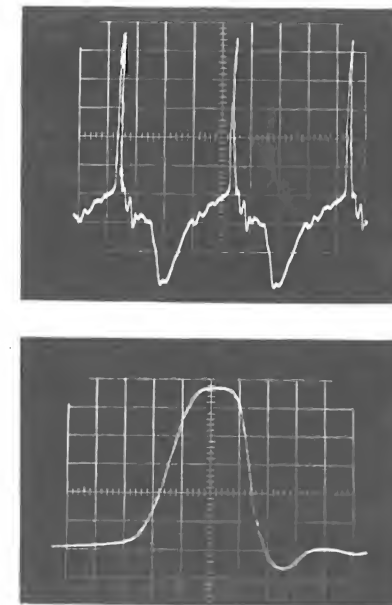
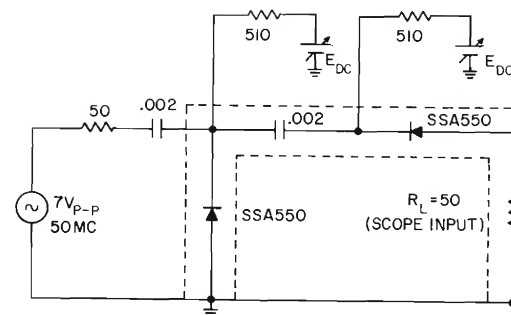
H = 2 nsec/CM
V = 0.5 V/CM

TIME →

SHUNT-SERIES PULSE CIRCUIT RESPONSE

Figure 17.16

REFERENCES

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[2] Gutzwiller, F.W., Sylvan, T.P., "Power Semiconductor Ratings Under Transient and Intermittent Loads," General Electric Application Note 200.9.

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[4] Ko, W.H., "The Reverse Transient Behavior of Semiconductor Junction Diodes," *IRE Transactions, ED-8,* March 1961, pp. 123-131.

[5] Giorgis, J., "The Logarithmic and Temperature Coefficient Characteristics of the 1N3605 and 1N3606 Diode," General Electric Application Note 90.47.

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NOTES

TRANSISTOR MEASUREMENTS

CHAPTER 18

INTRODUCTION

Accurate measurements demand a thorough knowledge of measurement principles and pitfalls. To simplify these measurements, such that they are non-discretionary go-no go types, requires in addition, prior information about the device characteristics and their probable distribution. Transistor measurements in particular, due to the extreme power sensitivity of *signal* transistors and the *active amplifier* nature of the device, impose great demands on the skill and ingenuity of the test-equipment designer.

To obtain precision and accuracy in transistor measurements, not only must the definition, meaning, and limits of each test be considered (as well as the actual measurement methods), but attention must also be given to the effect of the measurement upon the device. To illustrate: the transistor is a non-linear device and under normal dc bias conditions the emitter-base voltage drop in a germanium transistor is about 250 millivolts. If linear (small-signal) measurements are to be made, it becomes obvious that the rapid curvature of the forward-biased diode characteristic precludes the usual "one order of magnitude less" argument normally applied to signal/bias relationships for small-signal measurements and demands even smaller peak-to-peak signal excursions.

In addition, the transistor is a current amplifier and the effect of the input signal on the output current must be considered. Thus, prior knowledge of probable input impedance and device current gain becomes necessary. For example, assuming an ideal transistor at low frequency and neglecting parasitics, in measuring h_{ie}

$$h_{ie} = \frac{e_b}{i_b}\bigg|_{e_c = 0} \qquad \text{and } h_{fe} = \frac{i_c}{i_b}\bigg|_{e_c = 0}$$

then,

$$i_b = \frac{e_b}{h_{ie}} \text{ and } i_c = h_{fe}\, i_b$$

from the theory (see any basic transistor text) $h_{ie} = \dfrac{r_e}{(1 - \alpha_o)} \cong h_{fe}\, r_e$

$$\left(\text{since } h_{fe} = \frac{\alpha_o}{(1 - \alpha_o)}\right) \text{ so that } i_c = \frac{e_b}{r_e};$$

also, $r_e = \dfrac{KT}{qI_E}$ (see any basic transistor text) where K = Boltzmann's constant, T = temperature in degrees Kelvin, and q is the charge of the electron. Now, $\dfrac{KT}{q} = 26 \times 10^{-3}$ volts at room temperature; and, assuming

$$I_C = I_E \text{ (within 10\%)}$$

$$r_e = \frac{26 \times 10^{-3}}{I_C}$$

i_c is very much less than I_C, (say $i_c = 0.1\ I_C$) for small signal measurements.

Then,

$$i_c = 0.1\ I_C = \frac{e_b}{r_e} = \frac{e_b\ I_C}{26 \times 10^{-3}}$$

or,

$$\frac{e_b\ I_C}{26 \times 10^{-3}} = 0.1\ I_C \text{ whence } e_b \leqq 26 \times 10^{-4}$$

so that the maximum signal swing, e_b, should be in the order of 2.5 millivolts and is largely independent of gain or collector current. However, when the transistor is driven from a current source it is seen that since

$$e_{b\,max} = i_{b\,max}\ h_{ie},$$

then

$$i_{b\,max} = \frac{e_{b\,max}}{h_{ie}}$$

or,

$$i_{b\,max} = \frac{e_{b\,max}}{h_{fe}\ r_e} \cong \frac{25 \times 10^{-4}}{h_{fe\,max} \times \frac{25 \times 10^{-3}}{I_C}}$$

whence,

$$i_{b\,max} = \frac{I_C}{10\ h_{fe\,max}}$$

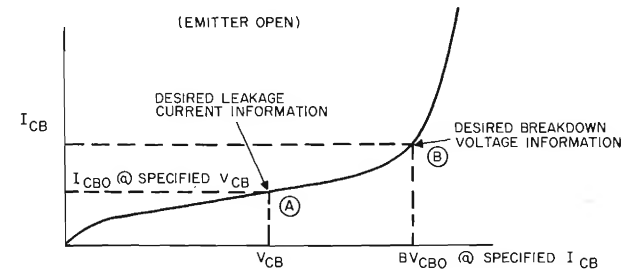
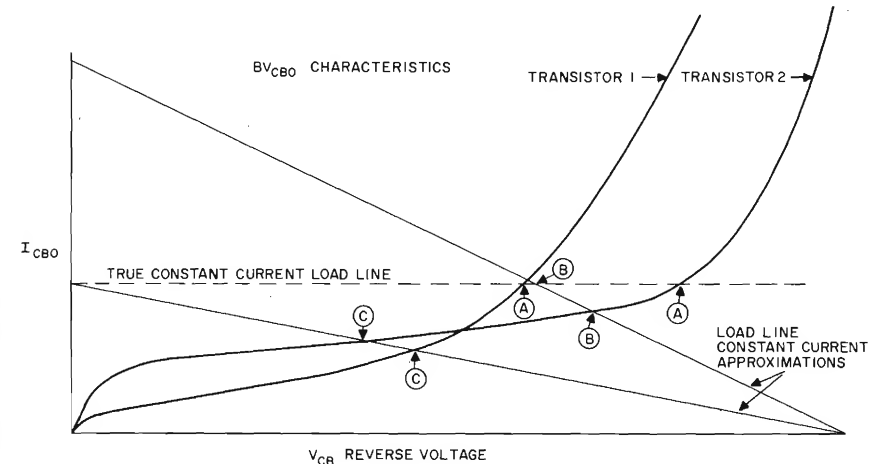
Here a knowledge of the probable range of h_{fe} expected is quite important. Thus, depending upon whether a current source or a voltage source is used in small signal measurements, care must be exercised to insure that small signal conditions truly exist.

REVERSE DIODE CHARACTERISTICS

General

I_{CO} or I_{EO} are the leakage currents within the safe operating region of reverse voltage and are intended to yield comparative, evaluative information as to permissible operation, surface condition and temperature effects on operation.

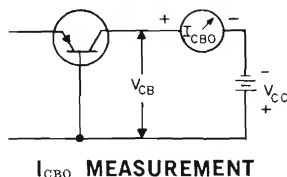
The breakdown voltage tests are indicative of the maximum voltage that can be applied to the device and serve to indicate the voltage at which "avalanche-breakdown" and "thermal-runaway" take place.

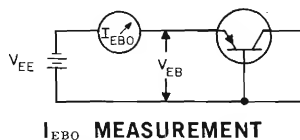
The curves of Figures 18.1 and 18.2 are arbitrary but representative ones for transistors and are included to explain what some of the reverse diode characteristic tests mean, and the points at which they are taken. In Figure 18.1, the collector to base reverse voltage of a transistor versus the leakage current is displayed; the points of interest are point A, the leakage current (I_{CBO} in this case) at a specified collector to base junction voltage, and point B, the breakdown voltage (BV_{CBO} in this case) at a specified leakage current. Figure 18.2 illustrates some points which must be considered when accurate breakdown voltage measurements are desired. The two transistors shown have different reverse voltage characteristics. The load line of the measuring instrument which is to approximate a constant current source may give slightly or grossly erroneous readings if care is not exercised in measurement technique. The true values of breakdown voltage are shown at points A. The slightly erroneous readings are at points B on the two characteristic curves while the grossly erroneous data is at points C.

REPRESENTATIVE COLLECTOR-BASE JUNCTION REVERSE CHARACTERISTICS
Figure 18.1

BV_{CBO} MEASUREMENT TECHNIQUES
Figure 18.2

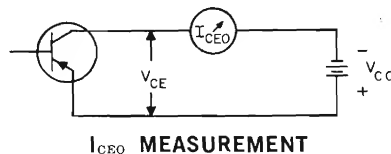
DC TESTS

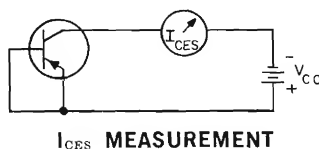
The following abstracts include the definitions of particular tests and the associated simplified circuits. The current measuring (I_{CBO}, I_{EBO}, etc.) circuits are discussed in more detail in the next section.

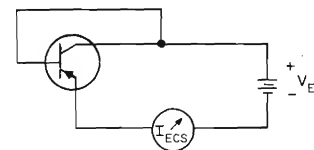
1. I_{CBO}, commonly called I_{CO}, is the dc collector current which flows when a specified voltage, V_{CBO}, is applied from collector to base, the emitter being left open (unconnected). The polarity of the applied voltage is such that the collector-base junction is biased in a *reverse* direction. (Collector is negative with respect to the base for a PNP transistor.)

   I_{CO} is greatly dependent on temperature and in some instances, transistors must be handled with gloves to prevent heating the transistor by contact with the operator's hand.

I_{CBO} MEASUREMENT
Figure 18.3

2. I_{EBO}, commonly called I_{EO}, is the dc current which flows when a specified voltage is applied from emitter to base, the collector being left open (unconnected). The polarity of the applied voltage is such that the emitter-base junction is biased in a reverse direction. (Emitter is negative with respect to the base for a PNP transistor). I_{EO} also is greatly dependent on the temperature and the same precautions apply as for I_{CO} determination.

I_{EBO} MEASUREMENT
Figure 18.4

3. I_{CEO} is the dc collector current which flows when a specified voltage is applied from collector to emitter, the base being left open (unconnected). The polarity of the applied voltage is such that the collector-base junction is biased in a reverse direction. (Collector is negative with respect to the emitter for a PNP transistor.) I_{CEO} is greatly dependent on temperature and the operator should use gloves when handling transistor before measuring.

I_{CEO} MEASUREMENT
Figure 18.5

4. I_{CES} is the dc collector current which flows when a specified voltage is applied from collector to emitter, the base being shorted to the emitter. The polarity of the applied voltage is such that the collector-base junction is biased in a reverse direction. (Collector is negative with respect to the emitter for a PNP transistor.)

I_{CES} MEASUREMENT
Figure 18.6

5. I_{ECS} is the dc emitter current which flows when a specified voltage is applied from emitter to collector, the base being shorted to the collector. The polarity of the applied voltage is such that the emitter-base junction is biased in a reverse direction. (Emitter is negative with respect to the collector for a PNP transistor.)

I_{ECS} MEASUREMENT
Figure 18.7

6. BV_{CE} Tests—BV_{CEO}, BV_{CER}, BV_{CES}, BV_{CEV}

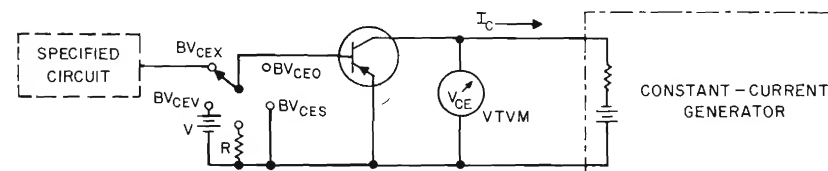
A BV_{CE} test is a measurement of the breakdown voltage of a transistor in the common emitter configuration. For the measurement to be meaningful, a collector current *must* be specified.

(NOTE: BASE CONTACT IS S POSITION SWITCH)

Figure 18.8

In measuring BV_{CE} breakdown voltages, a constant value of collector current, I_C, is caused to flow in the reverse direction (collector is negative with respect to the emitter for a PNP transistor) and the collector to emitter voltage, V_{CE}, is read on the meter. This voltage reading is the BV_{CE} breakdown voltage required.

In addition to a collector current specification, the condition of the base lead must be specified.

a. BV_{CEO} is the common emitter breakdown voltage (for a specified collector current, I_C) when the base is left open (unconnected).

b. BV_{CER} is the common emitter breakdown voltage (for a specified collector current, I_C) when a resistor of a *specified* value, R, is connected from the base to the emitter.

c. BV_{CES} is the common emitter breakdown voltage (for a specified collector current, I_C) when the base is shorted to the emitter.

d. BV_{CEV} is the common emitter breakdown voltage (for a specified collector current, I_C) when the base is biased with a voltage with respect to the emitter.

e. BV_{CEX} is the common emitter breakdown voltage (for a specified collector current, I_C) when the base is terminated through a specified circuit to the emitter.

It should be strongly emphasized that BV_{CE}, by itself, is meaningless unless: a collector current is specified, the condition of the base lead is specified (by the use of a third subscript), and, if the measurement is for BV_{CER} or BV_{CEV}, a definite resistor, R, or a definite voltage, V, are specified, or for BV_{CEX} a definite circuit is specified.

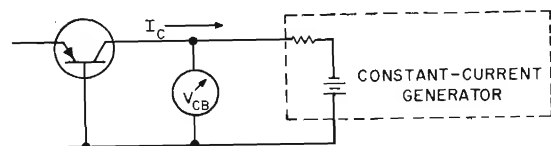
7. BV_{CBO} is a measurement of the breakdown of the collector-base junction with the emitter open. A collector current, I_C, must be specified.

BV_{CBO} MEASUREMENT

Figure 18.9

The emitter is left open (unconnected) as specified by the third subscript. A collector current, I_C, is caused to flow through the collector-base junction and the voltage drop V_{CB} is the breakdown voltage, BV_{CBO}. Polarity is such that the collector-base junction is biased in a reverse direction (collector is negative with respect to the base for a PNP transistor).

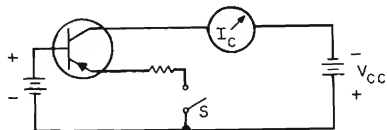
8. V_{RT} (reach through). Reach through voltage is that voltage which, when applied from the collector to base, causes the collector space charge layer to expand into the emitter junction.

SIMPLE GO-NO GO V_{RT} MEASUREMENT

Figure 18.10

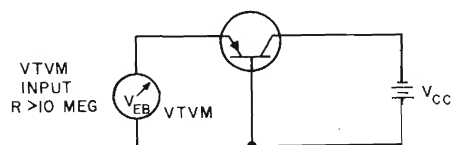
In Figure 18.10, if, when switch "S" is closed, I_C does not increase, the punch through voltage is greater than V_{CC}. Punch through may also be measured by the use of the circuit shown in Figure 18.11.

ALTERNATE GO-NO GO V_{RT} MEASUREMENT

Figure 18.11

If V_{EB} is less than 1 volt, then $V_{RT} > (V_{CC} - 1)$ volts.

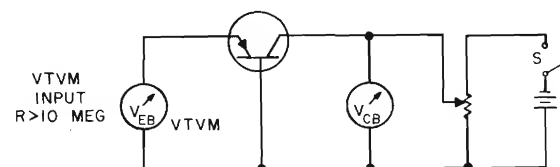
The above V_{RT} tests are go-no go in character. By making V_{CC} variable actual values may be determined; for example, in the circuit shown in Figure 18.12 one can adjust V_{CC} until the VTVM reads 1.0 volt, then V_{RT} equals $V_{CB} - 1$ volts.

V_{RT} MEASUREMENT

Figure 18.12

CURRENT MEASUREMENTS

1. General

In this section the elaboration of the basic circuit into actual test equipment (both qualitative and quantitative) is delineated. The necessity of saving time in measurement is considered of importance; and means that *constant* voltage and *constant* current techniques will be used. (Constant within the accuracy requirements desired.)

Certain problems arise concommitant with *constancy*. A voltage source, by definition, makes it difficult to limit the current through the ammeter in the event of device failure; and current sources have large open-circuit voltages prior to test, which can be damaging to the operator; and, due to circuit capacity, if the device has an extremely short thermal time constant, the unit under test may be damaged from the large instantaneous currents that can flow.

For the above reasons voltage and current "clamps" are resorted to in order to have the required constancy and are discussed, with their limitations, in conjunction with each class of test.

2. Clamp Circuits

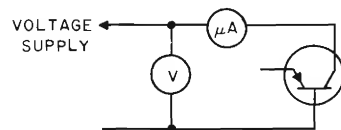
In the circuits shown in Figures 18.13 through 18.16, the measurement of I_{CBO} is accomplished. In Figure 18.13, the basic form of the circuit is shown. There is some error in this simple arrangement in establishing the test voltage conditions since there is a small voltage drop across the meter. Also, if a unit is shorted or has an excessively high leakage current, the microammeter may be damaged. For meter protection the circuit of Figure 18.14 is used. The diode used here is a large area diode which has a reverse leakage current greater than that which is intended to be measured. If a 1N91 is used the maximum leakage current which could be measured would be approximately 10 μa since this is the maximum reverse current which the 1N91 will conduct when a small reverse voltage is impressed across it. To avoid this current limitation and still protect the microammeter the circuit shown in Figure 18.15 is used. This circuit is basically a form of bridge so that if the drop through the limiting resistor is not enough to bring the reference point (the collector) below the clamp voltage, current flows through the diode and the voltage at the reference is that of the clamp supply less the forward drop in the diode.

BASIC I_{CBO} CIRCUIT

Figure 18.13

I_{CBO} CIRCUIT WITH METER PROTECTION

Figure 18.14

When the drop through the limiting resistor exceeds the allowed value, the current through the diode tries to reverse; thereupon, the diode becomes back biased and the reference point is driven by a current source, where $I_{limit} = V_{protection}/R_{reference}$ (which is considered a fault condition, but meter protection is accomplished by this current limiting).

Since the current under fault conditions is greater than the desired limit (and it is desired to keep the overload on the ammeter as small as possible) it is desirable to make the protection voltage much larger than the clamp voltage; preferably 10 times larger. The reverse current of the clamp diode at the clamp voltage must be considered, for it adds to the meter overload, and must have a breakdown voltage much greater than the clamp supply. When the currents that are being measured are appreciable (in the order of milliamps) the additional currents flowing through the reference (clamp) supply must be considered. Thus if 1 MA is the limiting current allowed, the clamp bleeder should carry much greater currents (>10 MA) so that the clamp voltage does not change. Where the test voltage is fairly low the drop through the ammeter or reading resistor must be considered for this subtracts from the supply to the tested device.

The go-no go test equipment of Figure 18.16 is designed to indicate only that the device possesses specified, or better, characteristics. Generally this type of equipment is designed individually for each requirement and has only limited flexibility.

COMPLETE I_{CBO} TEST CIRCUIT

Figure 18.15

GO-NO GO I_{CBO} TEST CIRCUIT

Figure 18.16

From the Figure 18.16 circuit go-no go BV_{CBO} tests can be made by using a current source whose value is that at which BV_{CBO} is defined. In this case the V_{CB} voltmeter will indicate that the voltage is less than (I_{CBO} is excessive), equal to, or greater than the required test BV_{CBO} voltage (I_{CBO} is less than the allowed current limit). The current for the voltmeter must be considered, and its accuracy at the limit point (V_T) must be checked to put the reject-line on the meter at the correct point. Once this has been done the readings are as accurate as the initial calibration and the stability of the power supply. To prevent overloading the voltmeter and to avoid the large open-circuit voltages at the test point, the current source is often voltage-clamped where the desired test voltage is less than that of the clamp. When this is done the circuit bears a close resemblance to the I_{CBO} test circuit of Figure 18.16.

LARGE-SIGNAL (DC) TRANSISTOR CHARACTERISTICS

The large-signal transistor characteristics may be divided into two categories with the line of demarcation being the difference between high-frequency pulse response and the dc parameters useful in control-circuit and some computer applications. The pulse response characteristics are discussed in a later section.

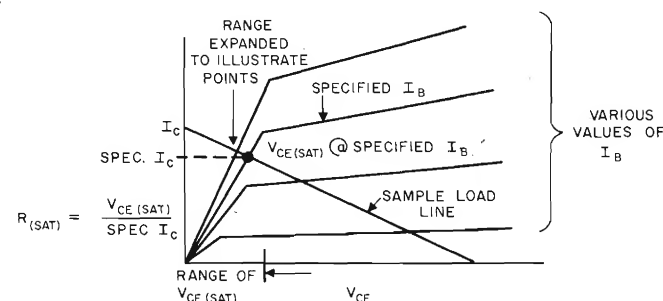
In the following curves Figures 18.17 and 18.18, the significant points of interest are described on the transistor family of curves where I_C vs. V_{CE} is plotted for various I_B values.

$V_{CE(SAT)}$ AND $R_{(SAT)}$ — FUNCTIONS OF I_B AND I_C

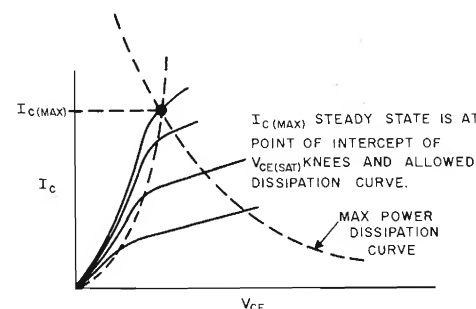
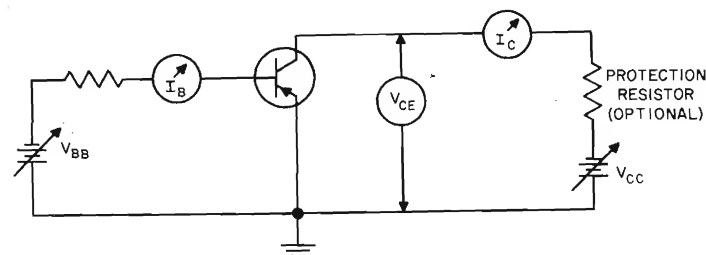
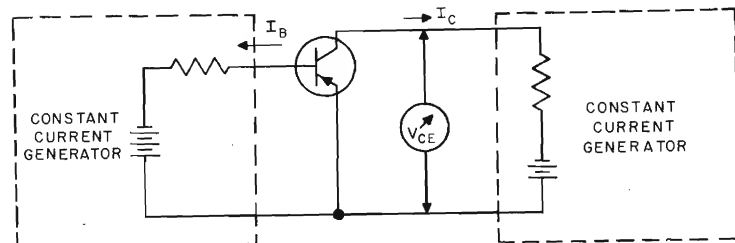
Figure 18.17

$I_{C(MAX)}$ STEADY STATE

Figure 18.18

LARGE SIGNAL DEFINITIONS AND BASIC TEST CIRCUITS

1. h_{FE} is the static value of the forward transfer current gain in the common emitter configuration and is measured as shown in Figure 18.19. It is the dc collector current, I_C, divided by the dc base current, I_B; $h_{FE} = \frac{I_C}{I_B}$.

h_{FE} MEASUREMENT
Figure 18.19

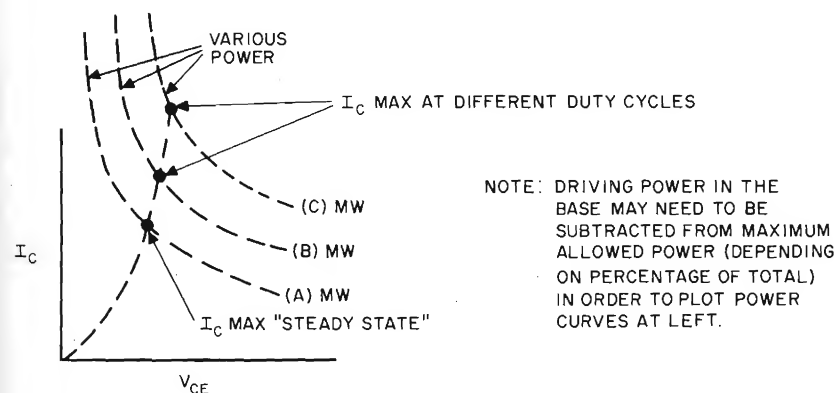
The collector voltage, V_{CE}, and the collector current, I_C, must be specified. A go-no go test for h_{FE} may be used, as shown in Figure 18.20.

GO-NO GO h_{FE} CIRCUIT
Figure 18.20

In the method shown in Figure 18.20, I_B is adjusted to give the base current required for an h_{FE} of the required value, I_C is adjusted to the specified value

$$I_B = \frac{I_C}{h_{FE}}.$$

If V_{CE} as read on the meter is less than that given in the test specifications, then the h_{FE} for the transistor is greater than that required. If V_{CE} is greater than the value specified, then h_{FE} is less than the required value.

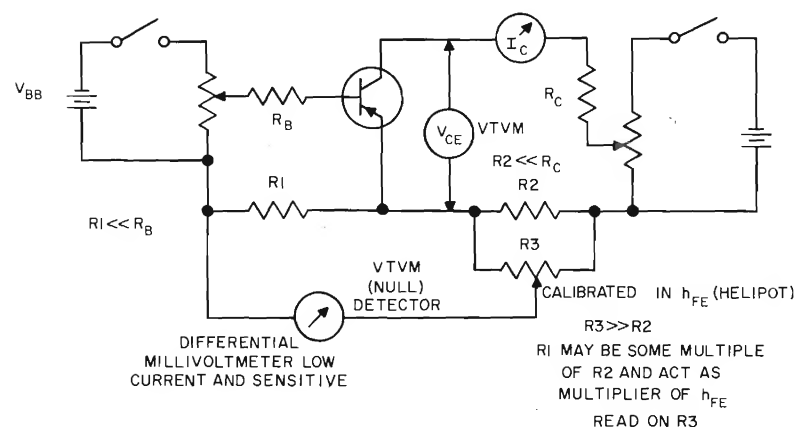
2. $V_{CE\,(SAT)}$ is the voltage from collector to the emitter, V_{CE}, for a given I_C and I_B while biased in the collector saturation region. The test is very similar to that for h_{FE} in Figure 18.20. I_C and I_B are adjusted to their specified values and V_{CE} as read on the meter connected from collector to emitter is $V_{CE\,(SAT)}$.

3. V_{BE} is a measurement of the base to emitter voltage, V_{BE}, when in the common emitter configuration and biased according to instructions given in the test specifications. A circuit similar to Figure 18.20 for h_{FE} may be used with the addition of a voltmeter (VTVM) between base and emitter.
4. h_{IE} is the equivalent (slope intercept) resistance equal to V_{BE}/I_B. This test is generally made at a specific I_B which is sufficient to saturate the device when it is driven by a specified I_C. This information finds maximum applicability in switching and computer applications.
5. h_{IB} is equivalent to h_{IE} except with the transistor operated in a grounded-base configuration. This resistance is an indication of the forward drop in the emitter, and finds application in some power transistor considerations, in bias requirements for some small-signal transistors, and in some regulated power supply applications.
6. $I_{C\,MAX}$ must be considered for two different applications,
   a. Steady state—I_C max. is determined by the intercept of the curve of the "knees" of the collector saturation points with the maximum allowable power dissipation curve.
   b. The second consideration of I_C max. involves the duty-cycle of the *on* times for switching applications and is dependent on the duty cycle of the circuit being used.

$I_{C\,MAX}$ CHARACTERISTICS
Figure 18.21

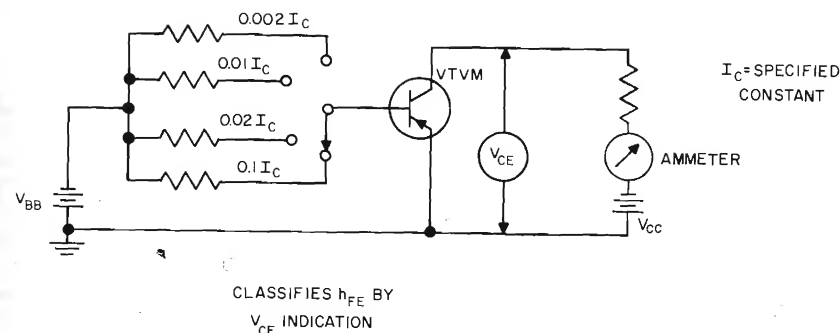
SOME TEST CIRCUITS

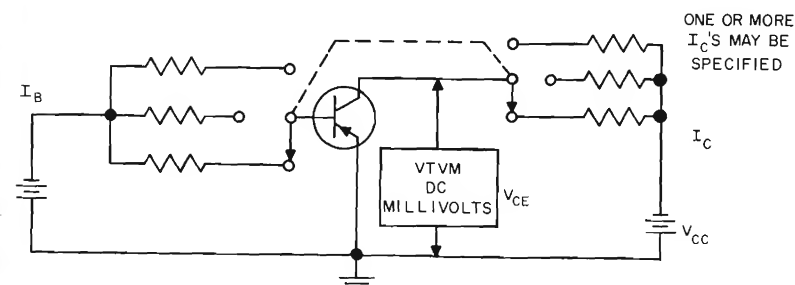
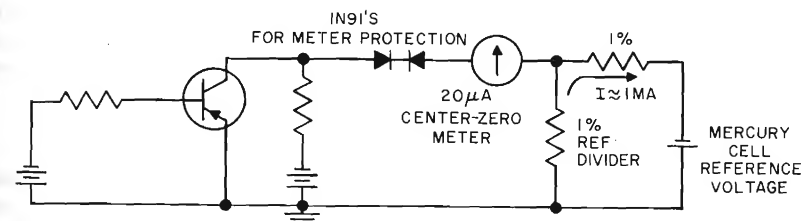
Methods of test and equipment for almost all parameters may be divided into two basic categories: (a) quantitative and evaluative equipment for engineering, and (b) go-no go equipment for use when the limits of allowed variance of a particular parameter have been determined and specified. The equipment required for the engineering measurements of dc parameters consist primarily of precise power (current and voltage) supplies, and reliable and precise (as well as often very sensitive) voltmeters and ammeters. The following section will be devoted to both quantitative and go-no go equipments and circuits in use.

1. h_{FE} measurement is accomplished in the circuit of Figure 18.22. The potentiometers are adjusted in the base and collector circuits to establish the proper measurement conditions; namely, since h_{FE} is a function of both V_{CE} and I_C, these two quantities must be specified. When the desired I_C and V_{CE} conditions are established the h_{FE} can be determined. As has been stated $h_{FE} = I_C/I_B$; thus two current reading resistors, R1 and R2, are inserted into the base and collector circuitry respectively. R1 is made very much smaller than R_B, and R2 is made very much smaller than R_C. Using a Helipot, R3, whose resistance is much larger than R2, the voltage drops across R1 and R2 can be compared. When R1 is equal to R2, for example, and a null is established on the VTVM when the Helipot reads twenty thousandths (20/1000) of full scale then the h_{FE} = 1000/20 or 50. If R1 = 10 R2, a greater range of the Helipot can be used and, in the example above, a null would be established at two hundred thousandths (200/1000) on the Helipot indicating $h_{FE} = 1000/200 \times 10 = 50$. On the physical test equipment the Helipot could be calibrated in h_{FE} for direct reading.

NOTE: IN ALL OF THE h_{FE} AND $V_{CE(SAT)}$ TEST CIRCUITS, IT MAY BE NECESSARY TO "CLAMP" THE BASE AND COLLECTOR SUPPLIES TO PREVENT DAMAGE TO EXTREMELY SENSITIVE AND LOW-POWER UNITS.

QUANTITATIVE h_{FE} MEASUREMENT
Figure 18.22

2. h_{FE} go-no go equipment is normally built using a constant collector current and classifying h_{FE} according to required base current as shown in Figure 18.23. When the desired V_{CE} and I_C measurement conditions are known, a circuit can be built as shown to classify the devices. If V_{CE} reads below the specified measurement condition, the h_{FE} is greater than that established by the fixed resistors and supplies; if the V_{CE} reads higher than that established as a measurement condition, the h_{FE} is lower than that established by the circuit.

3. The $V_{CE(SAT)}$ measurement, Figure 18.24, is often made by applying a specified I_C to the transistor and increasing I_B until an abrupt change in V_{CE} indicates that the collector voltage has dropped below the knee of the collector curve; however, in specifications both I_C and I_B are specified. I_B is usually

h_{FE} CLASSIFIER
Figure 18.23

sufficient to saturate the device; and, in go-no go testing, noting that V_{CE} is below some specified voltage, or that it is within certain specified limits is normal procedure. The latter being of particular importance in computer applications where maximum and minimum $V_{CE(SAT)}$ values are relied upon. Two circuits in which measurements can be performed are shown in Figure 18.24.

IN PLACE OF THE VTVM MILLIVOLTMETER SHOWN ABOVE A REFERENCE (NULL) COMPARATOR MAY BE USED FOR GO-NO GO TESTS:

$V_{CE(SAT)}$ MEASUREMENT
Figure 18.24

JUNCTION TEMPERATURE MEASUREMENTS

JUNCTION TEMPERATURE (T_J)

The measurement of junction temperature, depends on one of two temperature-sensitive mechanisms inherent in the junction device. These are the exponential rise of the reverse diode saturation current, and forward diode voltage decrease with temperature. In most instances experience has shown that calculated theoretical changes of I_{CO} and V_F are too gross (due to rather large "second-order" effects) to be sufficiently accurate indices of junction temperature; and the test device must, in fact, *be calibrated.* This requires that the unit be temperature cycled in an oven (allowing sufficient time for the device to stabilize at each temperature or using a large, high thermal-conductivity heat sink) and a plot of the desired index vs. temperature be made. Power is applied to the device in the forward direction, or through the application of bias current. This power is then momentarily switched off and the built-in *thermometer* checked by a suitably *gated* meter. The *off* time is either kept negligibly small when possible, or else considered in determining the average input power.

Both the I_{CO} and V_F methods are alike in having a large possible error due to the thermal response-time of the device. If the temperature at the junction declines rapidly, the resultant apparent value of T_J will be lower and fall somewhere between the true T_J and that of the thermal mass.

The reverse-current method suffers the additional handicap of charge-storage in the junction when the forward current is reversed. This charge must be swept out by the reverse voltage before a true indication of I_{CBO} can be obtained, a race between charge and thermal decays results. In the large area device of relatively small effective lifetime, the error will probably not be large, but the current metering system must be gated to prevent the charge-decay currents from registering. No peak-reading detectors can be used; although if the charge decays rapidly enough compared to the measuring time, and T_J is reasonably constant during this interval; an average reading metering system is sufficiently accurate, if suitably calibrated.

In the case of the small-area, long lifetime device the problem is more difficult. The masking effect here precludes reverse measurements and only forward measurements are feasible; there are still storage problems, but switching presents the major difficulty. Fast-acting mercury relays are generally used to prevent contact bounce and carry the required currents without large contact drops.

There are decided advantages to using forward voltage drop as the T_J index from the point of view of the circuit requirements. Since the detector (meter) circuit is driven by a voltage source the system is less liable to pick up extraneous hum that can plague the reverse-current measurements. (Particularly when I_{CBO} is low, as in silicon devices, where the current reading resistor is necessarily large.) Unfortunately, however, the change of V_F is comparatively small and the "thermometer" is therefore relatively insensitive. This may require differential amplifier techniques in the detector circuit for precise measurements of T_J.

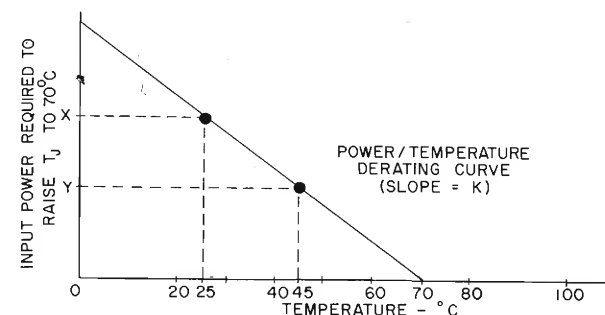
THERMAL IMPEDANCE

Once a means of measuring T_J has been developed, the measurement of thermal impedance is readily accomplished. The simplest means of measuring the case temperature — such as a thermocouple or large heat sink — may be used, and different powers are fed into the transistor while measuring T_J. By defining thermal resistance as the input power required to raise T_J to some arbitrary temperature, (say 70°C) and measuring this power at different ambients, sink or case temperatures, we may write the following definition:

if x watts = 70°C T_J from 25°C T_{sink}
and y watts = 70°C T_J from 45°C T_{sink}

Then,

$$R_{thermal} = \frac{45° - 25°}{x\text{-}y \text{ watts}} = \frac{20}{x\text{-}y} \text{ °C per watt}$$

we can draw a derating curve through these intercepts as shown in Figure 15.25

POWER VS. TEMPERATURE DERATING CURVE
Figure 18.25

TEST CIRCUIT FOR JUNCTION TEMPERATURE MEASUREMENTS

1. Description of Operation

Under certain conditions, the forward drop of a semiconductor junction varies linearly with temperature. By setting up these conditions and using a test circuit similar to that of Figure 18.26, it is possible to determine the temperature of a transistor collector junction for various power dissipations in the transistor.

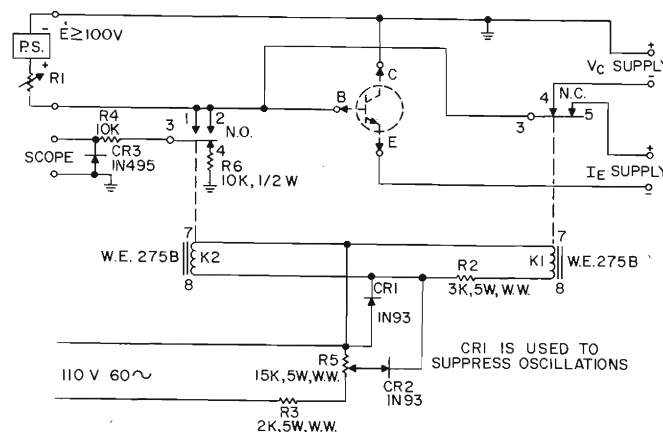
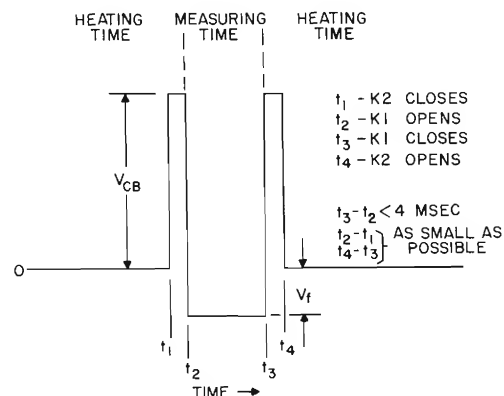



Figure 18.26 THERMAL MEASUREMENTS TEST CIRCUIT

The circuit shown is one of several variations which can be used. K1 is a mercury relay (W. E. 275 B type) which interrupts the circuit in which the transistor is heated. K2 is another relay of the same type that puts the transistor in a temperature measuring circuit when it is not in the heating circuit. The relays operate at 60 cps. The transistor under test is heated for about 80% of the time and its forward drop (temperature) measured during the other 20%. If the scope were put directly on contact No. 3 of K2, the presentation would be similar to that shown in Figure 18.27.

OSCILLOSCOPE PATTERN
Figure 18.27

In this presentation, V_f is the forward drop of the collector junction while it is in the measuring circuit, and V_{CB} is the collector to base voltage while in the heating circuit. The scope vertical amplifier is normally set to the range that will best show the variations in V_f. Under this condition, V_{CB} is of such magnitude that it would overdrive the scope and cause distortion of the V_f presentation. To prevent this situation, a clamp consisting of R4 and CR3, is inserted between the scope and contact No. 3 of K2. This minimizes the possibility of overdriving, but still allows the monitoring of V_f. Since V_f varies linearly with temperature, the changes in junction temperature can be determined by measuring the changes in V_f.

Now, back to the conditions mentioned earlier. The first of these is that the measuring current (I_f) through the junction during the measurement must be held constant. This requirement is met by using a power supply (PS) with V = 100 volts and a high resistance (R1).

Another condition is that I_f be set to such a value that dV_f/dT will be a constant over a wide range of temperature T. Based primarily on calibration tests of several types of transistors, I_f should be adjusted to give a $V_f \approx 500$ mv at 27°C for silicon junctions and a $V_f \approx 200$ mv at 27°C for germanium junctions. This is accomplished by adjusting the value of R1. Once the conditions are met, the final requirement is that the value of dV_f/dT be known.

dV_f/dT for different transistors can be determined by placing the units in an oven, adjusting I_f to the value specified in above paragraph and then measuring V_f at different oven temperatures. Sufficient time must be allowed

for the junction temperature to reach that of the oven as mentioned earlier. This would be the most accurate value of dV_f/dT to use since it is determined for each transistor on an individual basis. A more convenient, but less accurate method, would be to take the average value of several transistors of the same type. Here the accuracy of the value of dV_f/dT would be dependent on the spread, but in general would be within the accuracy of the temperature measuring circuit described.

2. Procedure for Determining Junction Temperature
   a. Determine dV_f/dT for the transistor collector junction.
   b. With $V_C = 0$, and $I_E = 0$ connect transistor to terminals CBE of test circuit. Handle transistor in such a manner that its temperature is not raised above ambient (use gloves, etc.). Adjust R5 for time relationships shown in Figure 18.27.
   c. Adjust R1 for a reading of V_f on the scope equal to 500 mv + (27° − T amb.) × dV_f/dT.
   d. Set V_C and I_E to desired bias conditions.
   e. Note change in V_f. $T_{junc} = T_{amb} + \frac{(\Delta V_f)}{dV_f/dT}$
3. Procedure for Determining Thermal Resistance from Junction to Ambient
   a. Determine junction temperature as above.
   b. Measure power input to the transistor to give this temperature rise. ($P_{in} = V_{CE}$ max. × I_E max. × duty cycle).
   c. Thermal resistance from junction to ambient (Θ_{JA}) is then computed,

$$\Theta_{JA} = \frac{T_J - T_{ambient}}{P_{in}}$$

EXAMPLE:

A 2N657 transistor (a silicon NPN mesa with pellet mounted directly on flat metal header) is calibrated in an oven with I_f adjusted to give a V_f (V_{CB}) of 500 mv at 27°C. The slope dV_f/dT was found to be 2.5 mv/°C. It was desired to find what power was required to raise the junction 125°C above ambient and to determine the thermal resistance from junction to ambient at 149°C; room temperature = 24°C.

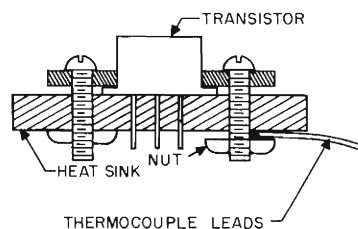
1. The transistor was connected to the terminals provided on test set up. $V_C = 0$ and $I_E = 0$.
2. R1 was adjusted to give a V_f of 500 + 3° (2.5 mv/°C) or 507 mv. (This took a resistance of nearly 20 megohms.)
3. For the junction temperature to rise 125°C, the voltage V_f in step 2 would have to drop by 313 mv (125 × 2.5). V_{CB} supply was set at 25v. I_E was then increased slowly until V_f dropped to (507 - 313) or 194 mv.
4. The voltage from C to E read with a Weston analyzer was found to be 20.0 volts. (This is an average voltage). The current in the emitter, read with a Weston analyzer in the emitter current lead, was found to be 33.3 ma. (Average value.) Thus the power dissipated in the transistor was approximately equal to

$$\frac{20.0 \times 33}{0.8} \text{ or } 834 \text{ mw.} \qquad P_{in} = \frac{I_{av} \times E_{av}}{\text{duty cycle}}$$

5. Since $\Theta_{JA} = \frac{T_J - T_A}{P_{in}}$

then $\Theta_{JA} = \frac{149 - 24}{834} = 0.149°C/mw$

4. Procedure for Determining Thermal Resistance from Junction to Sink

The thermal resistance from junction to sink is a useful parameter for computing operating junction temperature of a sink mounted transistor from the input power and sink temperature. Junction to sink thermal resistance can be calculated using the same procedure as used for Θ_{JA} with the exception that sink temperature is now used instead of ambient temperature. The heat sink will be more efficient if it is placed in contact with the surface on which the pellet is mounted. For instance, units which have the pellet mounted on the header should have the heat sink placed in contact with the header, giving an excellent thermal path. The contact between the sink and the transistor header could be achieved by holding the unit tightly against a 2″ x 2″ x ⅝″ piece of copper by a steel washer clamped down on the transistor flange. Holes are only large enough so that the insulated transistor leads can pass through. Silicone grease is spread over all contact surfaces to provide a better thermal path between the transistor header and the copper. The sink temperature can now be measured by placing the thermocouple between the bottom of the copper fin and the nut as indicated in Figure 18.28.

THERMOCOUPLE PLACEMENT
Figure 18.28

Once case temperature is established, Θ_{JS} can readily be obtained by using the same procedure as used to find Θ_{JA}.

SMALL SIGNAL MEASUREMENTS (AUDIO) OF TRANSISTOR PARAMETERS

The two most familiar matrices (the z and y) proved to be difficult to apply to transistors in practice, for driving the collector of a transistor with a current, in measuring z_{22B}, required large source impedances; and driving the input to the transistor with a voltage source, as in measuring y_{11e}, could produce large errors due to the current sensitivity of the device. (Base currents when multiplied by h_{fe} could cause current clipping in the collector.)

To overcome these disadvantages the *h* or hybrid matrix was proposed and became commonly used. The device characteristics that make the *h* matrix most useful at audio and low rf frequencies change appreciably as the frequency is increased. Above 30 mc the terminal requirements become increasingly difficult to obtain; measurements at these higher frequencies will be discussed in next section, (High Frequency Small Signal Measurements of Transistor Parameters).

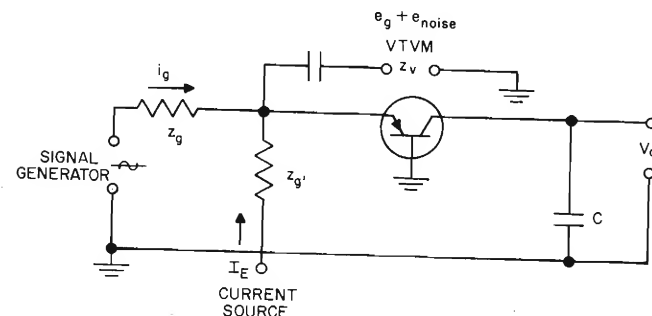
Consider the terminal requirements of the *h* matrix, and how they may be obtained in practice. The matrix is described as follows:

$h_{11} = e_1/i_1$ when $e_2 = 0$ (Input impedance, short circuit output)
$h_{12} = e_1/e_2$ when $i_1 = 0$ (Reverse voltage ratio, open circuit input)
$h_{21} = i_2/i_1$ when $e_2 = 0$ (Forward current gain, short circuit output)
$h_{22} = i_2/e_2$ when $i_1 = 0$ (Output admittance, open circuit input)

These matrix quantities are defined for either common base, common emitter or common collector configuration. Originally 270 cps was the audio frequency used in parameter determination, but today 1 kc is used more frequently although both are still common.

In establishing the correct a.c. conditions several considerations are of importance. In establishing these conditions, the desired percentage of accuracy will be used as the factor which will determine how well the ideal measurement conditions are realized. 1/(Desired Percentage of Accuracy) will be called $(DPA)^{-1}$; thus, if the desired accuracy is 5% then $1/.05 = 20$ or $(DPA)^{-1} = 20$. The following notes on each measurement show where errors may be introduced and indicate what conditions must be established for measurements to be of desired accuracy.

COMMON BASE CONFIGURATION

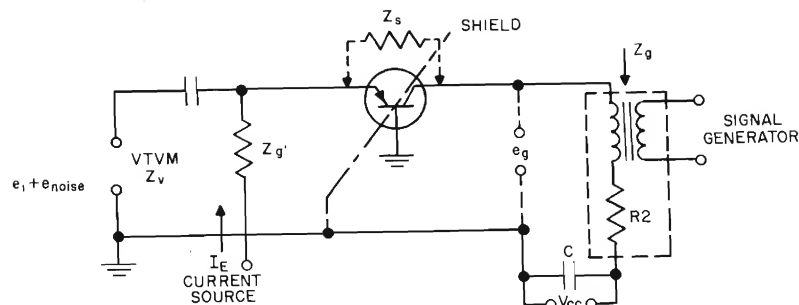
1. h_{ib} (h_{11b}) $\quad h_{ib} = \frac{e_g}{i_g}$

h_{ib} MEASUREMENT
Figure 18.29

For desired accuracy,

$$\frac{Z_v Z_g Z_g'}{Z_v Z_g + Z_v Z_g' + Z_g Z_g'} \geqslant (DPA)^{-1} h_{ib\,(MAX)}$$

$$\omega C \geqq (DPA)^{-1} h_{ob\ MAX} \text{ (for all tests)}$$

$$e_{noise} \ll e_g h_{ib\ MIN}$$

2. h_{rb} (h_{12b}) $\quad h_{rb} = \frac{e_1}{e_g}$

h_{rb} MEASUREMENT
Figure 18.30

z_s = effective leakage impedance

For desired accuracy,

$e_g << V_{cb}$

$I_C R2 << V_{cb}$

$$z_s >> \frac{z_v z_g'}{z_v + z_g'} \geqq (DPA)^{-1} h_{ib\ MAX}$$

$e_{noise} << 10^{-4} e_g$

$$\frac{1}{z_g} \geqq (DPA)^{-1} h_{ob\ MAX}$$

3. h_{fb} (h_{21b}) $\quad h_{fb} = \frac{i_2}{i_g}$

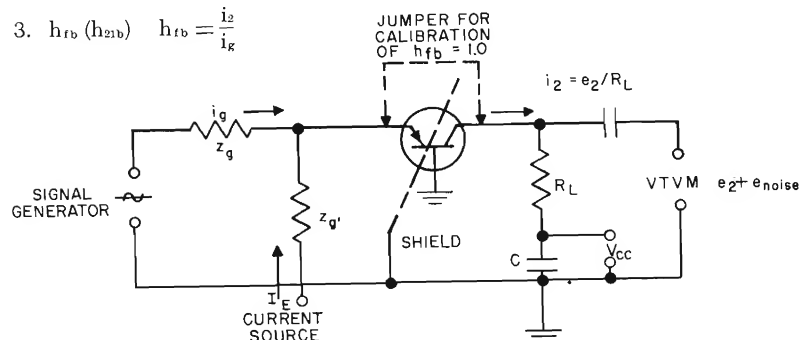



Figure 18.31 h_{fb} **MEASUREMENT**

$$i_2 = \frac{V_2}{R_L}$$

For the desired accuracy use the same considerations as for h_{ib} and,

$$\omega C >> \frac{1}{R_L} >> h_{ob\ MAX}$$

(R_L is normally less than or equal to 100 ohms average)

$$\frac{z_g z_g'}{z_g + z_g'} \geqq (DPA)^{-1} R_L$$

$i_g << I_C$

4. h_{ob} (h_{22b}) $\quad h_{ob} = \frac{i_g}{e_g}$; $i_g \cong \frac{e_v}{R_L}$ since i_e is small.

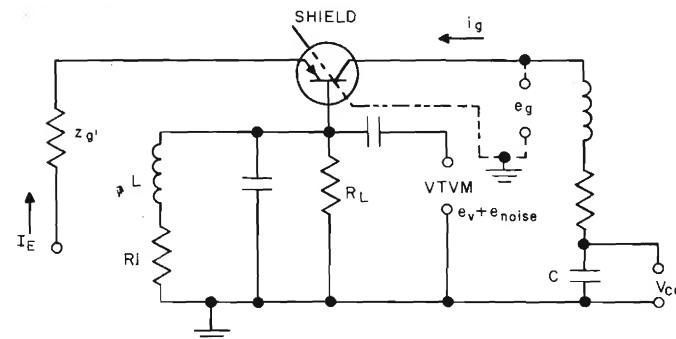



Figure 18.32 h_{ob} **MEASUREMENT**

For the desired accuracy use the same considerations as for h_{rb} and,

$e_g h_{ob\ MIN} R_L >> e_{noise}$

$$z_s >> \frac{1}{h_{ob\ MIN}} \geqq (DPA)^{-1} R_L$$

$[I_{CBO} + (1 + h_{FB}) I_E] R_L << V_{CC}$

$Q\omega L \geqq (DPA)^{-1} R_L$ at measuring frequency

To satisfy some of the above R_L requirements and yet have z_L large enough to have sufficient sensitivity; a parallel resonant circuit of low series R is bridged across R_L to reduce the dc drop.

COMMON EMITTER CONFIGURATION

When considering practical measurements of grounded emitter parameters it is also necessary to consider the dc bias requirements. It immediately becomes apparent that each transistor will require base bias adjustments to obtain specified base conditions. Since it would be preferable to avoid this time consuming operation and particularly so when many units must be measured, a *quasi* grounded emitter circuit is used. Through the use of high Q, parallel resonant circuits, the device sees a grounded base bias supply and an ac grounded-emitter configuration. Of course this technique is applicable to fixed-frequency measurements only. It is also necessary to consider the current multiplication of input measuring currents appearing in the collector circuit. To maintain *small signal* requirements steps are taken to insure that these collector signal currents will be much less than the dc bias currents. (See Introduction, to this chapter.)

1. h_{ie} (h_{11e}) $\quad h_{ie} = \frac{e_g}{i_g}$

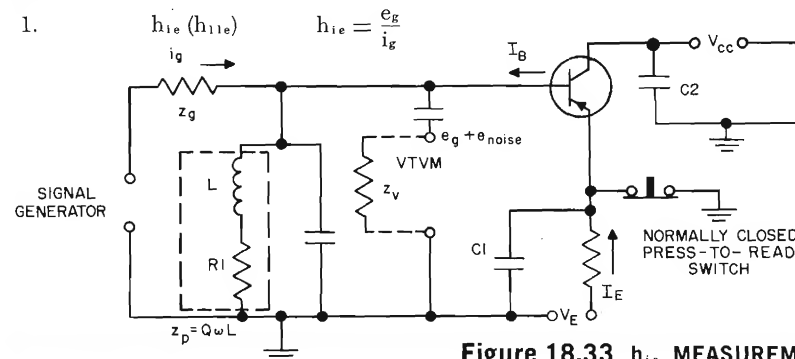



Figure 18.33 h_{ie} **MEASUREMENT**

Coils used are high Q toroids in which dc saturation must be considered when certain bias conditions are used.

For the desired accuracy,

$$i_g << \frac{I_c}{h_{fe\ MAX}}$$

$$I_B\, R1 << V_{cc}$$

$$\frac{z_v\, z_p\, z_g}{z_v\, z_g + z_v\, z_g + z_p\, z_g} \geqq (DPA)^{-1}\, h_{ie\ MAX}$$

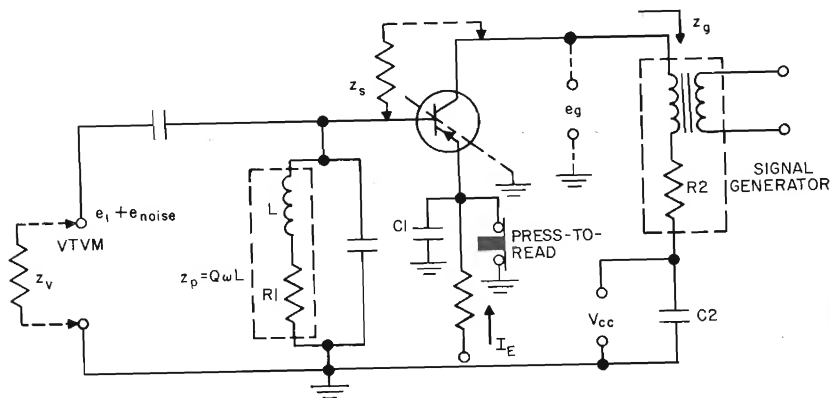
$$\frac{1}{\omega C1} << r_e \text{ at specified } I_E$$

$$\text{where } r_e \cong \frac{kT}{qI_E} \cong 26\ \Omega \text{ at } I_E = 1 \text{ ma (see Introduction this chapter)}$$

$$\omega C2 >> h_{oe}$$

$$e_{noise} << h_{ie\ MIN}\, i_g$$

The press-to-read switch is incorporated to prevent charging C1 to V_E when no transistor is in the socket. Otherwise, the discharge of the capacitor may destroy a unit as it is inserted into the socket for test.

2. h_{re} (h_{12e}) $\qquad h_{re} = \frac{e_1}{e_g}$

h_{re} MEASUREMENT
Figure 18.34

C1, C2, and R1 are the same as for h_{ie}

For desired accuracy,

$$I_c\, R2 << V_{cc}$$

$$e_g << V_{cc}$$

$$z_s >> \frac{z_p\, z_v}{z_p + z_v} \geqq (DPA)^{-1}\, h_{ie\ MAX}$$

$$e_{noise} << h_{re\ MIN}\, e_g$$

$$\frac{1}{z_g} \geqq (DPA)^{-1}\, h_{oe\ MAX}$$

3. h_{fe} (h_{21e}) $\qquad h_{fe} = \frac{i_2}{i_g}\ ;\ i_2 = \frac{e_2}{R_L}$

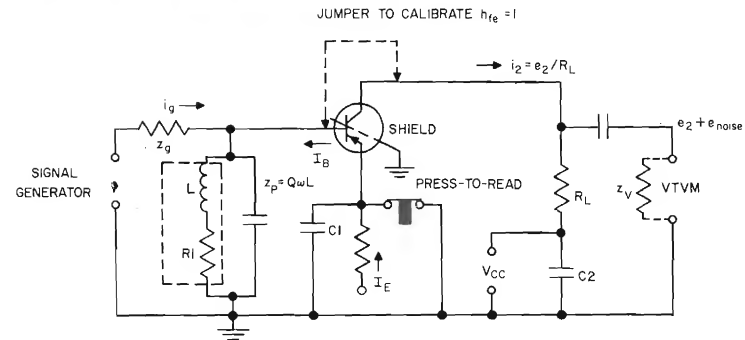



Figure 18.35 h_{fe} **MEASUREMENT**

For the desired accuracy, use the same considerations as for h_{ie} and,

$$e_{noise} << i_g\, R_L$$

$$R_L << \frac{1}{h_{oe\ MAX}}, \qquad R_L \text{ is generally about 50 ohms.}$$

4. h_{oe} (h_{22e}) $\qquad h_{oe} = \frac{i_g}{e_g}\ ;\ i_g \cong \frac{e_o}{R_L}$

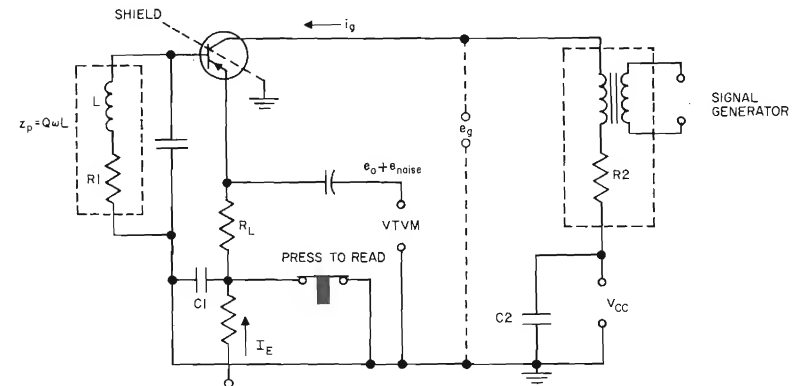



Figure 18.36 h_{oe} **MEASUREMENT**

z_g, R1, R2, C1, and C2 same as for h_{re}

For the desired accuracy,

$$z_p >> h_{fe\,MAX}\,(R_e + R_L)$$

$$e_{noise} << h_{oe\ MIN}\, R_L\, e_g$$

$$e_g << V_{cc}$$

COMMON COLLECTOR CONFIGURATION

Common collector parameters may be calculated from measurements of common base and common emitter. Notice that the two parameters not identical to those in common emitter configuration are in one case almost equal to h_{fe} and in the other almost equal to 1.

1. $h_{ic} = h_{ie}$
2. h_{rc} (h_{12c}) $\qquad h_{rc} = \frac{e_1}{e_g}$

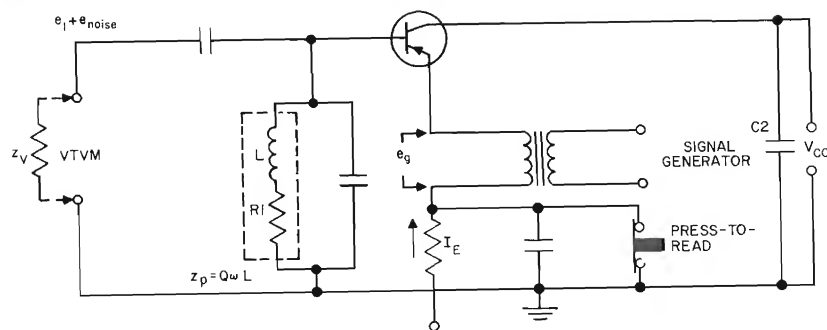



Figure 18.37 h_{rc} **MEASUREMENT**

Driving conditions are the same as for h_{re}; however, $e_g << V_{EB}$, also $h_{rc} \cong 1.0$ and deviations from unity are difficult to measure.

3. h_{fc} (h_{21c}) $\qquad h_{fc} = \frac{i_2}{i_g}$; $i_2 = \frac{e_2}{R_L}$

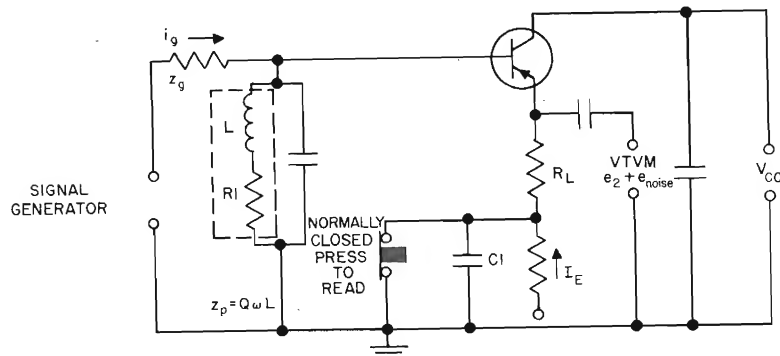



Figure 18.38 h_{fc} **MEASUREMENT**

Driving considerations are the same as for h_{fe} if R_L is kept small; otherwise,

$$z_p \geqq (DPA)^{-1} (R_e + R_L)$$

$$h_{fc} \cong h_{fe}$$

$$h_{fc} = \frac{1}{1 + h_{fb}}$$

4. $h_{oc} = h_{oe}$

GENERAL

Some of the parameters mentioned are particularly difficult to measure, the terminal requirements difficult to obtain, or particularly sensitive to temperature. When measuring h_{fb} it is found that as this parameter approaches unity, the difference is increasingly hard to detect. Instead, h_{fe} could be measured and h_{fb} calculated; or an attempt to measure $1 + h_{fb}$ could be made instead. A circuit for measuring $1 + h_{fb}$ is shown in Figure 18.39.

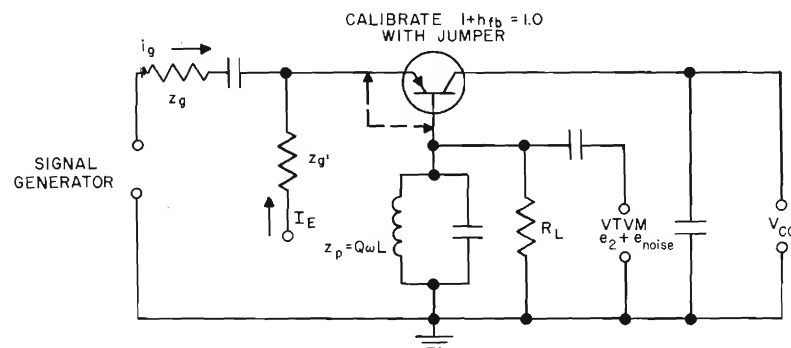
$$1 + h_{fb} = \frac{i_1}{i_g}, \qquad i_1 = \frac{e_2}{R_L}$$

1 + h_{fb} MEASUREMENT

Figure 18.39

Considerations for obtaining accuracy are,

$$\frac{z_g\, z_g'}{z_g + z_g'} \geqq (DPA)^{-1} (h_{ib} + R_L)$$

$$z_p \geqq (DPA)^{-1} R_L$$

$$e_{noise} << (1 + h_{fb\ MAX}) R_L i_g$$

$$\omega C_2 >> h_{oe\ MAX}$$

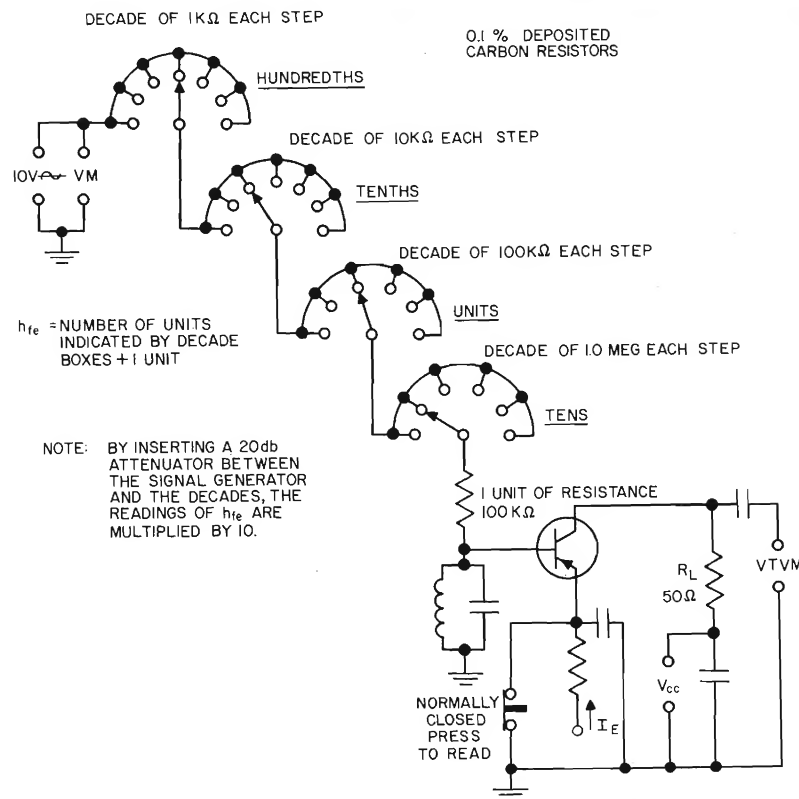
However, since R_L appears in the collector loop, the collector is not really short circuited, and R_L must therefore be kept quite small. On the other hand, it must be insured that $i_g << I_E$ (in the order of 0.1 ma RMS for 1.0 ma I_E). Now the maximum current that will flow through R_L will be i_g when $h_{fb} = 0$, therefore in practice $i_g R_L = 10^{-4} \times 10^2$ or about 10 mv at most. Since, too, it is preferable to measure up to $h_{fb} = 0.999$, the ability to measure $1 + h_{fb}$ max. $\times\ i_g R_L$ = about 10 microvolts is necessary. Some available VTVM's do not have sufficient sensitivity for this measurement and either selective VTVM's or pre-amplifiers must be used; at this point, noise and "pick-up" become important considerations.

Similar important considerations also arise in measuring h_{fe}. In order to maintain the collector signal current within the required small signal level, one must start with 10^{-4} amps and a reading resistor of 50 ohms max, assuming 1.0 ma dc collector current. This output signal of 5 mv is the maximum signal level in the collector. To measure h_{fe} up to 1000, one would have to insert a base signal current of 10^{-7} amps; and calibrating by inserting this signal into the 50 ohm resistor, it develops that only 5μv of signal are available and the permissible noise background is less than 0.5 μv.

To illustrate a method whereby most of these difficulties may be eliminated by a different technique of measuring, the circuit of Figure 18.40 is considered.

In this instance a constant signal voltage (say 10V) and a *unit* of resistance are used that will limit the signal current to that permissible in the collector circuit. At 50 ohm and 0.1 ma a *reference* signal of 5 mv exists, which is readily measurable. The *unit* of resistance is 100 K. Now *units* of resistance are inserted in the base circuit (ac) until the collector current returns to the reference level. The number and fractions thereof of units of resistance will read h_{fe} directly; and the result is that a calibrated decade resistance box is used to read h_{fe}. At 1 kc accuracy is not limited by the resistors, but rather by the ½ to 1% resetability of the VTVM pointer. By using a

ALTERNATE h_{fe} MEASUREMENT

Figure 18.40

selective VTVM with an expanded scale, such as the Hewlett-Packard 415B, (VSWR indicator) resetability and accuracy can be improved to better than 0.2%. The limitation now is the accuracy with which the temperature of the unit under test can be maintained since h_{fe} is temperature sensitive.

HIGH FREQUENCY SMALL SIGNAL MEASUREMENTS OF TRANSISTOR PARAMETERS

GENERAL

The subject of high frequency *h* parameter measurements is considered in this section. Measurements from 100 kc to above 300 mc are considered.

1. Common Base - Common Emitter

   Several considerations must enter into making a small signal measurement other than the high frequency techniques. Of importance is the time required and, in common emitter measurements, the effect of the dc shunt paths. For both of these reasons, all of the common emitter measurements are made in the *pseudo* grounded emitter configuration where, to dc, the circuit appears common-

base. This was described in the last section. All of the considerations described there are equally applicable at high frequencies.

2. Broad-Band Measurements

   Common base broad-band measurements are feasible up to 100 mcs with care in circuit layout and due attention to socket capacity, etc. Common emitter measurements are broad-band in a very limited sense. By picking a sufficient number of spot frequencies data are obtained to draw a curve of parameter vs. frequency. The spot-frequency approach results directly from the circuits which will be described.

INPUT IMPEDANCE: (h_{ib}, h_{ie})

1. 200 kc to 5 mcs

   For this measurement the British Wayne-Kerr Model B601 Bridge was found to be the most suitable. By using suitable multiplier taps it will measure from a few ohms to more than one megohm of R parallel and reactances of ± several hundred μμf with reasonable accuracy. However, some reactance errors arise in measuring low parallel R values, due to inductance inside the bridge.

   A receiver is used as the bridge detector. A unit with a few μv sensitivity and a frequency range of 200 kc to 5 mcs. This detector sensitivity is mandatory, since the maximum signal voltage the bridge applies to the input of the transistor must be less than 5 mv, if overdriving the unit and distortion are to be avoided. Since small-signal conditions are to be maintained, the ac currents permissible should be at most 10% of the dc bias currents. Assuming 1.0 ma I_E and 50 ohms of h_{ib} then the maximum input signal voltage is $10^{-4} \times 50 = 5$ mv. Now for common-emitter operation, (assuming $1 + h_{fb}$ of .01), the base current is 10^{-5} amps. For 500 ohm of h_{ie} the maximum signal swing is $10^{-5} \times 5 \times 10^2 = 5$ mv. These figures are arbitrary, but realizable, and show the need for care. A suitable substitute is to incorporate means of reading the ac current in the collector; and, abiding by the 10% rule, the input signal is adjusted to the maximum permissible. The signal generator used is a Tektronix 190 with the attenuator fixed to limit the input signal to the bridge. Since the Tektronix 190 starts at 375 kc this is the lowest frequency measured. Another generator, such as the Hewlett-Packard 650-A will extend the low frequency range. Test circuits are in plug-in boxes, for connecting to the bridge and are shown in Figure 18.41(A).

2. 1 to 100 mcs

   At higher frequency the small signal terminal requirements of *h* parameters (viz. *open* and *short* circuits) are progressively more difficult to obtain. In general, the input impedances are lower due to decreasing current gain and shunt reactance effects. The requirements of low driving signal voltage and the detector sensitivity demanded are even more stringent.

   The Wayne-Kerr Model 701B Admittance Meter is used with a Hallicrafter SX-62A receiver as the null detector. Mathematical conversion from the parallel admittances to the required series $R_s \pm jX_s$ will be necessary. The generator used here is a Measurements Corp. Model 80 with a 2 mc to 420 mc frequency range. Since the Wayne-Kerr Model 701-B bridge has a 3:1 step-down transformer built in, the signal input to the bridge is limited to 10 mv maximum. The circuits used in measurements are shown in Figure 18.41(B).

(A) UP TO 5 MC

(B) UP TO 100 MC

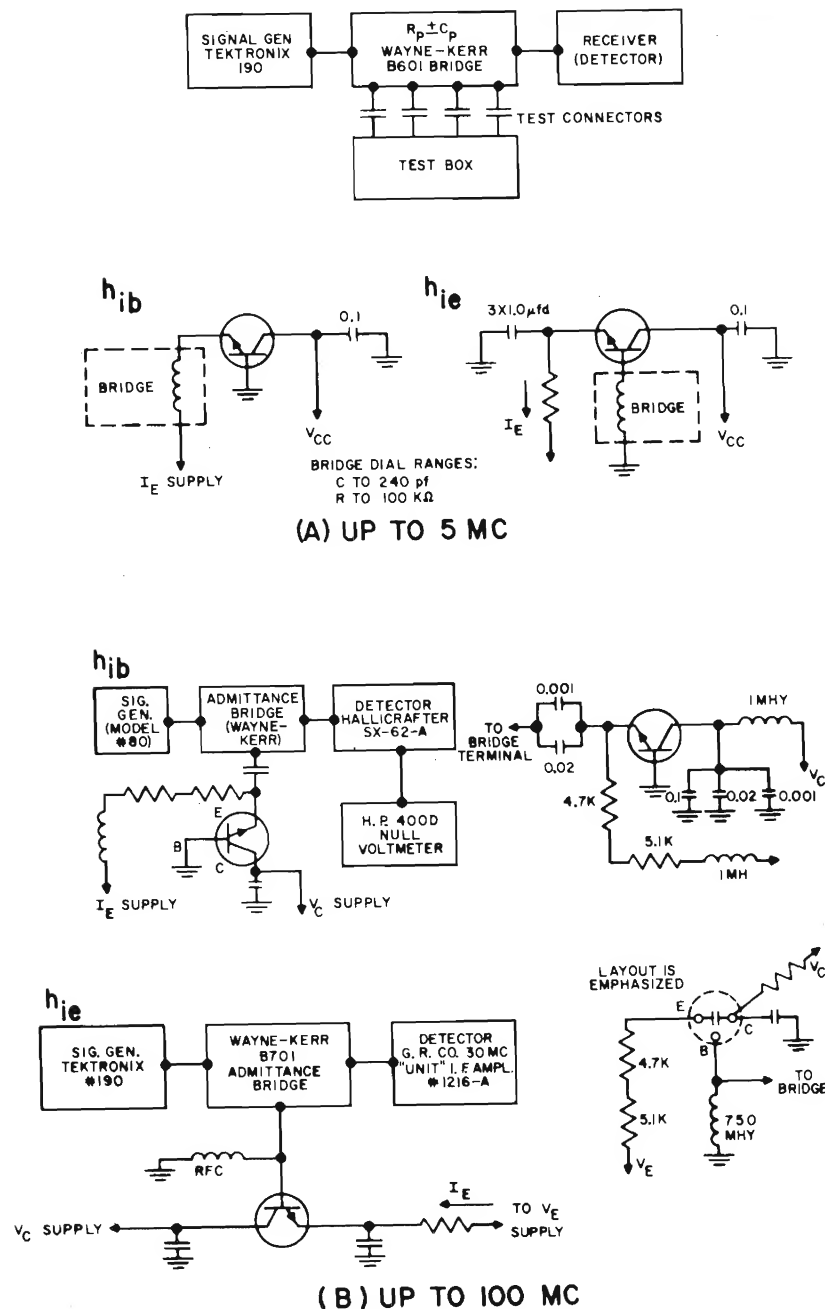



Figure 18.41 h_{ib} AND h_{ie} MEASUREMENT

3. 30 Mcs and Higher

Two different Rohde and Schwartz Diagraphs are being used above 30 mc. One, Model ZDV, BN3561 operates from 30 to 300 mc; another, Model ZDD, BN3562 operates from 300 to 2400 mc. These diagraphs measure the impedance or admittance of an unknown by measuring the reflection coefficient between a reference and an unknown transmission line. All shorts and opens at advanced frequencies can be established by using transmission lines of the appropriate length; that is, an open quarter-wave line is an ac short and an open half-wave line is an ac open. The system used is basically a 50 ohm system and measurement of h_{ib} or h_{ie} may be read directly from the Smith chart display of the diagraph.

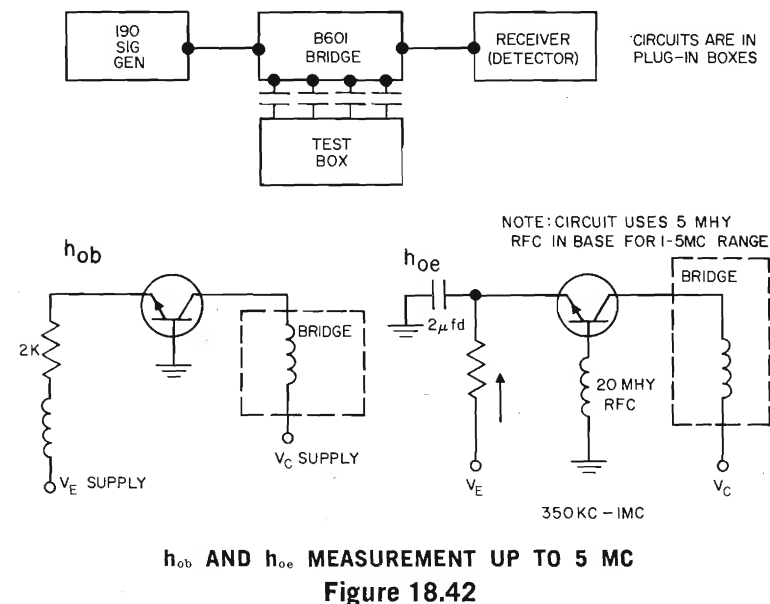
OUTPUT ADMITTANCE (h_{ob}, h_{oe})

1. 200 kc to 5 mcs

The same equipment is used here as for the h_{ib} measurements. However, as much as 1.0 volts rms (although less is preferable) can be applied at the collector. The slope of the characteristic is reasonably constant over a large range of V_{cc}.

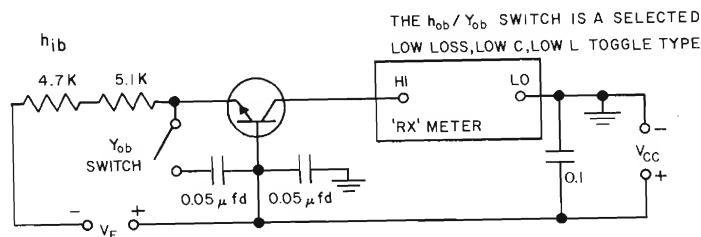
A conversion from $R_p \pm jX_p$ to $G \pm jB$ is necessary. Circuits are in plug-in boxes.

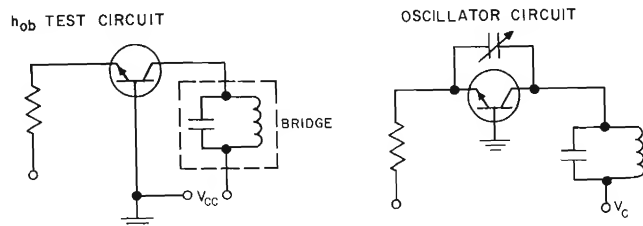
h_{ob} AND h_{oe} MEASUREMENT UP TO 5 MC

Figure 18.42

2. 500 kc to 200 mcs

The Boonton Radio Corp. Model 250 RX meter is used to make these measurements. The bridge measures $R_p \pm C_p$ and has a built-in signal generator and heterodyne detector. The "RX" meter measures R_p from 15 ohms to over 100 k ohms and -80 pf to $+20$ pf (with means of extending this range by adding external reactance).

Since dc currents of up to 50 ma may flow through the bridge, the

shunt-feed problems are alleviated somewhat, and the entire bias supply is "floated" with respect to the bridge as follows:

h_{ob} AND h_{oe} MEASUREMENT UP TO 200 MCS
Figure 18.43

The built-in positive feed-back in the common base configuration, due to "overlap" capacity, etc., will often make the resistance term appear negative. The bridge, of course, is not designed to measure −R. Yet by balancing the bridge at R = 10k, for example, and rebalancing with the unit inserted one can calculate the effective −R term. The built-in capacity is sufficient to warrant great care to prevent any more from being added by the external circuit, and a shield between emitter and collector should be included in the physical circuit. A comparison of the measuring circuit of Figure 18.44, and that of an oscillator clarifies the above requirement for minimum capacitance. Also note that h_{ob} may not be measurable at some frequencies, and an ac by-pass may be switched in, in order to measure the parallel equivalent of y_{ob}, which is also useful in determining h_{rb} at high frequencies.

COMPARISON OF h_{ob} TEST CIRCUIT WITH THAT OF AN OSCILLATOR
Figure 18.44

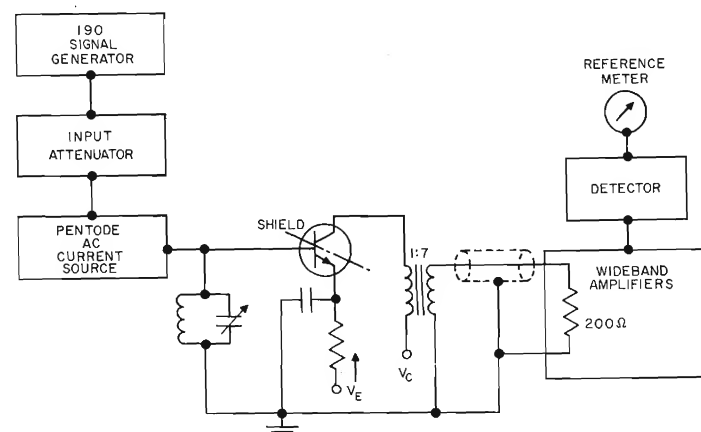
3. 30 Mcs and Up

   The Rohde and Schwartz Diagraph is also used on output measurements at higher frequencies. However, since the diagraph is a 50 ohm system, the resolution above 2.5 k ohm is difficult; thus, on some devices the real part of h_{ob} and h_{oe} may be difficult to determine except to say that it is less than 1/2.5 k or 0.4 millimhos.

FORWARD CURRENT RATIO (h_{fb}, h_{fe} AND f_{hfb})

Maintaining a high impedance, broad band current source in the presence of capacity is difficult. The problem arises in determining what signal current is being injected into the transistor, i.e., in calibrating the *unity* input current. It is convenient to assume that when the current is jumpered into the collector reading resistor to calibrate the set, this current will then flow into the transistor too. However, even 5 $\mu\mu$f of capacity of the emitter socket has a capacitive reactance of only 1.5 k ohms at 20 mcs, which is not a good current source if $R_L = 25$ ohms and $h_{ib} = 200$ ohms. This can cause a 10% current change, and much larger errors in frequency when measuring f_{hfb}, (the slope of h_{fb} with frequency is relatively small) since $\alpha \approx \dfrac{\alpha_o}{1 + j\dfrac{f}{f_{hfb}}}$.

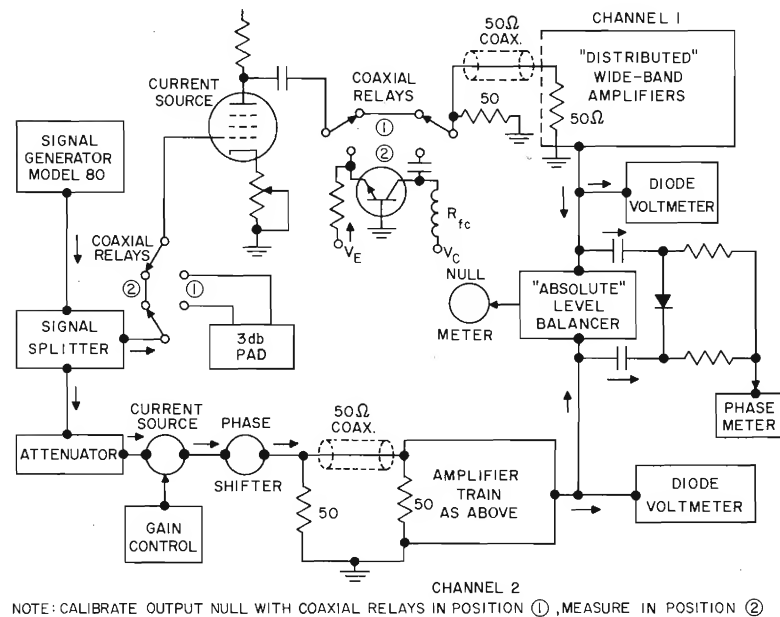
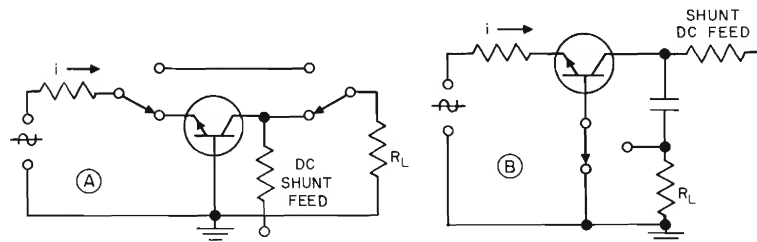
Another factor rises which must be considered. The input impedance of the transistor looks inductive below f_{hfb}, and at some point becomes resonant with the terminal capacity. If the real part of h_{ib} is larger than the reactive part, then the Q of the circuit exceeds unity and more current flows in the emitter. At this juncture, the current gain appears to exceed unity. It is the nature of h_{fb} to return to unity at high enough frequency, as an examination of the equivalent circuit will show. Of course, h_{fb} could be measured at many frequencies while resonating out the terminal capacity for each step. This is done for h_{fe} and f_{hfb}, but is time-consuming. Time consuming, too, is the recalibration operation in f_{hfb} measurements, but this time has been reduced as much as possible in the circuit shown in Figure 18.46. The switching is made automatic, and the gain is changed to correct for the difference between h_{fb-o} (low frequency) and unity. This too is automatically switched between *calibrate* and *measure* positions. With a flat 3 db pad (General Radio type), the detector becomes a reference indicator. Now the frequency is found where both readings are equal.

The phase of h_{fb} at any frequency may be found by using a parallel (and as nearly identical as possible — but without the transistor) channel as a reference. The two channels are amplitude and phase balanced without the transistor. The transistor is then inserted, amplitudes rebalanced, and the peak vector voltage between the

h_{fe} AND f_{ae} MEASUREMENT UP TO 10 MCS
Figure 18.45

channels measured. An Advance Electronics Corporation "Vectrolizer" is used. This consists of a peak reading diode differential detector and dc amplifier/voltmeter.

The usual considerations of signal currents in the collector still apply. Lead-length is critical in this equipment and *disc* type by-pass capacitors are preferable.

1. h_{fe} and $f_{\alpha e}$ to 10 mcs is measured in the arrangement shown in Figure 18.45.
2. h_{fb}, f_{hfb} and phase of α to 100 mcs is measured as shown in Figure 18.46.

Two basic methods of calibrating *unity* current are shown in Figure 18.47.

h_{fb}, f_{hfb}, AND PHASE OF α MEASUREMENT UP TO 100 MCS
Figure 18.46

METHODS OF CALIBRATING UNITY CURRENT
Figure 18.47

Signal generators used are either the Tektronix Model 190, up to 50 mcs, or the Measurement Corporation Model 80 up to 100 mcs, and beyond. The distributed amplifiers used are the Hewlett-Packard Model 460A or the Spencer-Kennedy Model 201, the latter having a 200 mcs cut-off frequency. Detectors are the Hewlett-Packard Model 401-B or the Boonton Electronics Company Model 91-B. The "Vectrolizer" has already been described.

Finite termination transfer constants can be measured on the diagraph which when coupled with a knowledge of the other h parameters measured will yield the h_{fb}, h_{rb}, h_{fe} or h_{re}. The computation involved is somewhat long and tedious and with any large number of measurements would almost require a computer. In the measurement of h_{fe} at high frequencies another test facility has been developed which will perform this measurement at certain fixed frequencies. 20, 40, 100, and 200 mcs are currently used. This measurement is essentially used to determine the f_t of a device where f_t is equal to h_{fe} times the frequency of measurement if the h_{fe} vs. frequency characteristic is decreasing at 6 db/octave at the frequency of measurement. f_t is defined as the frequency at which $h_{fe} = 1$.

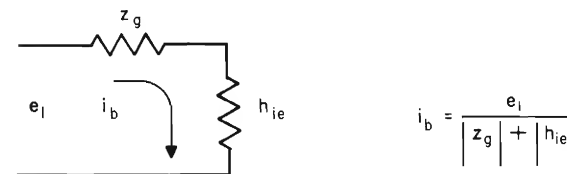
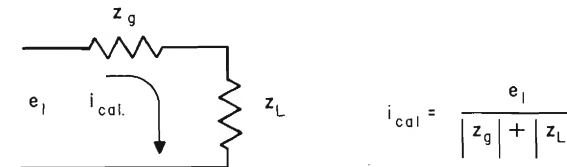



Figure 18.48 BASE ERROR TERMS

$(i_b)\ (h_{fe})$ i_c h_{oe} y_L i_l

$$i_l = i_c \left(\frac{y_L}{y_L + h_{oe}}\right)$$

$$i_l = i_c \left(\frac{1}{1+\left|\frac{h_{oe}}{y_L}\right|}\right)$$

$$i_l = i_{cal} \left(\frac{1+\left|\frac{z_L}{z_g}\right|}{1+\left|\frac{h_{ie}}{z_g}\right|}\right)\left(\frac{1}{1+\left|\frac{h_{oe}}{y_L}\right|}\right) h_{fe}\ \text{(ACT.)}$$

$$h_{fe}\ \text{(MEAS.)} = \frac{i_l}{i_{cal}}$$

h_{fe} (MEAS.) SHOULD = h_{fe} (ACT.)

$$\frac{i_l}{i_{cal}} = h_{fe}\ \text{(MEAS.)} = \left(\frac{1+\left|\frac{z_L}{z_g}\right|}{1+\left|\frac{h_{ie}}{z_g}\right|}\right)\left(\frac{1}{1+\left|\frac{h_{oe}}{y_L}\right|}\right) h_{fe}\ \text{(ACT.)}$$

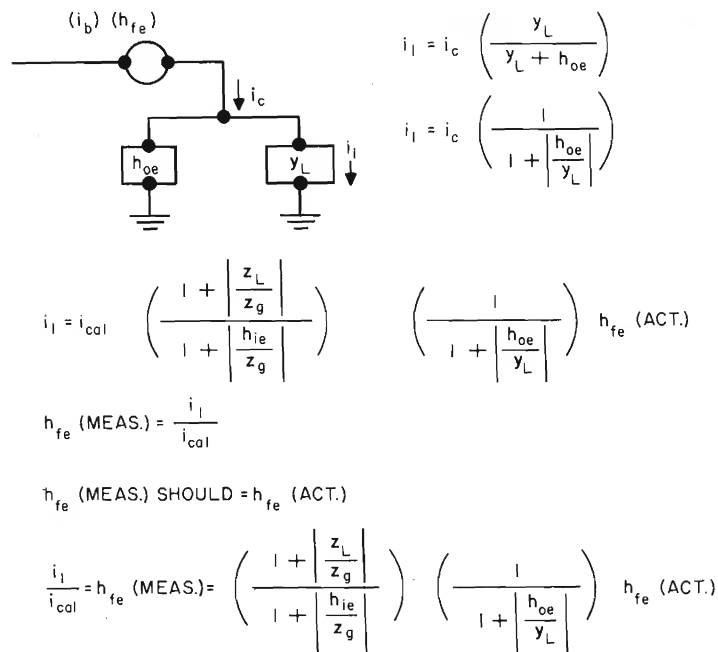



Figure 18.49 COLLECTOR ERROR TERMS

a. f_t Measurement

In a high frequency mesa transistor, the f_t point or the frequency where $h_{fe} = 1$, usually occurs at a frequency in the order of several hundred megacycles which makes measurement of this quantity quite difficult. This is in addition to the device parasitics interfering with the measurement. To avoid such difficulties, h_{fe}, (the short circuit current gain of a transistor), is measured at a fixed frequency somewhat below the $h_{fe} = 1$ value. The f_t point can then be very closely approximated by applying the relationship of $f_t = (h_{fe})\ (f_{measured})$ as mentioned. In the particular test set described provisions were made to check h_{fe} at two fixed frequencies an octave apart. This, in effect, tells:

1. If the particular transistor under test has any useful gain at these frequencies.
2. If the transistor is following the theoretical 6 db/octave slope.
3. If the second condition holds, what the value of f_t is.

For example, two sets of similar design will be described for two different types of mesa transistors. The fixed frequencies of one are 100 and 200 mcs, and the other, 20 and 40 mcs.

Problems which must be avoided in the measurement of f_t are:

1. The signal level applied to the base must not be too high for a small signal measurement.
2. The signal fed into the base must be a suitable current source.
3. The output reading load must be well defined.

To illustrate where these problems arise, consider the errors in calibration in the input circuit of Figure 18.48, and in the output circuit of Figure 18.49 when the transistor is inserted. Combining these two terms results in Figure 18.50 where the total relationship of *measured* h_{fe} as compared to ***actual*** h_{fe} is shown.

The object of this measurement is to get the *measured* value of h_{fe} to equal or to approximately equal the *actual* h_{fe} value. Therefore, both the input and output error terms must be minimized; i.e., the variation of the input loop impedance when changing from the calibrating load to the input impedance

$$h_{fe}\ \text{(MEAS.)} = \left(\frac{1+\left|\frac{z_L}{z_g}\right|}{1+\left|\frac{h_{ie}}{z_g}\right|}\right)\left(\frac{1}{1+\left|\frac{h_{oe}}{y_L}\right|}\right) h_{fe}\ \text{(ACT.)}$$

ERROR TERMS IN h_{fe} MEASUREMENT

Figure 18.50

of the transistor under test must be minimized and the magnitude of the output admittance, h_{oe}, as compared to the load must be minimized. In other words,

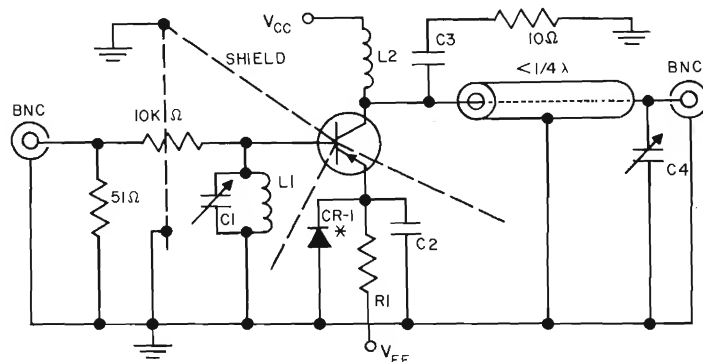
$$\frac{h_{ie}}{z_g} \text{ and } \frac{h_{oe}}{Y_L} \text{ must be} < 1.$$

The signal current generator uses a 10 k ohm series resistor to the base of the transistor and is placed through a double sided copper clad shield which tends to reduce the shunt capacitance across the resistor since at high frequencies shunt or stray capacities lower the impedance of a current source. To compensate for the residual capacitance in the test set described and therefore raise the current source's effective impedance at the base of the transistor socket, a high Q parallel resonant circuit is placed to ground. (One of the methods which can be used to tune the resonant circuit is to install it physically in the test circuit and then connect an RX Bridge as closely as possible to the base terminal of the transistor socket. Set the C_p dial on the RX meter to 0 pf. Tune the capacitor in the test set and the R_p dial on the RX meter until the meter on the RX bridge nulls. Then read the R_p dial. This is the effective impedance which normally is from 4 to 8 k ohms depending upon the frequency of the test set.)

Some mesa transistors tend to exhibit an output impedance, $1/h_{oe}$, in the order of from 50 to 100 ohms at high frequency. Therefore, in order to measure this type of transistor with accuracy the magnitude of the load admittance terms, y_L, must be greater than 100 millimho (or $R_L < 10\Omega$). In order to realize this condition, transmission line techniques are applied. Not only does the transmission line transform the 3 k ohms resistance of the rf millivoltmeter used as a detector to approximately 1 ohm, but the standing wave voltage transformation permits operation at lower signal levels. Effectively a quarter wave transmission line is placed from the collector of the transistor socket to the rf millivoltmeter. In practice, it is found much easier to cut a piece of cable shorter than the actual quarter wave length and use a variable ceramic capacitor at the rf voltmeter end of the cable to ground. When adjusted, this capacitor electrically extends the line to exactly a quarter wave length.

With mesa transistors in a psuedo-grounded emitter configuration which is used in this circuit, a mesa transistor may break into oscillation. Therefore,

a series RC circuit, using a 10 ohm resistor, is placed from collector to ground. This effectively lowers the collector impedance at frequencies other than the frequency of interest and discourages unwanted oscillations.

Figure 18.51 is the diagram of the test set. High frequency construction techniques are used. Shielding is of utmost importance, and the input circuit must be isolated from the output circuit to avoid leakage of signal which could cause a calibration error. (In this case, the base from the collector.) In

	20 MC	40 MC	100 MC	200 MC
C1	3–12 pf	3–12 pf	1.5–7 pf	1.5–7 pf
C2	0.1μf	0.1μf	0.01μf	0.01μf
C3	0.1μf	0.1μf	0.01μf	0.01μf
C4	3–12 pf	3–12 pf	1.5–7 pf	1.5–7 pf
L1	10μh	2.2μh	0.68μh	0.15μh
L2	82μh	47μh	4.7μh	4.7μh
R1	2–500Ω IN SERIES	2–500Ω IN SERIES	2.2 K	2.2 K

*CR1 SHOWN FOR PNP OPERATION OF CIRCUIT (3-1N540'S IN SERIES)

DIAGRAM OF h_{fe} TEST SET

Figure 18.51

constructing this test circuit, double sided copper-clad board is used. Components are physically placed such that lead length is kept to a minimum. To eliminate lead inductance of the transistor under test, a socket is used which allows close connection of the circuit to the transistor header. A rectifier, CR-1, is connected from emitter to ground to insure that C2 does not charge-up when the test socket is empty. This prevents destroying the next transistor to be tested. In Figure 18.51 the circuit is connected for PNP operation of the test set. A switchable attenuator box is used instead of the range switch of the rf millivoltmeter. The rf millivoltmeter used in this test set has about a 1 db non-linearity from scale to scale and within a scale. To avoid this error and still use the instrument, an alternate method is required using a single point on the voltmeter (say full scale on the 3 mv scale) and working around that level with a switchable attenuator.

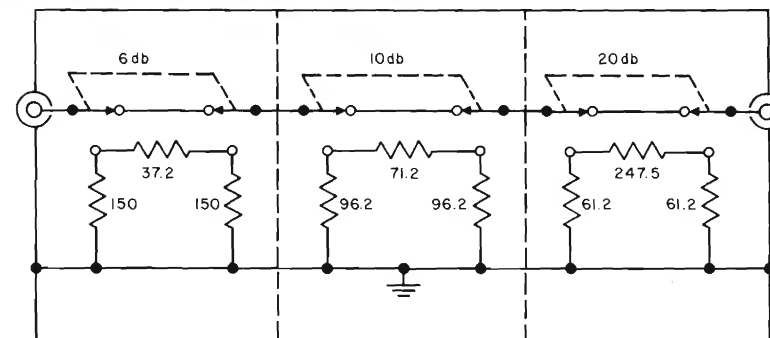



Figure 18.52 ATTENUATOR BOX

Figure 18.52 shows the attenuator box. Three switchable pads are incorporated enabling any combination of the three pads to be used. This in effect keeps the rf millivoltmeter on the same scale (3 mv scale) and within that scale, the pointer is always no less than ⅔ of full scale. The design formulas for these pads were taken from *Reference Data for Radio Engineers** using unbalanced π networks keeping the input and output impedances equal to 50 ohms.

POWER GAIN MEASUREMENT

GENERAL

In a practical and useful amplifying device there is one question of paramount importance, how much will it amplify at the frequency (or band of frequencies) of interest? In short, what is the power gain? Obviously where the amplifier has insufficient gain to fulfill the minimum requirements, the device is of only passing interest. Other important considerations may include flat frequency response, amplifier stability with temperature variation and other environmental changes, effective operating life of the device and total power consumption. Power gain, however, is still of primary interest and will be discussed in this section.

From the standpoint of the circuit designer the power amplifier should, among other things, be a *unilateral* device with no internal feedback of any sort, and have equal input and output driving point impedances. It should contribute no noise of its own to the signal being amplified, have a perfectly flat gain/frequency response, and a large gain-bandwidth product. Transistors, however, are not unilateral devices. Depending upon the circuit configuration being used (common base or common emitter) and the particular frequency, the internal feedback may be either negative or positive, and may even shift phase from one to the other. This effect is not unique to transistors, of course, but these internal aspects do necessitate some thought in defining Power Gain. Consider the case of an amplifier with positive feedback. When the feedback power is great enough to overcome the associated circuit losses, the device will oscillate. Describing the power gain of an oscillator is, of course, meaningless. With no signal applied and any signal at all out of the device, its apparent gain, according to the usual definitions, is infinite! This suggests the need for additional constraints in the definition of gain. Gain may be described under *neutralized* or *unilateralized* conditions, with attendant problems of defining measurement of the

*Published by International Telephone and Telegraph Company.

degree of *unilaterality*. Gain may also be defined with certain boundary conditions, or stability criteria, for example, when gain is measured with only that feedback required to make the output driving-point impedance appear infinite. This will be discussed later.

Problems of gain measurement break down into three specific phases:

a. Means of measuring input and output powers of the transistor.

b. Determining the effects of the circuit on the device.

c. Determining the effects of the device upon the circuit.

To be still more specific: in (a.) the generator and load impedances are adjusted to match (either resistively or complex conjugate) the transistor for maximum power gain. It must also be insured that the device is not over-driven either current or voltage-wise. In other words, assurance must be maintained that small signal conditions apply. Due to the extreme signal sensitivity of the usual low-power transistor, the measuring of ac powers in the order of 1 to 10 microwatts (ac currents in the order of microamperes and ac voltages of a few millivolts) is of concern. As a result the measurement problem is more complex than may be immediately apparent.

In (b.) spurious paths or parasitic strays can introduce unwanted feedback, and the particular terminations used must not permit the transistor to operate in a region where internal feedback can cause potential unstability. This is the "gain" of an oscillator paradox. The ideal way to guarantee that the above conditions do not exist is to measure the two port impedances when terminated at the other end by the apparent required match, to see that no signs of negative-resistance exist. This latter condition leads to (c.).

In any circuit with R, L, and C components, a basic loaded Q is present. Assume that this circuit is the complex conjugate match for a transistor. When this transistor is inserted, its output conductance appears across the circuit and the circuit Q should decrease to half the original value. Now consider what would happen were the device to have positive feedback. With enough feedback the output of the transistor has a negative resistance component which absorbs some of the circuit losses and the Active Q now increases. Even if this feedback is internal, rather than caused by unknown and uncontrolled strays, it is difficult to state with confidence the true gain of the transistor. However, a means of using the bandwidth of the circuit as a criterion of stability is available. Thus, the Active Q may be made less than that of the circuit Q alone. This approach will not suffice for negative feedback where the solution relies on the neutralizing techniques which are to be discussed shortly.

MEASURING POWER GAIN

Power gain depends on the particular definitions used and the frequency or band of frequencies being considered. These definitions are as follows:

1. $$G = \left(\frac{i_2}{i_1}\right)^2 \frac{R_L}{R_i} \text{ or } G = \frac{P_{out}}{P_{in}}; \text{ where } \frac{i_2}{i_1} = \text{current amplification gain}$$

   This is the low frequency case and is the actual gain between R_{gen} and R_{load} and is maximum when $R_{gen} = R_{input}$ and $R_L = R_{output}$ $P_{available} = \frac{(E_o)}{4 R_{gen}}$ where E_o = open circuit generator voltage.

2. $G_{Transducer}$ (circuit gain or available power)

   $G_{Transducer}$ is the output to available power ratio. The closeness of matching conditions to the two-port impedances of the amplifier will determine how closely G_T approaches $G_{max\ available}$.

3. $G_{available}$

   This is the gain of the transistor with only the real part of its input and output impedances matched to the load and generator.

4. $G_{maximum\ available}$

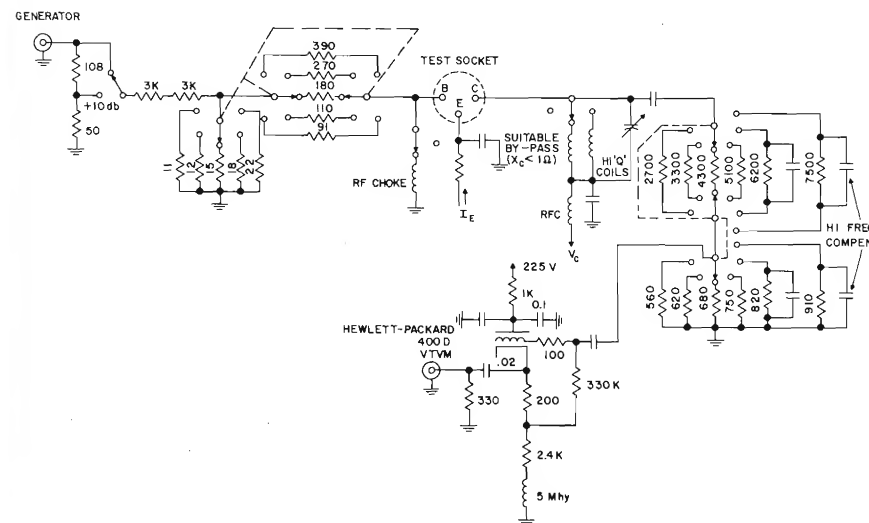
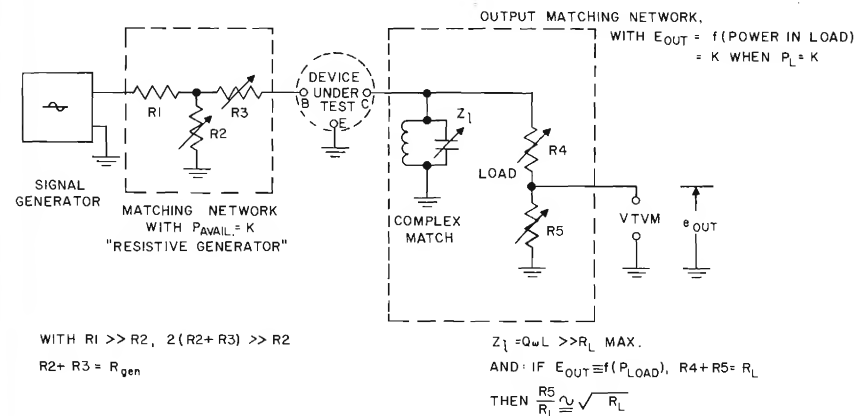
   The real parts are matched and the reactances are tuned out, that is, the same impedance but of opposite phase. This is the complex-conjugate match and is the most true gain obtainable. Close attention is required to distinguish between this and pseudo gains which may appear larger due to positive feedback.

POWER GAIN MEASUREMENT CIRCUITS

Figure 18.53

All of the foregoing definitions, with the possible exception of (1) may be considered as classes and are often divided into sub-classes as determined by the considerations mentioned earlier when discussing the phases of the measurement problem. As to the particulars of each measurement set: while it may be possible to measure the current amplification gain in (1) and (3), it is usually easier to have switchable R_G and R_L so arranged that the available generator power is kept constant and an output voltage is obtained proportional to the power in the load. It should be noted that this circuit is also applicable to (2) as long as a resistive generator is desired or necessary. The device, potentially unstable if complex-conjugate matched, may be usably stable if only one terminal is complex matched and the other resistively terminated. For practical reasons the generator is usually the resistive match as shown in Figure 18.53.

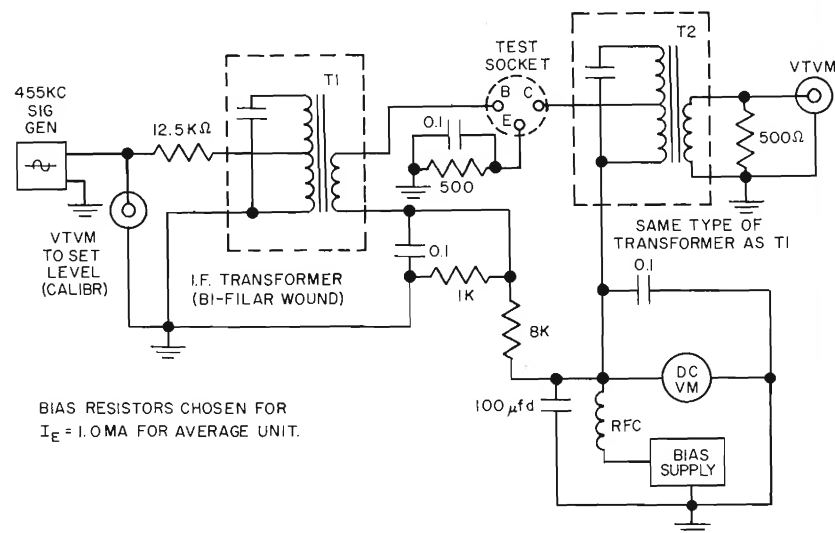
Measurement of (2) often takes the form of the circuit shown in Figure 18.54. This is a *functional* IF test.

FUNCTIONAL IF POWER TEST

Figure 18.54

To reproduce the measurements from set to set, the transformer loaded impedances, losses, and bandwidth must be specified. The layout is standardized and precision resistors and meters are used to establish the dc bias conditions. Since gain varies with temperature, means of controlling or at least monitoring temperature should be included. The use of attenuators to set relative levels on the VTVM is encouraged, rather than relying on the linearity and accuracy of the VTVM.

For complex-conjugate matching, and also for a simple method of measuring high-frequency gain, the π network has proven very useful as an impedance transformer. With care, the losses in the network can be kept low (in the order of 1 db). It should be remembered that this network acts as a filter, and bandwidth measurements should not be made. Where bandwidth is important the use of variable link coupling networks will prove more satisfactory.

In the following circuit, Figure 18.55, the detector is coupled into the generator at the calibrate jack. The network is then adjusted for a maximum reading. Assuming

the losses of the input network are constant with small variations of match, and the input impedance of the transistor is close to the 50 ohms of the detector, the output will be the zero db reference setting, and only the losses in the output network are important. By keeping these losses small with proper network design, the losses can then be considered as part of the transistor's gain.

NEUTRALIZATION

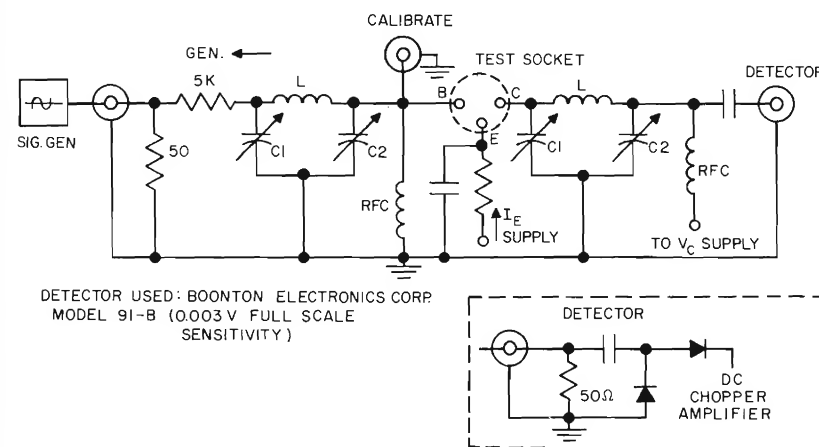
The need for neutralization arises when internal feedback exists. The device is not unilateral and variations of load affect the input impedance. This fact enables one to devise methods of determining when neutralization has been accomplished. There are two accurate measuring techniques. One uses a resonant load and sweeps the input

HIGH FREQUENCY POWER GAIN

Figure 18.55

with a variable frequency signal current source. As the signal goes above and below the resonant frequency, the load becomes first capacitive and then inductive. If a high impedance sensitive detector is used to look at the input voltage, the changing impedance is seen at the input due to reflected load changes. At frequencies up to 5 or 10 mcs such detectors are available, but in the VHF range a different approach is used. The second approach, applicable at most frequencies, is to measure the feedback voltage appearing at the input when a signal is applied at the output. This is precisely what is done in measuring h_{rb}.

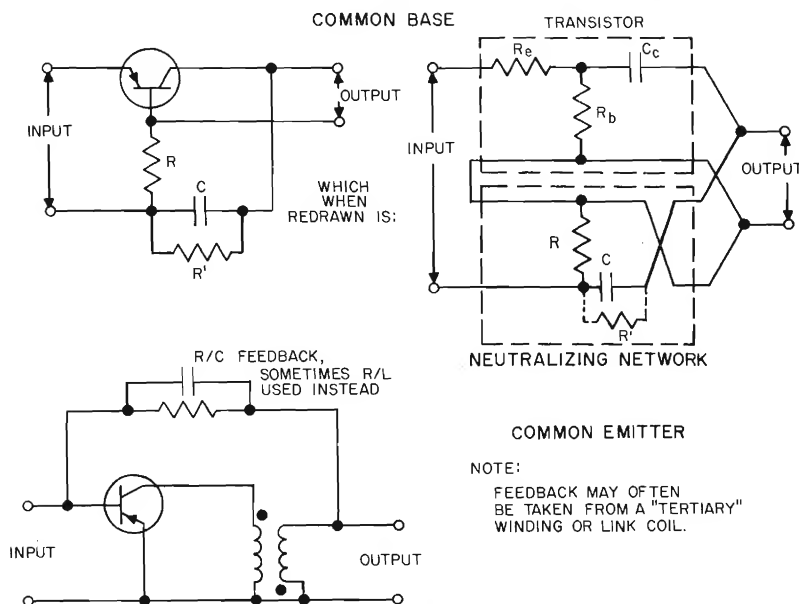
In both methods some out of phase feedback is applied in parallel with the device, so as to cancel either impedance changes or feedback voltage. Means of amplitude and phase control will need to be incorporated in the neutralizing network to avoid over-compensation. Simplified circuit diagrams are illustrated in Figure 18.56 to show some of the various feedback schemes used. The feedback networks are lumped-constant types at lower frequencies and transmission line types at VHF.

NEUTRALIZATION MEASUREMENTS

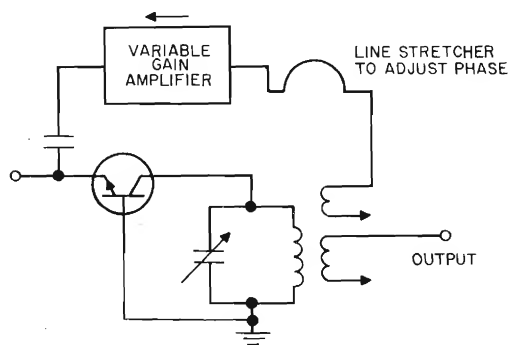
Figure 18.56

SCHEMATIC OF TRUE GAIN MEASUREMENT

Figure 18.57

To check the true gain of a transistor, unilateral amplifiers are used in the feedback path to supply the power consumed in the feedback (neutralizing) network, thereby not loading the transistor's output, as shown in Figure 18.57.

TRANSISTOR NOISE MEASUREMENTS

GENERAL

The noise output from an amplifier consists of two parts:

1. Output due to noise generated at the input-terminals.
2. Output due to noise generated inside the amplifier itself.

Part 1 of the noise power output is predictable since the available noise-power in any resistor is

$$P_n = kT\bar{B} \qquad (18a)$$

where,

k = Boltzman's constant

T = Absolute temperature (°K)

$\bar{B}$ = Effective bandwidth

and this effective bandwidth is

$$\bar{B} = \frac{1}{G}\int_0^\infty G(f)\, df \qquad (18b)$$

By measuring the gain with frequency, integrating and dividing by the maximum gain, the equivalent rectangular power pass-band is found. Since noise-power at the output consists of two parts, and one of these may be predicted, this may be used to specify the noisiness of an amplifier. The index used for this purpose is called the noise factor and is defined

$$F = \frac{\text{Total noise power out}}{\text{Power gain} \times \text{Noise power due to source resistor}} \qquad (18c)$$

or,

$$F = \frac{P_N}{G \cdot P_n}$$

But since, $G = \frac{(P_S)_{out}}{(P_S)_{in}}$, where P_S is signal power

$$F = \frac{P_N}{\frac{(P_S)_{out}}{(P_S)_{in}} \cdot P_n} = \frac{\frac{(P_S)_{in}}{P_n}}{\frac{(P_S)_{out}}{P_N}} = \frac{\left(\frac{\text{Signal}}{\text{Noise}}\right)_{in}}{\left(\frac{\text{Signal}}{\text{Noise}}\right)_{out}} \qquad (18d)$$

Noise Figure (NF) = 10 log F. Expressed in terms of voltage and resistance, the available noise-power can be written

$$P_n = \frac{\overline{E_n^2}}{4\,R_g} = KT\bar{B} \qquad (18e)$$

or,

$$\bar{E}_n = \sqrt{4\,KT\bar{B}\,R_g} \qquad (18f)$$

At room temperature, $4\,KT = 1.6 \times 10^{-20}$ joules.

MEASUREMENT OF NOISE FIGURE

In equation (18f) E_n is the noise voltage at the input. Now a signal is added at the input (γ times E_n) such that the output level with signal is much greater than the noise

output. This value γ is the signal-to-noise ratio and "calibrates" the output level of the entire measuring system. When the signal is removed, the output level should drop to $1/\gamma$ of this *calibrated* level provided the amplifier is perfect. Since the amplifier contributes some noise, the level will not drop that far. The ratio between the actual level of noise background and the *ideal* case is the noise factor and the noise figure may be read on the db scales of the VTVM used. Since the noise voltage fluctuates, sufficient capacitance must be added across the meter movement of the VTVM to integrate the noise voltage with time. If an average-reading meter (calibrated in RMS of a sine wave) is used, then the meter will read 11% lower on noise than on sinusoidal signals, and the "calibration" signal must be reduced accordingly for correct measurements. If a *true RMS* meter or bolometer is used, this correction is unnecessary.

Since the unknown signal is present during the calibration process, the measured Noise Figure is not the true Noise Figure.

According to equation (18d)

$$F = \frac{\left(\frac{\text{Signal}}{\text{Noise}}\right)_{in}}{\left(\frac{\text{Signal}}{\text{Noise}}\right)_{out}} \tag{18g}$$

The input during calibration is $S'_{in} = (P_S)_{in} + P_n$. The noise input is $N'_{in} = P_n$ and,

$$\frac{S'_{in}}{N'_{in}} = 1 + \frac{(P_S)_{in}}{P_n} \tag{18h}$$

The apparent output signal $S'_{out} = G\,[(P_S)_{in} + P_n] + P_E$. The apparent output noise $N'_{out} = GP_n + P_E$, where P_E is the noise generated in the transistor. Therefore,

$$\frac{S'_{out}}{N'_{out}} = \frac{G\,[(P_S)_{in} + P_n] + P_E}{GP_n + P_E} \tag{18i}$$

The measured noise factor

$$F_M = \frac{\frac{S'_{in}}{N'_{in}}}{\frac{S'_{out}}{N'_{out}}} = \frac{1 + \frac{(P_S)_{in}}{P_n}}{\frac{G\,[(P_S)_{in} + P_n] + P_E}{GP_n + P_E}} = \frac{1 + \frac{S_{in}}{N_{in}}}{1 + \frac{S_{out}}{N_{out}}} \tag{18j}$$

since $G\,(P_S)_{in}$ is the true output signal $= S_{out}$, and $GP_n + P_E$ is the true output noise $= N_{out}$.

By re-arranging equation (18j)

$$F_M = \frac{\frac{S_{in}}{N_{in}}}{\frac{S_{out}}{N_{out}}} \cdot \frac{1 + \frac{N_{out}}{S_{out}}}{1 + \frac{N_{in}}{S_{in}}} = F\,\frac{1 + \frac{N_{in}}{S_{in}}}{1 + \frac{N_{out}}{S_{out}}} \tag{18k}$$

or the true noise factor

$$F = F_M\,\frac{1 + \frac{N_{in}}{S_{in}}}{1 + \frac{N_{out}}{S_{out}}} \tag{18l}$$

From equation (18l) it is seen that if S_{out} is much greater than the noise background level F approaches F_M since this also implies $S_{in} >> N_{in}$.

One other complication is that the noise output of the transistor under test is far below the level of sensitivity of most commercially available meters, so that an amplifier must be used to raise the noise level to a readable level. Unfortunately, this amplifier can contribute noise of its own and degrade the readings.

It is easily shown that the total noise factor of a cascade system is

$$F_T = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1\,G_2} + \ldots\ldots \tag{18m}$$

So that G should be made as high and F_2 as low as possible to avoid these errors. (Removing the device under test while observing the noise background will supply a quick check on post-amplifier degradation. The output level should drop 20 db or more.)

A much more convenient way to make noise factor measurement is to use a noise diode. It is known that the output noise current from such a noise diode is

$$\overline{I_N^2} = 2q\,I_{DC}\,\overline{B} \qquad I_{DC} = \text{plate current in diode}$$
$$q = \text{electron charge} \qquad \overline{B} = \text{effective bandwidth} \tag{18n}$$

If the source resistance is R_g, the available noise power is

$$S_i = \frac{\overline{I_N^2}\,R_g}{4} = \frac{2q\,I_{DC}\,\overline{B}\,R_g}{4} \tag{18o}$$

This is the noise power generated by the diode alone. The noise power due to R_g is

$$N_i = KT\overline{B} \tag{18p}$$

and this is in addition to S_i.

The excess noise generated in the amplifier is N_E and the power gain is G and if M is defined as the ratio of noise power output with diode turned on to noise power output with diode turned off, then

$$M = \frac{\left(KT\overline{B} + \frac{2q\,I_{DC}\,\overline{B}\,R_g}{4}G + N_E\right)}{KT\overline{B}\,G + N_E} \tag{18q}$$

or,

$$M - 1 = \frac{\frac{2q\,I_{DC}\,\overline{B}\,R_g}{4}G}{KT\overline{B}\,G + N_E} \equiv \left(\frac{S}{N}\right)_{out} \tag{18r}$$

and since,

$$\left(\frac{S}{N}\right)_{in} = \frac{\frac{2q\,I_{DC}\,\overline{B}\,R_g}{4}}{KT\overline{B}} \tag{18s}$$

we have,

$$F = \frac{\left(\frac{S}{N}\right)_{in}}{\left(\frac{S}{N}\right)_{out}} = \frac{\frac{2q\,I_{DC}\,\overline{B}\,R_g}{4}}{M - 1} \tag{18t}$$

But at $T = 290°K\ (17°C)$, $\frac{2q}{4\,KT} = 20\ (\text{volts})^{-1}$

So equation (18t) can be written as

$$F = \frac{20\,I_{DC}\,R_g}{M - 1} \tag{18u}$$

Usually M is chosen to be equal to 2 therefore the noise factor is,

$$F = 20\,I_{DC}\,R_g \tag{18v}$$

EQUIVALENT NOISE CURRENT AND NOISE VOLTAGE

Because of the internally generated noise, the output noise current is not zero when the input is open, and for the same reason the output noise voltage is not zero when the

input is short-circuited. Since the noise current and noise voltage output are solely dependent on the transistor it seems that a noise specification based on those two quantities would be more generally useable. In the following derivation the relationship between open circuit noise current, short-circuit noise voltage and noise factor will be shown. A noisy amplifier may be substituted by a noise-less amplifier with equivalent noise-current and noise-voltage sources connected to the input, as shown in Figure 18.58.

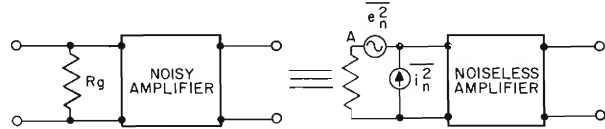



Figure 18.58 THEVENIN'S EQUIVALENT OF NOISY AMPLIFIER

The total noise-power at point A is proportional to

$$\overline{i_T^2} = \frac{4\,KT\overline{B}}{R_g} + \frac{\overline{e_N^2}}{R_g^2} + \overline{i_N^2} \qquad (18w)$$

The first term is the noise-current generated in R_g and since the noise factor,

$$F = \frac{\text{all noise}}{\text{noise due to } R_g}$$

then,

$$F = 1 + \frac{\overline{e_N^2}}{4\,KT\overline{B}\,R_g} + \frac{\overline{i_N^2}\,R_g}{4\,KT\overline{B}} \qquad (18x)$$

$$\overline{B} = \text{effective bandwidth} = \frac{1}{G_{MAX}} \int_0^\infty G(f)df$$

where,

$G(f)$ = gain as function of frequency
G_{MAX} = maximum gain.

Defining,

$$\left.\begin{aligned} R_{eqv} &= \frac{\overline{e_N^2}}{4\,KT\overline{B}} \\ I_{eqv} &= \frac{\overline{i_N^2}}{2\,q\overline{B}} \end{aligned}\right\} \qquad (18y)$$

equation (18x) will be,

$$F = 1 + \frac{R_{eqv}}{R_g} + \frac{2q\,I_{eqv}}{4\,KT} \qquad (18z)$$

and since,

$$\frac{2q}{4\,KT} = 20\ (\text{volts})^{-1} \text{ at } T = 290°K,$$

$$F = 1 + \frac{R_{eqv}}{R_g} + 20\,I_{eqv}\,R_g \qquad (18aa)$$

In Figure 18.58 the noise-voltage source may be thought of as a lossless resistor R_{eqv}, and the current source as a parallel shot noise generator due to an equivalent dc current I_{eqv}.

To find the optimum value on the noise factor the derivative of F equation (18x) is taken with respect to R_g, and this optimum noise factor is found to be

$$F_{opt} = 1 + \frac{\sqrt{\overline{e_N^2}\,\overline{i_N^2}}}{2\,KT\overline{B}} = 1 + 2\sqrt{20\,R_{eqv}\,I_{eqv}} \qquad (18bb)$$

for,

$$R_g = R_{opt} = \sqrt{\frac{\overline{e_N^2}}{\overline{i_N^2}}} = \sqrt{\frac{R_{eqv}}{20\,I_{eqv}}} \qquad (18cc)$$

From equation (18bb) it is seen that the optimum noise factor can be found analytically if $\overline{e_N^2}$ and $\overline{i_N^2}$ are known. This is also the noise factor which will be measured if a measurement is made with a source resistance R_{opt}.
Combining equations (18x) and (18bb).

$$F = 1 + \frac{F_{opt} - 1}{2}\left[\frac{R_g}{R_{opt}} + \frac{R_{opt}}{R_g}\right] \qquad (18dd)$$

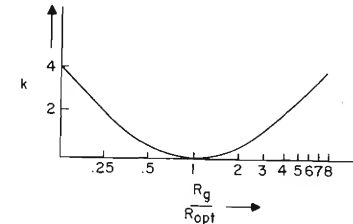
Therefore, if F_{opt} and R_{opt} are given, the noise factor can be found for any source resistance R_g.

Defining a factor k, as

$$k = \frac{1}{2}\left[\frac{R_g}{R_{opt}} + \frac{R_{opt}}{R_g}\right]$$

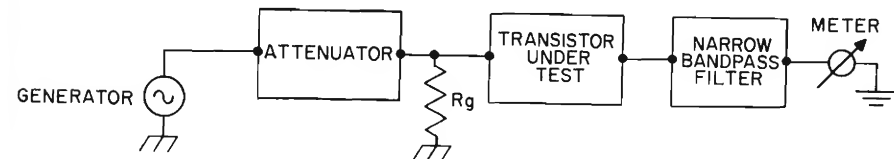
equation (18dd) becomes

$$F = 1 + (F_{opt} - 1)\,k \qquad (18ee)$$

FACTOR k VS. $\frac{R_g}{R_{opt}}$
Figure 18.59

For example, the optimum noise figure $(NF)_{opt}$ is given as 1.5 db or $F_{opt} = 1.4$. The optimum source-resistance is 1000 ohms. What is the noise factor in a circuit where $R_g = 8$ k ohms. The ratio $R_g/R_{opt} = 8$, and from the Figure 18.59, k is found to be 4. Therefore, the noise factor will be

$F = 1 + (F_{opt} - 1)\,k = 1 + (1.4 - 1) < 4 = 2.6$
$NF = 4.1$ db

MEASUREMENT OF $(\overline{e_N^2})^{1/2}$ AND $(\overline{i_N^2})^{1/2}$ FOR TRANSISTORS

The schematic in Figure 18.60 is used to measure $(\overline{e_N^2})^{1/2}$.

SET UP TO MEASURE $(\overline{e_N^2})^{1/2}$
Figure 18.60

R_g must be chosen so as to be much smaller than the input resistance of the transistor. It is known from transistor-analysis that

$$R_{eqv} \cong \frac{r_e}{2} + r_b'$$

To make $\frac{R_{eqv}}{R_g}$ in equation (18aa) the dominant term,

$$R_{eqv} >> R_g \text{ or } R_g << \frac{r_e}{2}$$

The measurement-procedure is as follows:

a. The back-ground noise-level is noted.

b. The signal generator is connected through a suitable attenuator, and the level of the generator is adjusted until the device output level is 20 db above back-ground level.

c. The required input level is measured from which e_n can be determined.

To measure the equivalent noise-current, an almost identical circuit is used. The only difference being R_g replaced by a high resistor inserted in series as shown in Figure 18.61.

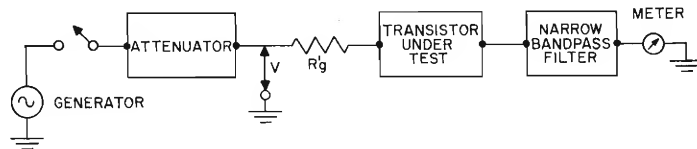



Figure 18.61 SET UP TO MEASURE $(\overline{i_N^2})^{1/2}$

A condition which must be satisfied is

$$\sqrt{\frac{4\,KTB}{R_g'}} << \sqrt{\overline{i_N^2}}$$

If the background noise level is V_n and the input voltage V gives E volts out, then equivalent noise-current is

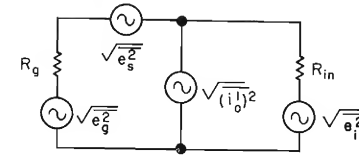
$$\overline{i_N} = \frac{V}{R_g} \cdot \frac{V_N}{E}$$

It should be strongly emphasized that $\overline{e_N}$ and $\overline{i_N}$ must be measured under the same operating conditions to have any practical significance, and also the necessary correction must be made for the lower meter reading on noise.

MEASUREMENT OF NOISE FACTOR WITHOUT USING SIGNAL GENERATOR OR NOISE DIODE

The concept of equivalent noise current and equivalent noise voltage can be used to measure noise factor without a signal generator or noise diode. Since the noise factor depends on the source resistance, and every resistor is a thermal noise source by nature, the source resistance can be utilized as a noise generator. The method is based on three measurements, from which the noise factor can be computed

1. The noise voltage at the output, input open-circuited.
2. The noise voltage at the output, input short-circuited.
3. The noise voltage at the output, the desired source resistance connected to the input.

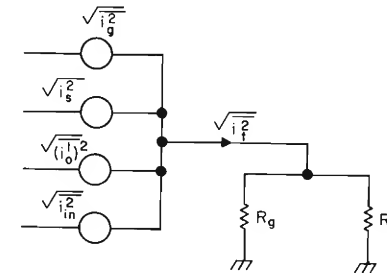
One necessary condition in this method is that the input resistance to the device be known, or be measurable.

EQUIVALENT NOISE CIRCUIT
Figure 18.62

$\sqrt{\overline{e_g^2}}$ is the noise voltage generated in the source resistance R_g

$\sqrt{\overline{e_s^2}}$ is the equivalent noise voltage, input shorted

$\sqrt{\overline{(i_o')^2}}$ is the true equivalent noise current, input open

$\sqrt{\overline{e_{in}^2}}$ is the noise voltage generated in the input resistance

The above circuit, Figure 18.62, is re-drawn as a current equivalent in Figure 18.63.

NOISE CURRENT EQUIVALENT CIRCUIT
Figure 18.63

The relationships between currents and voltages are

$$\overline{i_g^2} = \frac{\overline{e_g^2}}{R_g^2}\ ; \quad \overline{i_s^2} = \frac{\overline{e_s^2}}{R_g^2}\ ; \quad \overline{i_{in}^2} = \frac{\overline{e_{in}^2}}{R_{in}^2}$$

The total current flowing into the parallel combination of R_g and R_{in}

$$\overline{i_T^2} = \frac{\overline{e_g^2} + \overline{e_s^2}}{R_g^2} + \overline{(i_o')^2} + \frac{\overline{e_{in}^2}}{R_{in}^2} \qquad (18ff)$$

The measured open circuited equivalent noise voltage is due to

$$\overline{e_o^2} = \overline{(i_o')^2}\,R_{in}^2 + \overline{e_{in}^2} \qquad (18gg)$$

Combining (18ff) and (18gg) gives

$$\overline{i_T^2} = \frac{\overline{e_g^2} + \overline{e_s^2}}{R_g^2} + \frac{\overline{e_o^2}}{R_{in}^2} \qquad (18hh)$$

The noise factor

$$F = \frac{\overline{i_T^2}}{\overline{i_g^2}} = \frac{\dfrac{\overline{e_g^2} + \overline{e_s^2}}{R_g^2} + \dfrac{\overline{e_o^2}}{R_{in}^2}}{\dfrac{\overline{e_g^2}}{R_g^2}} = 1 + \frac{\overline{e_s^2}}{\overline{e_g^2}} + \frac{\overline{e_o^2}}{\overline{e_g^2}}\left(\frac{R_g}{R_{in}}\right)^2 \qquad (18ii)$$

From this last equation it is seen that F can be expressed in terms of voltage ratios; and, therefore, only output voltages have to be measured. Equation (18ii) is not too useful since we can not measure e_g separately.

The noise factor may also be expressed as,

$$F = \frac{[\text{total voltage across parallel } R_g \text{ and } R_{in}]^2}{[\text{voltage across parallel } R_g \text{ and } R_{in} \text{ due to } i_g]^2}$$

$$F = \frac{\overline{e_T^2}}{\overline{i_g^2}\left[\frac{R_g R_{in}}{R_g + R_{in}}\right]^2} = \frac{\overline{e_T^2}}{\overline{e_g^2}\left[\frac{R_{in}}{R_g + R_{in}}\right]^2} \qquad (18jj)$$

Multiplying both sides of (18jj) by $\overline{e_S^2}$ and solving for $\frac{\overline{e_S^2}}{\overline{e_g^2}}$

$$\frac{\overline{e_S^2}}{\overline{e_g^2}} = F \frac{R_{in}^2\, \overline{e_S^2}}{(R_{in} + R_g)^2\, \overline{e_T^2}} \qquad (18kk)$$

Substituting the identity,

$$\frac{\overline{e_o^2}}{\overline{e_g^2}} \equiv \frac{\overline{e_o^2}}{\overline{e_S^2}} \cdot \frac{\overline{e_S^2}}{\overline{e_g^2}}$$

and equation (18kk) into equation (18ii), and solving for F,

$$F = \frac{1}{1 - \frac{\overline{e_S^2}}{\overline{e_T^2}} \cdot \frac{1 + \frac{\overline{e_o^2}}{\overline{e_S^2}}\left(\frac{R_g}{R_{in}}\right)^2}{\left(1 + \frac{R_g}{R_{in}}\right)^2}} \qquad (18ll)$$

According to equation (18cc),

$$R_{opt} = \sqrt{\frac{\overline{e_N^2}}{\overline{i_N^2}}}$$

and since,

$$\overline{e_N^2} \equiv \overline{e_S^2}$$

and,

$$\overline{i_N^2} \equiv \frac{\overline{e_o^2}}{R_{in}^2}$$

$$R_{opt} = \sqrt{\frac{\overline{e_S^2}}{\overline{e_o^2}}}\, R_{in} \qquad (18mm)$$

and equation (18ll) becomes,

$$F = \frac{1}{1 - \frac{1 + \left(\frac{R_g}{R_{opt}}\right)^2}{\frac{\overline{e_T^2}}{\overline{e_S^2}}\left(1 + \frac{R_g}{R_{in}}\right)^2}} \qquad (18nn)$$

$\sqrt{\overline{e_T^2}}$ output voltage when R_g is connected to input

$\sqrt{\overline{e_S^2}}$ output voltage, input terminals shorted

$\sqrt{\overline{e_o^2}}$ output voltage, input terminals open

$$R_{opt} = R_{in} \sqrt{\frac{\overline{e_S^2}}{\overline{e_o^2}}}$$

R_{in} = input resistance of transistor.

Thus, the measurement of noise factor is accomplished without the use of a noise generator or diode.

TRANSISTOR NOISE ANALYZER

A more convenient way to measure equivalent noise voltage and current is to use the Quan Tech Transistor Noise Analyzer Model 310. This is an instrument where equivalent noise voltage and current can be read directly at three different center frequencies, namely at 100 cps, 1 kc, and 10 kc. The noise voltages and currents are read in volts per square root cycle ($V/\sqrt{\text{cycle}}$) and Amperes per square root cycle ($A/\sqrt{\text{cycle}}$).

Example:

Transistor 2N123

$V_{CE} = -5$ V

$I_E = 1$ mA

Equivalent short-circuited noise voltage $\overline{e_N} = 1.8 \times 10^{-9}\ V/\sqrt{\text{cycle}}$

Equivalent open-circuited noise current $\overline{i_N} = 2.5 \times 10^{-12}\ A/\sqrt{\text{cycle}}$

(measured at 1 kc)

This gives

$$R_{opt} = \frac{1.8 \times 10^{-9}}{2.5 \times 10^{-12}} = 720 \text{ ohms}$$

and

$$F_{opt} = 1 + \frac{e_N\, i_N}{2\,KT} = 1 + \frac{1.8 \times 2.5}{8} = 1.564$$

Optimum noise figure = 1.94 db.

CHARGE CONTROL PARAMETER MEASUREMENT

The measurement of the charge parameters (described in Chapter 6) are discussed in this section. The four parameters which are currently specified on G.E. specification sheets are measured in the manner shown in the following paragraphs. NPN configuration is used for circuit layouts, but PNP measurements can be accomplished by reversing the polarity of V_{in} and V_{CC}. One consideration which should be mentioned before the actual circuits are introduced is that of measurement accuracy. In any measurement of switching speed, determination of the pulse voltage magnitudes and the bias voltages is extremely critical. In these parameter measurements, an attempt was made to minimize the number of critical pulse and bias voltage measurements necessary.

τ_a, EFFECTIVE LIFETIME IN THE ACTIVE STATE

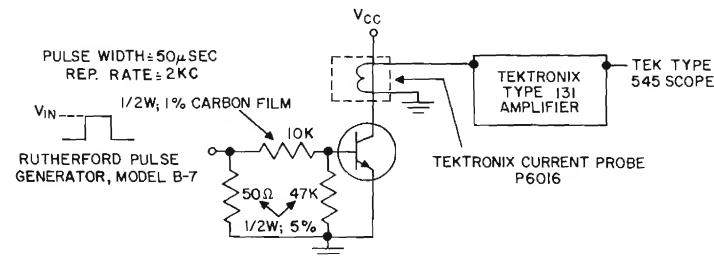
The circuit used to measure τ_a is shown in Figure 18.64. Inasmuch as the circuit

τ_a **TEST CIRCUIT**

Figure 18.64

contains no dissipation limiting resistor, extreme caution should be used to assure that $V_{CC} \cdot I_C$ does not exceed the dissipation limits of the device.

To perform the actual measurement, the following steps are taken:

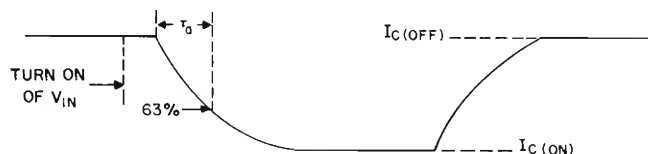
1. Before the device is inserted into the test socket, V_{in} amplitude is set to below + 0.3 volts.
2. V_{CC} is set to +4 volts. (This voltage may be lowered when dissipation is an important factor, but should not be made lower than +2 volts.)
3. A Tektronix Type 131 Amplifier and Tektronix Type 545 Oscilloscope (or equivalent) are set up so that the collector current at which measurement is desired produce a scope deflection equal to 3 cm. The current at which the measurements should be made is that I_C for which the device dissipation rating is approached by the $V_{CC} \cdot I_C$ product. This point is used for the measurement so that the τ_a obtained will be the true minimum and be accurate for "worst-case" design techniques.
4. The device is now inserted into the test socket. *CAUTION:* If the base lead accidently touches the collector lead during insertion, the device may be destroyed, unless an electrically current-limited power supply is used.
5. The input voltage is now increased until the I_C deflection is 3 cm (or the desired I_C value).
6. τ_a is the time constant of the resulting pulse waveform as shown in Figure 18.65. It is *not* necessary to record the input pulse amplitude.

τ_a **MEASUREMENT WAVEFORM**

Figure 18.65

τ_b, EFFECTIVE LIFETIME IN SATURATED STATE

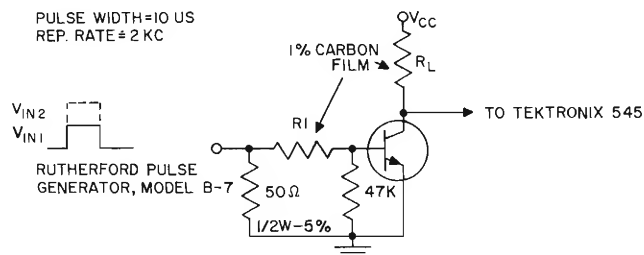
The test circuit for measuring τ_b is shown in Figure 18.66

τ_b **TEST CIRCUIT**

Figure 18.66

The following steps are taken to perform the τ_b measurement:

1. V_{CC} is chosen to be approximately one-half the transistor's breakdown voltage (about 10 volts for most alloy switching transistors).
2. R_L is chosen so the current flowing when the transistor is saturated is equal to a median current. (For alloy types where 100 ma is the maximum current permissible, R_L could be from 200 ohms to 1K for $V_{CC} = 10$ volts. In switching transistors of the mesa type, $V_{CC} = 10$ volts and $R_L = 1K$ are common conditions.)
3. R1 is normally from 2 to 5 times larger than R_L.
4. V_{in} is the quantity varied in order to make the τ_b measurement. The transistor is saturated at two different values of V_{in}, and the change in storage time is measured. Ease and accuracy of the measurement may be enhanced with the use of a Rutherford Model B7 pulse generator since V_{in} may be varied by the built-in decade attenuator.
5. The unit is inserted into the test circuit.
6. Two values of V_{in} are chosen which fulfill the conditions that the circuit β (forced β, forced h_{FE}, or $V_{CC}\,R1/V_{in}\,R_L$) is not more than ⅓ of the device h_{FE}.
7. The storage time portion of the trace is observed as shown in Figure 18.67. Only Δt_S and V_{in2}/V_{in1} need be recorded. Δt_S is observed as the V_{in} value is switched between V_{in1} and V_{in2} by manually switching the generator's pulse amplitude.
8. τ_b is obtained by using the relationship that $\tau_b = \dfrac{\Delta t_S}{\ln\left(\frac{V_{in2}}{V_{in1}}\right)}$.

(If $V_{in2} = 2.72\ V_{in1}$, then $\tau_b = \Delta t_S$.)

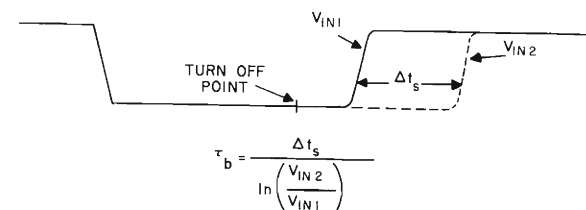



Figure 18.67 τ_b **MEASUREMENT WAVEFORM**

$\overline{C_{BE}}$, AVERAGE EMITTER JUNCTION CAPACITANCE

Figure 18.68 is circuit used to measure $\overline{C_{BE}}$. It should be noted that the input pulse used is to reverse bias the base emitter diode and is *not* of the polarity *which* would turn the base-emitter diode on. To obtain the actual value of $\overline{C_{BE}}$, the following steps are taken

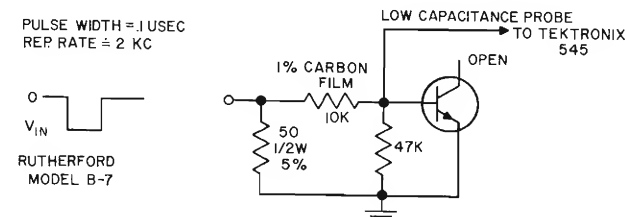
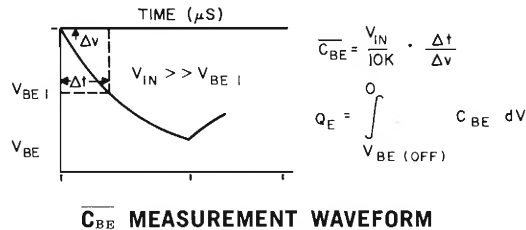
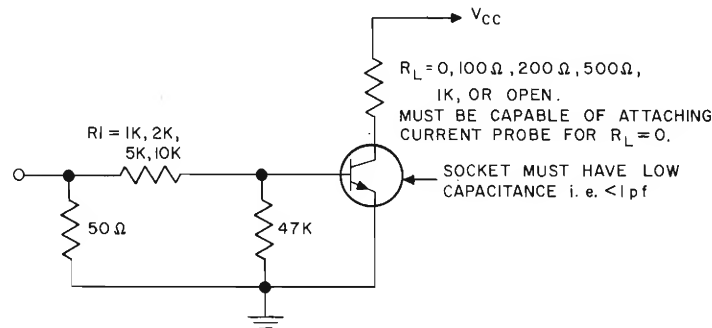



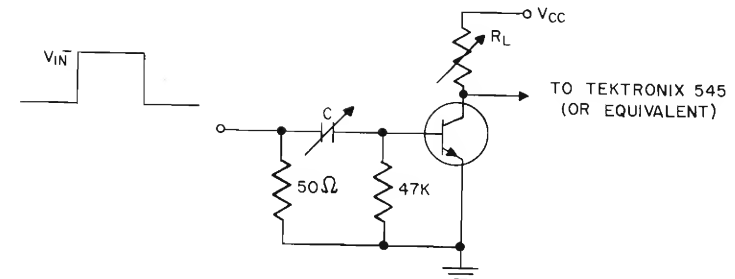
Figure 18.68 $\overline{C_{BE}}$ **TEST CIRCUIT**

1. Normally, V_{in} is from 10 to 20 volts and depends somewhat on junction breakdown voltage, i.e., 10 volts may be too high for a low breakdown unit.
2. Insert the transistor into the test socket.
3. V_{BE} transient is observed on the oscilloscope as shown in Figure 18.69. The value of $\overline{C_{BE}}$ is obtained from the relationship shown below the curve.
4. One measurement of capacitance is made to determine measurement gear capacity by performing the same steps with the test socket empty. Measurement gear capacitance is subtracted from the measured $\overline{C_{BE}}$ to determine the actual $\overline{C_{BE}}$.

$\overline{C_{BE}}$ MEASUREMENT WAVEFORM
Figure 18.69

COMPOSITE CIRCUIT FOR τ_a, τ_b, $\overline{C_{BE}}$

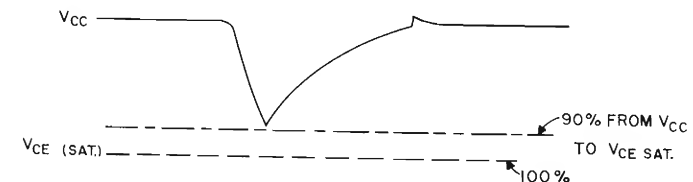
The similarity of the τ_a, τ_b, and $\overline{C_{BE}}$ test circuits allow that they may be combined in one flexible test circuit as shown in Figure 18.70. The appropriate R1 and R_L conditions allow for the various parameter measurements.

COMPOSITE CIRCUIT
Figure 18.70

Q_B*, TOTAL CHARGE TO BRING TRANSISTOR TO EDGE OF SATURATION

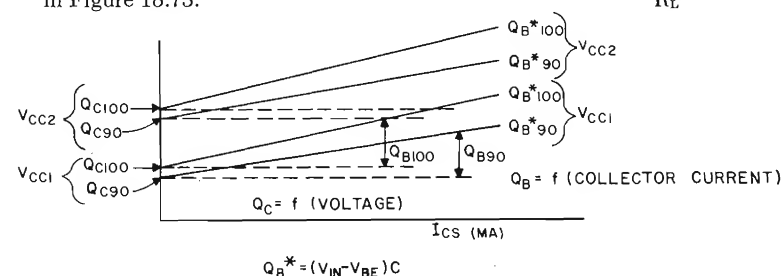
The circuit used to measure Q_B* is shown in Figure 18.71. Capacitor, C, is chosen to supply adequate charge to the device being tested without requiring an excessive V_{in} pulse. For alloy transistors a 5 to 100 pf variable capacitor with the capability of switching in additional capacitance, in steps of 100 pf, is used. Mesa transistors require a 3 to 50 pf range. It is important that low inductance capacitors be used. General

Q_B* TEST CIRCUIT
Figure 18.71

Radio precision capacitors, Hammarlund type air dielectric capacitors, or their equivalents are satisfactory. In any case, excessive capacity between the base lead and circuit ground must be avoided.

Q_B* is a function of collector voltage variation and collector current. Thus, measurements are made for various V_{CC} and R_L combinations. The following steps are taken to obtain Q_B* data.

1. V_{CC} is determined first. Several values of V_{CC} will be necessary to determine the full Q_B* picture; however, data is taken for one V_{CC} value and various R_L values. V_{CC} values of interest range from BV_{CEO} value to a value of 1 or 2 volts.
2. The unit is now inserted into the test socket.
3. The product $C(V_{in} - V_{BE})$ is the charge which is placed into the transistor to bring it to the edge of saturation. A value of V_{in} is chosen which is sufficient to permit enough charge to pass into the base of the transistor to bring it to the edge of saturation. This, of course, will also depend upon the range of capacitance available. V_{in} is normally between 5 and 20 volts, so that $V_{in} >> V_{BE}$. The capacitor used should be carefully chosen for large variation so as to render the test set more valuable.
4. With V_{CC} and V_{in} adjusted, data can be taken. Record the values of V_{CC} and V_{in}. A typical oscilloscope pattern is shown in Figure 18.72.

Q_B* COLLECTOR WAVEFORM
Figure 18.72

As C is increased, the peak of the waveform will approach $V_{CE(SAT)}$. C_{90} is the value of capacitance necessary for the peak to reach 90% of the waveform from V_{CC} to $V_{CE(SAT)}$, while C_{100} is the value of capacitance necessary for the peak of the waveform to reach $V_{CE(SAT)}$.

5. $Q_B{}^*{}_{90}$ and $Q_B{}^*{}_{100}$ are the products of C_{90} $(V_{in} - V_{BE})$ and C_{100} $(V_{in} - V_{BE})$ respectively. $Q_B{}^*$ values are then plotted against I_{CS} (i.e., $\frac{V_{CC} - V_{CE(SAT)}}{R_L}$) as shown in Figure 18.73.

$Q_B{}^*$ PLOT VS. I_{CS}
Figure 18.73

These plots are generally linear over a wide collector current and voltage range for alloy and diffused transistors. The intercept on the $Q_B{}^*$ axis is called Q_C and is the part of $Q_B{}^*$ which varies with collector voltage. The part of $Q_B{}^*$ which varies with I_{CS} is called Q_B. Thus, $Q_B{}^* = Q_B + Q_C$. If desired, Q_B and Q_C can also be plotted separately.

CALIBRATION OF CAPACITOR, C, ON $Q_B{}^*$ TEST SET

A simple method of calibrating the capacitor on the $Q_B{}^*$ test set is available if the circuit in Figure 18.74 is used. The fact that the reactance of the capacitor at 1.59 mc (frequency chosen for convenience) is large compared to 10 ohms, permits the 10 ohm resistor to be used as a current measuring device. Looking at the equations

$$X_C = (2\pi f C)^{-1}$$
$$V_{in} = I X_C$$

or,

$$C = (2\pi f X_C)^{-1} = \frac{I}{2\pi f V_{in}}$$

If $V_{in} = 1$ volt RMS and $f = 1.59$ mc, then,

$$C = (I)\ 10^{-7}$$

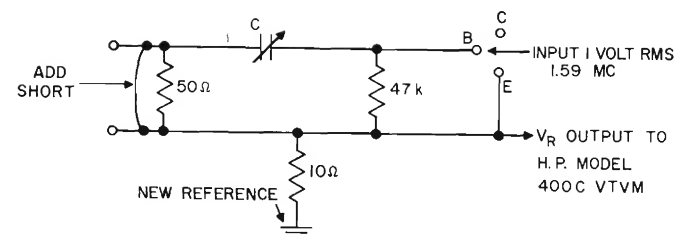
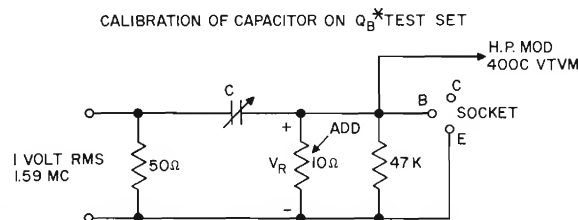
Using the 10 ohms to measure current,

$$I = V_R/10 \text{ ohms}$$

therefore,

$$C = V_R\ (10^{-8}).$$

Thus, the VTVM reading, V_R, is used to calibrate C, and 0.1 mv RMS indicates 1 pf, etc.

CAPACITOR CALIBRATION
Figure 18.74

STRAY CAPACITANCE MEASUREMENT
Figure 18.75

If it is desirable to know the stray capacitance from the base to emitter in the test circuit, a similar measurement can be made as shown in Figure 18.75. The variable capacitor is set at a known value, say C_1, so $C_{stray} = V_R\ (10^{-8}) - C_1$. Note that in this determination of stray capacitance the normal circuit reference has been changed. Care must be taken to insure that the old reference is not shorted to the new test reference.

NOTES

CHAPTER 19

THE TRANSISTOR SPECIFICATION SHEET & SPECIFICATIONS

PLANAR EPITAXIAL TRANSISTORS

NPN

SILICON TYPES
2N2193
2N2193A
2N2194
2N2194A
2N2195
2N2195A

This family of General Electric devices are PLANAR EPITAXIAL transistors designed for high speed switching and high frequency amplifier circuits.

FEATURES:
- Low Leakage Current
- Low $V_{CE(SAT)}$
- Guaranteed current gain from 0.1 to 1000 ma.
- High Breakdown Voltage

absolute maximum ratings (25°C unless otherwise specified)

		2N2193 2N2193A	2N2194 2N2194A	2N2195 2N2195A	
Voltage					
Collector to Base	V_{CBO}	80	60	45	volts
Collector to Emitter	V_{CEO}	50	40	25	volts
Emitter to Base	V_{EBO}	8	5	5	volts
Current					
Collector	I_C	1.0	1.0	1.0	amp
Transistor Dissipation					
(Free Air 25°C) *	P_T	0.8	0.8		watts
(Free Air 25°C) **	P_T			0.6	watts
(Case Temperature 25°C) ***	P_T	2.8	2.8	2.8	watts
(Case Temperature 100°C) ***	P_T	1.6	1.6	1.6	watts
Temperature					
Storage	T_{STG}	←	−65 to +300	→	°C
Operating Junction	T_J	←	−65 to +200	→	°C

*Derate 4.6 mw/°C increase in ambient temperature above 25°C
**Derate 3.4 mw/°C increase in ambient temperature above 25°C
***Derate 16.0 mw/°C increase in case temperature above 25°C

DIMENSIONS WITHIN JEDEC OUTLINE TO-5

NOTE 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed .010.

NOTE 2: Measured from max. diameter of the actual device.

NOTE 3: The specified lead diameter applies in the zone between .050 and .250 from the base seat. Between .250 and 1.5 maximum of .021 diameter is held. Outside of these zones the lead diameter is not controlled. Leads may be inserted, without damage, in .031 holes while transistor enters .371 hole concentric with lead hole circle.

electrical characteristics: (25°C unless otherwise specified)

		2N2193 2N2193A Min.	Max.	2N2194 2N2194A Min.	Max.	2N2195 2N2195A Min.	Max.	
DC CHARACTERISTICS								
Collector to Base Voltage ($I_C = 100\ \mu a$)	V_{CBO}	80		60		45		volts
Collector to Emitter Voltage ($I_C = 25$ ma)†	V_{CEO}	50		40		25		volts
Emitter to Base Voltage ($I_E = 100\ \mu a$)	V_{EBO}	8		5		5		volts
Forward Current Transfer Ratio								
($I_C = 150$ ma, $V_{CE} = 10$ V)†	h_{FE}	40	120	20	60	20		
($I_C = 10$ ma, $V_{CE} = 10$ V)	h_{FE}	30		15				
($I_C = 1000$ ma, $V_{CE} = 10$ V)†	h_{FE}	15						
($I_C = 0.1$ ma, $V_{CE} = 10$ V)	h_{FE}	15						
($I_C = 500$ ma, $V_{CE} = 10$ V)†	h_{FE}	20		12				
($I_C = 10$ ma, $V_{CE} = 10$ V, $T_A = -55$°C)	h_{FE}	20						
Base Saturation Voltage ($I_C = 150$ ma, $I_B = 15$ ma)	$V_{BE(SAT)}$		1.3		1.3		1.3	volts
Collector Saturation Voltage ($I_C = 150$ ma, $I_B = 15$ ma)	$V_{CE(SAT)}$	(0.35 volts max., 2N2193, 94, 95 only)						
	$V_{CE(SAT)}$	(0.25 volts max., 2N2193A, 94A, 95A only)						
	$V_{CE(SAT)}$	(0.16 volts typ., 2N2193A, 94A, 95A only)						
CUTOFF CHARACTERISTICS								
Collector Leakage Current ($V_{CB} = 30$ V)	I_{CBO}				10		100	mμa
($V_{CB} = 30$ V, $T_A = 150$°C)	I_{CBO}				25		50	μa
($V_{CB} = 60$ V)	I_{CBO}		10					mμa
($V_{CB} = 60$ V, $T_A = 150$°C)	I_{CBO}		25					μa
Emitter Base Cutoff Current ($V_{EB} = 5$ V)	I_{EBO}		50					mμa
Emitter Base Leakage Current ($V_{EB} = 3$ V)	I_{EBO}				50		100	mμa
HIGH FREQUENCY CHARACTERISTICS								
Current Transfer Ratio ($I_C = 50$ ma, $V_{CB} = 10$ V, f = 20 mc)	h_{fe}	2.5		2.5		2.5		
Collector Capacitance ($I_E = 0$, $V_{CB} = 10$ V, f = 1 mc)	C_{ob}		20		20		20	pf
SWITCHING CHARACTERISTICS (See Figure 1) ($V_{BB} = 15$V, $V_{cc} = 15$V)								
Rise Time	t_r		70		70			nsec
Storage Time	t_s		150		150			nsec
Fall Time	t_f		50		50			nsec

†Pulse width ≤300 μsec, duty cycle ≤2%

GENERAL ELECTRIC

Part 1—The Transistor Specification Sheet

The published transistor specification sheet is fully as important as the device it describes since it provides the description necessary for sensible use of the subject transistor.

Four general categories of information are presented. These are

1. a statement of broad device capabilities and intended service
2. absolute maximum ratings
3. electrical characteristics
4. generic or family electrical characteristics

Let's study each of these categories in some detail and use the specification sheet for 2N2193 through 2N2195 as a guide.

1. GENERAL DEVICE CAPABILITIES

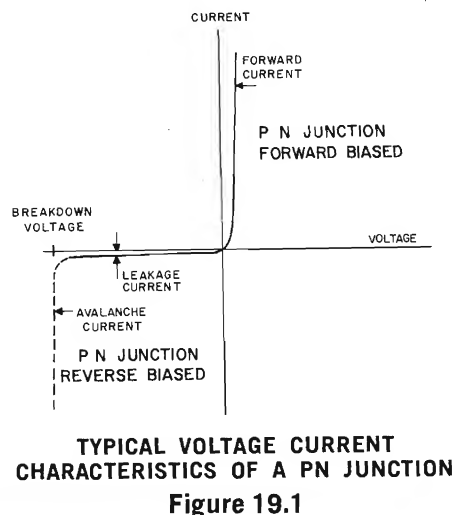
The lead paragraph found at the top of the sheet furnishes the user with a concise statement of the most likely applications and salient electrical characteristics of the device. It is useful in first comparison of devices as one selects the proper device for a particular application.

2. ABSOLUTE MAXIMUM RATINGS

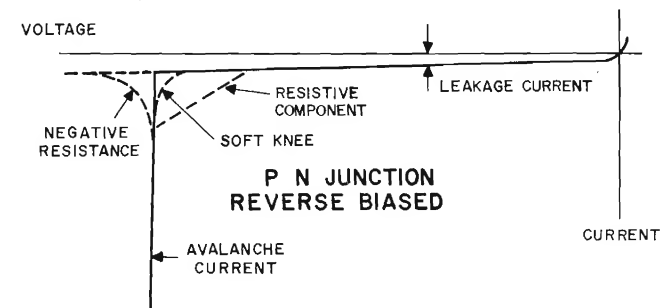
Absolute maximum ratings specify those electrical, mechanical, and thermal ratings of a semiconductor device which, as limiting values, define the maximum stresses beyond which either initial performance or service life is impaired.

VOLTAGE

The voltages specified in the *Absolute Maximum Ratings* portion of the sheet are breakdown voltages with reverse voltage applied to one selected junction, or across two junctions with one junction reverse biased and the second junction in some specified state of bias. Single junction breakdown either between collector and base or between emitter and base has the form shown in Figure 19.1.

TYPICAL VOLTAGE CURRENT CHARACTERISTICS OF A PN JUNCTION
Figure 19.1

The solid portion of the curve is the active, normally used portion of a diode or any compound junction device. The dotted portion exhibits large dramatic changes in reverse current for small changes in applied voltage. This region of abrupt change is called the *breakdown* region. If breakdown occurs at relatively low voltage, the mechanism is through tunneling or "zener" breakdown. The means of conduction is through electrons which have "tunneled" from valence to conduction energy levels. A more complete explanation of tunneling is contained in the Tunnel Diode Manual.*

At higher voltage levels conduction is initiated and supported by solid ionization. When the junction is reverse biased, minority current flow (leakage current) is made up of holes from the n-type material and electrons from the p-type material. The high field gradient supplies carriers with sufficient energy to dislodge other valence electrons, raising their energy level to the conduction band resulting in a chain generation of hole-electron pairs. This process is called *avalanche*. While theory predicts an abrupt, sharp (sometimes called *hard*) characteristic in the breakdown region, a *soft* or gradual breakdown often occurs. Another possibility is the existence of a negative resistance "hook." The hook usually occurs when zener breakdown is the predominant mechanism. Figure 19.2 graphically illustrates these possibilities. In practice, silicon, because of lower leakage current, exhibits a sharper knee than does germanium.

TYPICAL VARIATIONS IN BREAKDOWN CHARACTERISTIC OF A PN JUNCTION
Figure 19.2

The family of the 2N2193 to 2N2195 silicon devices are measured for individual junction breakdown voltages at a current of 100 microamperes. V_{CBO}, the collector-base diode breakdown voltage— with emitter open circuited or floating — is shown to be a minimum of 80 volts for the 2N2193 and 2N2193A.

V_{EBO}, the emitter-base breakdown voltage — with collector open circuited or floating — is specified at 8 volts minimum for the 2N2193 and 2N2193A.

The breakdown voltage between collector and emitter is a more complex process. The collector-base junction in any configuration involving breakdown is always reverse biased. On the other hand, the condition applied to the emitter-base diode depends upon the nature of base lead connection. The most stringent requirement is realized by allowing the base to float. The next most stringent requirement is connecting the

*See references at end of Chapter 1.

base to the emitter through a resistor. A more lenient measurement is with base and emitter shorted. Finally, the condition yielding the highest breakdown voltage is that which applies reverse bias to the emitter-base junction. The symbols for the breakdown voltage, collector to emitter, under the foregoing base connection conditions are V_{CEO}, V_{CER}, V_{CES}, and V_{CEX} respectively. On some specification sheets the letter B, signifying breakdown, precedes the voltage designation, i.e., BV_{CEO}.

The generic shape of breakdown characteristics differs among transistors fabricated by different processes. Figure 19.3 is typical of the planar epitaxial 2N2193. Note that the BV_{CEO} curve exhibits little current flow (I_{CEO}) until breakdown is initiated. At breakdown a region of negative resistance appears and disappears at increased collector voltage. The region of negative resistance is not suitable for measurement and specification because of instability. The low current positive resistance region below (in voltage) the breakdown region is so low as to cause instrumentation difficulties. It is desirable, therefore, to measure breakdown voltage at a current, in the breakdown region, where the slope is positive. This current for the 2N2193 family is 25 ma.

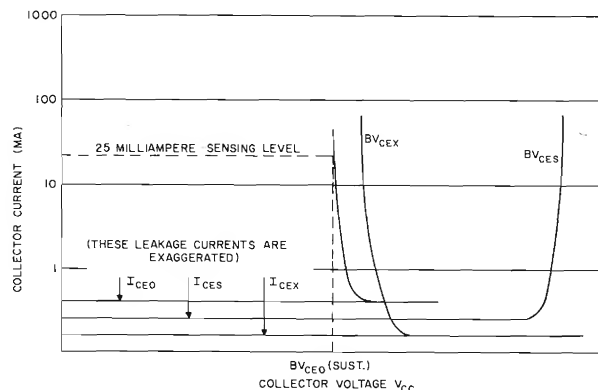
Since BV_{CER} and BV_{CEX} as well as BV_{CEO} exhibit a negative resistance region, they must also be measured in a region of positive resistance. The voltage thus measured is always less than voltage needed to establish breakdown. For this reason it has been suggested that these voltages be named differently than breakdown voltages. One proposal is to designate them as "sustaining" voltages with the prefix letter L substituted for B, i.e., LV_{CER}. The nomenclature $V_{CER\,(SUST.)}$ has also been used.

TYPICAL PLANAR EPITAXIAL COLLECTOR BREAKDOWN CHARACTERISTICS

Figure 19.3

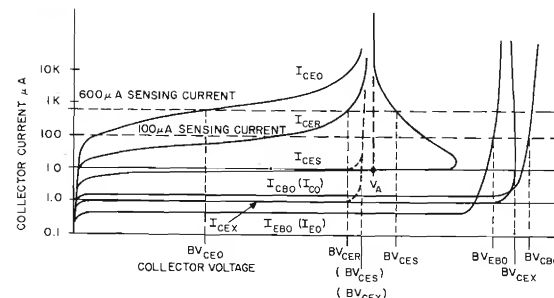
The behavior of alloy devices is sufficiently different to warrant separate consideration. Figure 19.4 illustrates a typical family of breakdown characteristics. Since leakage currents are appreciable in this class of devices they form an important part of breakdown consideration. In the specification of BV_{CEO}, consideration must be given to I_{CO} multiplication. In this connection I_{CEO} is approximately $h_{FE} \times I_{CO}$. This product may exceed 100 μa (the usual BV_{CBO} sensing current) at voltages well below breakdown. For this reason it is common to specify breakdown at a collector current of 600 μa. Figure 19.4 shows the realistic increase in voltage resulting from the use of a 600 μa sensing current. The earlier statement that BV_{CEO} is a very conservative rating is particularly true of germanium alloy devices. It is primarily applicable to circuits with little or no stabilization.

TYPICAL FAMILY OF ALLOY TRANSISTOR BREAKDOWN CHARACTERISTICS

Figure 19.4

BV_{CES} is measured with the base shorted to the emitter. It is an attempt to indicate more accurately the voltage range in which the transistor is useful. In practice, using a properly stabilized circuit, such as those described in Chapter 4, the emitter junction is normally forward biased to give the required base current. As temperature is increased, the resulting increase in I_{CO} and h_{FE} requires that the base current decrease if a constant, i.e., stabilized, emitter current is to be maintained. In order that base current decrease, the forward bias voltage must decrease. A properly designed biasing circuit performs this function. If temperature continues to increase the biasing circuit will have to reverse bias the emitter junction to control the emitter current. This is illustrated by Figure 4.1 which shows that $V_{BE} = 0$ when $I_C = 0.5$ ma at 70°C for the 2N525. $V_{BE} = 0$ is identically the same condition as a base to emitter short as far as analysis is concerned. Therefore, the BV_{CES} rating indicates what voltage can be applied to the transistor when the base and emitter voltages are equal, regardless of the circuit or environmental conditions responsible for making them equal. Figure 3.4 indicates a negative resistance region associated with I_{CES}. At sufficiently high currents the negative resistance disappears. The 600 μa sensing current intersects I_{CES} in the negative resistance region in this example. Oscillations may occur depending on the circuit stray capacitance and the circuit load line. In fact, "avalanche" transistor oscillators are operated in just this mode.

Conventional circuit designs must avoid these oscillations. If the collector voltage does not exceed V_A (Figure 19.4) there is no danger of oscillation. V_A is the voltage at which the negative resistance disappears at high current.

To avoid the problems of negative resistance associated with BV_{CES}, BV_{CER} was introduced. The base is connected to the emitter through a specified resistor. This condition falls between BV_{CEO} and BV_{CES} and for most germanium alloy transistors avoids creating a negative resistance region. For most low power transistors the resistor is 10,000 ohms. The significance of BV_{CER} requires careful interpretation. At low voltages the resistor tends to minimize the collector current as shown by equation (3s), in Chapter 3. Near breakdown the resistor becomes less effective permitting the collector current to increase rapidly.

Both the value of the base resistor and the voltage to which it is returned are important. If the resistor is connected to a forward biasing voltage the resulting base drive may saturate the transistor giving the illusion of a collector to emitter short. Returning the base resistor to the emitter voltage is the standard BV_{CER} test condition. If the resistor is returned to a voltage which reverse biases the emitter junction, the

collector current will approach I_{CO}. For example, many computer circuits use an emitter reverse bias of about 0.5 volts to keep the collector current at cut-off. The available power supplies and desired circuit functions determine the value of base resistance. It may range from 100 to 100,000 ohms with equally satisfactory performance provided the reverse bias voltage is maintained.

In discussing the collector to emitter breakdown so far, in each case the collector current is I_{CO} multiplied by a circuit dependent term. In other words all these collector to emitter breakdowns are related to the collector junction breakdown. They all depend on avalanche current multiplication.

Another phenomenon associated with collector to emitter breakdown is that of *reach-through* or *punch-through.* Silicon devices as typified by grown diffused, double diffused, planar, mesa, and planar epitaxial structures do not exhibit this characteristic. The phenomenon of reach-through is most prevalent in alloy devices having thin base regions, and lighter base region doping than collector region doping. As reverse voltage is increased the depletion layer spreads more in the base than in the collector and eventually "reaches" into the emitter. An abrupt increase in current results.

The dotted lines in Figure 19.4 indicate the breakdown characteristics of a reach through limited transistor. Several methods are used to detect reach through. BV_{CEX} (breakdown voltage collector to emitter with base reverse biased) is one practical method. The base is reverse biased by 1 volt. The collector current I_{CEX} is monitored. If the transistor is avalanche limited BV_{CEX} will approach BV_{CBO}. If it is reach-through limited it will approach BV_{CES}.

Note that I_{CEX} before breakdown is less than I_{CO}. Therefore, if I_{CO} is measured at a specified test voltage and then the emitter is connected with a reverse bias of 1 volt, the I_{CO} reading will decrease if reach-through is above the test voltage and will increase if it is below.

"Emitter floating potential" is another test for reach-through. If the voltage on an open-circuited emitter is monitored while the collector to base voltage is increased, it will remain within 500 mv of the base voltage until the reach-through voltage is reached. The emitter voltage then increases at the same rate as the collector voltage. V_{RT} is defined as $(V_{CB} - 1)$ where V_{CB} is the voltage at which $V_{EB} \doteq 1v$.

CURRENT

The absolute maximum collector current, shown as 1 ampere for the 2N2193, is a pulse current rating. In this case it is the maximum collector current for which h_{FE} is specified. In some cases the current level at which h_{FE} drops from its maximum value by 50% is specified. In all cases judgement concerning adverse life affects is a major consideration. Also in all cases no other absolute maximum rating can be exceeded in using this rating. In cases of very short, high current pulses, the power dissipated in transition from cutoff to saturation must be considered so that thermal ratings are not exceeded.

TRANSISTOR DISSIPATION

Transistor dissipation ratings are thermal ratings, verified by life test, intended to limit junction temperature to a safe value. Device dissipation is shown for three cases. The first indicates the transistor in free air at an ambient temperature of 25°C. The 2N2193 under these conditions is capable of dissipating 0.8 watt. Further, we must derate at a rate of 4.6 mw/°C for an ambient temperature above 25°C. This thermal derating factor can be interpreted as the absolute maximum thermal conductance

junction to air, under the specified conditions. If dissipation and thermal conductance are specified at 25°C case temperature an infinite heat sink is implied and both dissipation and thermal conductance reach their largest allowable values. For the 2N2193 these are 2.8 watts and 16 mw/°C respectively.

Both free air and infinite heat sink ratings are valuable since they give limit application conditions from which intermediate (in thermal conductance) methods of heat sinking may be estimated.

TEMPERATURE

The 2N2193 family carries a storage temperature rating extending from −65°C to +300°C. High temperature storage life tests substantiate continued compliance with the upper temperature extreme. Further, the mechanical design is such that thermal/mechanical stresses generated by rated temperature extremes cause no electrical characteristic degradation.

Operating junction temperature although stated implicitly by thermal ratings is also stated explicitly as an absolute maximum junction temperature.

3. ELECTRICAL CHARACTERISTICS

Electrical characteristics are the important properties of a transistor which are controlled to insure circuit interchangeability and describe electrical parameters.

DC CHARACTERISTICS

The first characteristics shown are the voltage ratings, repeated in the order of the absolute maximum ratings, but this time showing the conditions of test. Note that these and subsequent electrical parameters are measured at 25°C ambient temperature unless otherwise noted. The 2N2193 has the highest rated breakdown voltages of the series at $V_{CBO} = 80V$, $V_{CEO} = 50V$, and $V_{EBO} = 8V$.

Forward current transfer ratio, h_{FE}, is specified over four decades of collector current from 100 microamperes to 1 ampere. Such wide range in collector current is feasible only in transistors having very small leakage currents. Note that h_{FE} measurements at 150, 500 and 1000 ma. are made at a 2% duty cycle and pulse widths less than or equal to 300 microseconds. This precaution is necessary to avoid exceeding thermal ratings. Both the 2N2193 and 2N2193A have a specified minimum current gain at −55°C. A collector current of 10 ma. was chosen as being most useful to the circuit designer who wishes to predict low temperature circuit performance.

Base saturation, $V_{BE\ (SAT)}$, specifies the base input voltage characteristic under the condition of both junctions being foreward biased. The conditions of measurement specify a base current of 15 ma. and a collector current of 150 ma. Base-emitter drop is then 1.3 volts. This parameter is of particular interest in switch designs and is covered in further detail in Chapter 3 (Equations 3u & 3v).

Collector saturation voltage, $V_{CE\ (SAT)}$, is the electrical characteristic describing the voltage drop from collector to emitter with both base-emitter and collector-base junctions foreward biased. Base and collector currents are stipulated. For the 2N2193 through 2N2195 these are 15 ma. and 150 ma. respectively. The quotient of collector and base currents is termed "forced beta."

The principal difference between "A" and "non-A" versions of the 2N2193 family lie in their maximum collector saturation voltages. "A" versions exhibit 0.16 volts typically and are specified at 0.25 volts maximum. The "non-A" versions are specified at 0.35 volts maximum. It is interesting to note that the 1.05 volt (minimum) difference

between $V_{BE\ (SAT)}$ and $V_{CE\ (SAT)}$ is the level of false trigger (noise immunity level) for DCTL switches. In germanium alloy devices this level is generally less than 0.3 volt and is seldom greater than 0.7 volt in other silicon devices (see Chapter 6). The wide difference in $V_{BE\ (SAT)}$ and $V_{CE\ (SAT)}$ is undesirable if Darlington connection of devices is desired for saturated switching. The collector saturation characteristic of the compound device demonstrates that the lead section is incapable of saturating the output section. Modification of the circuit to provide separate connection of the input section collector directly to the joint collector supply will provide the needed $V_{BE\ (SAT)}$ to allow output section saturation.

CUTOFF CHARACTERISTICS

Chapter 1 contains a detailed study of transistor leakage currents. This examination deals with phenomena which predominate in alloy structures. The principal differences in planar epitaxial devices lie in the relative magnitudes of the leakage current components. The complete protection afforded by the passivation layer reduces surface leakage to a very small value. Further, it reduces the surface thermal component by decreasing recombination velocity. Figure 1.25(B) shows the variation with temperature of I_{CBO} for units of the 2N2193 family. It is interesting to note that the theoretical semi-log plot of I_{CBO} vs. temperature is a straight line. At high temperatures planar devices follow predicted behavior quite well. At lower temperatures, the temperature rate is considerably less than that which would be predicted by the theoretical model.

The 25°C I_{CBO} and I_{EBO} maximum limits are both 100 nanoamperes. I_{CBO} rises to 25 microamperes at 150°C, typically, and carries a 150°C upper limit of 50 μa.

HIGH FREQUENCY CHARACTERISTICS

The small-signal foreward current transfer ratio, h_{fe}, is shown as a minimum of 2.5 at 20 mc. This parameter is specified for those amplifier applications requiring control of high frequency h_{fe}. Chapter 18 treats the measurement of high frequency h_{fe} in detail. See also Chapter 2.

SWITCHING CHARACTERISTICS

Chapters 6 and 18 on switching and measurements, respectively, discuss and define transient response times t_d, t_r, t_s, and t_f. The circuit used to measure t_r, t_s, and t_f is shown in Figure 19.5. The specified maximum *rise, storage,* and *fall times* are measured in this circuit. The base of the transistor under test is clamped at approximately −1.5 volts by the diode returned to a −1 volt bus. As the point V_{in} is raised in potential the base is unclamped and the transistor moved through the active region to saturation. As noted in the referenced chapters, the switching times measured are highly circuit

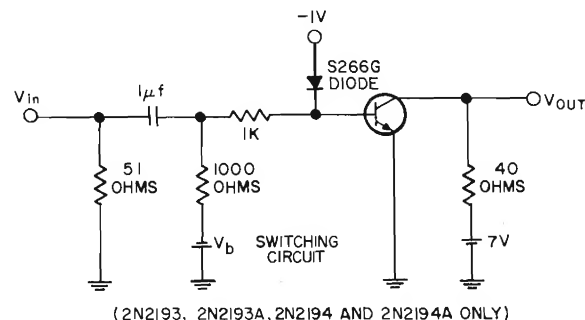



Figure 19.5

dependent. By the time this description is published more thorough switching characterization will be made available, which specify t_d, t_r, t_s, and t_f as a function of the ratio of collector current to foreward base current (forced beta).

GENERIC CHARACTERISTICS

Much information about the behavior of semiconductor devices is conveyed by showing *typical* behavior. This information is presented graphically and differs from other electrical specifications by not bearing the high statistical assurance associated with maximum and minimum limits. Statistical confidence is assigned the generic characteristics of some devices by showing 5th, 50th, and 95th percentile points of a given characteristic. This sort of specification is found as part of very thoroughly characterized devices such as the 2N335 and 2N396.

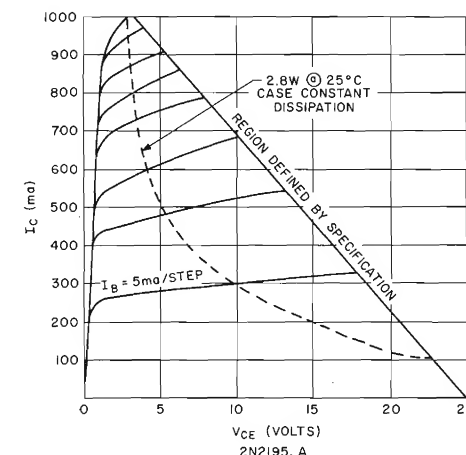
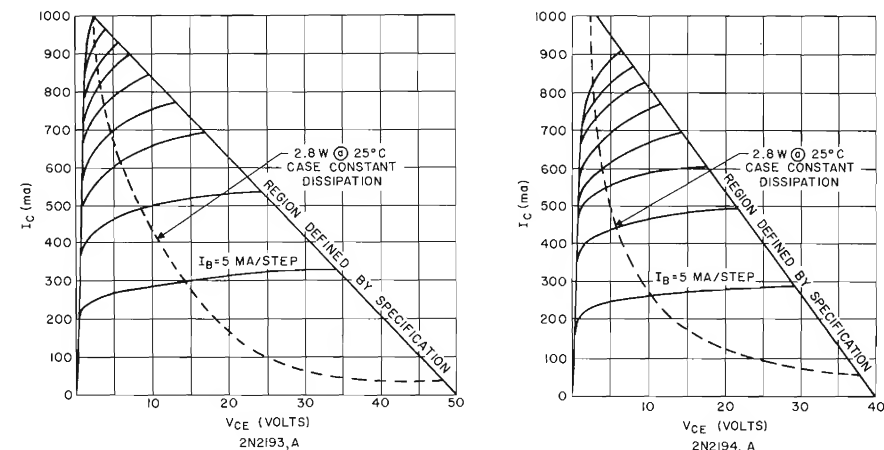



Figure 19.6

The specification sheet for the 2N2193 family includes collector family data for the 2N2193, 2N2194 and 2N2195 and associated "A" versions. The hyperbola of constant 2.8 watt 25°C dissipation is shown in Figure 3.6 to demark the area of permissible static operation as defined by previously discussed thermal limitations. In addition, a triangular area bounded by the collector current and collector voltage axes and a line noted as "region defined by specification" is specified. This area is one that defines the safe boundary for transient operation and should at no time be exceeded.

Semiconductor manufacturers go to great lengths in constructing their product specification sheets because they realize the value of offering the designer adequate information. If the device described therein is to be of use to the design engineer, is to be used properly for optimum performance and reliability by the designer within the limits specified by the manufacturer, the specification sheet must be accurate, complete, and reliable. This requires precise and time consuming measurements, coupled with costly hours of anlysis and preparation of the final specification sheet. The transistor specification sheet is, without doubt, the most important work tool the electronics circuit designer has at his disposal. When understood by the designer and used intelligently, many labor hours can be saved.

EXPLANATION OF PARAMETER SYMBOLS

SYMBOL ELEMENTS

A	Ampere (a.c., r.m.s or d.c.), ambient, anode electrode
a	Ampere (peak or instantaneous)
B, b	Base electrode, breakdown
C, c	Capacitance, collector electrode, cathode electrode
Δ	(Delta) A small change in the value of the indicated variable
E, e	Emitter electrode
F, f	Frequency, forward transfer ratio
G, g	Gain, acceleration of gravity, gate electrode
h	General symbol for hybrid parameter
I, i	Current, input, intrinsic region of device
J, j	Reference electrode
K, k	Unspecified (general) measurement electrode. Also degrees Kelvin
L, l	Inductance
N, n	n-region of semiconductor device
O, o	Output, open circuit
P, p	Power, p-region of semiconductor device
Q	Charge
R, r	Resistance, reverse transfer ratio
T	Temperature
t	Time

V	Voltage (max., avg. or rms)
v	Volt (peak or instantaneous)
W	Watt (max., avg. or rms)
w	Watt (peak or instantaneous)
X	Unspecified (general) parameter
Y	General symbol for an admittance parameter
θ	(Theta) Thermal resistance
Z, z	General symbol for impedance, impedance parameter

DECIMAL MULTIPLIERS

Prefix	Symbols	Multiplier	Prefix	Symbols	Multiplier
tera	T	10^{12}	centi	c	10^{-2}
giga	G	10^{9}	milli	m	10^{-3}
mega	M or Meg	10^{6}	micro	μ	10^{-6}
kilo	K or k	10^{3}	nano	n	10^{-9}
hecto	h	10^{2}	pico	p	10^{-12}
deka	da	10	femto	f	10^{-15}
deci	d	10^{-1}	atto	a	10^{-18}

PARAMETER SYMBOLS

BV_{CBO}	*Dc breakdown voltage collector to base junction reverse biased, emitter open-circuited (value of I_C should be specified).
BV_{CEO}	*Dc breakdown voltage, collector to emitter, with base open-circuited. This may be a function of both "m" (the charge carrier multiplication factor) and the h_{fb} of the transistor. Specify I_C.
BV_{CER}	*Dc breakdown voltage, similar to BV_{CEO} except a resistor value "R" between base and emitter.
BV_{CES}	*Dc breakdown voltage, similar to BV_{CEO} but base shorted to emitter.
BV_{CEV}	*Dc breakdown voltage, similar to BV_{CEO} but emitter to base junction reverse biased.
BV_{CEX}	*Dc breakdown voltage, similar to BV_{CEO} but emitter to base junction reverse biased through a specified circuit.
BV_{EBO}	*Dc breakdown voltage, emitter to base junction reverse biased, collector open-circuited. Specify I_E.
BV_R	Dc breakdown voltage, reverse biased diode.
C_c	Barrier capacitance.
C_{eb}	*(Common base) capacitance emitter to base, collector open.
C_{ij}	Input capacitance.
C_{ob}	*(Common base) collector to base } Output capacitance measured across the output terminals.
C_{oe}	*(Common emitter) collector to emitter. } Output capacitance measured across the output terminals.

*Test conditions must be specified.

Symbol	Definition
f	Frequency at which measurement is performed.
f_{hfb} (f_{ab})	(Common base) small-signal short-circuit forward current transfer ratio cut-off frequency.
f_{hfe} (f_{ae})	(Common emitter) small-signal short-circuit forward current transfer ratio cut-off frequency.
f_{max} (f_{osc})	Maximum frequency of oscillation.
f_t	Gain bandwidth product frequency at which the small signal, common emitter, short-circuit, forward current, transfer ratio (h_{fe}) is unity or zero db.
$-g$	Negative conductance.
G_{pb}	*(Common base) small-signal power gain.
G_{PE}	*(Common emitter) large-signal power gain.
G_{pe}	*(Common emitter) small-signal power gain.
$G_{pe\ (CONV.)}$	*(Common emitter) conversion gain.
h_{fb}	(Common base) — Small-signal short-circuit forward current transfer ratio, output ac short-circuited.
h_{fc}	(Common collector) — Small-signal short-circuit forward current transfer ratio, output ac short-circuited.
h_{fe}	(Common emitter) — Small-signal short-circuit forward current transfer ratio, output ac short-circuited.
h_{fj}	(General) — Small-signal short-circuit forward current transfer ratio, output ac short-circuited.
h_{FE}	*(Common emitter) static value of forward current transfer ratio, $h_{FE} = \frac{I_C}{I_B}$
h_{FE} (inv.)	Inverted h_{FE} (emitter and collector leads switched)
h_{ib}, h_{ie}, h_{ic}, h_{ij}	(Common base, common emitter, common collector, general) small-signal input impedance, output ac short-circuited.
h_{IE}	(Common emitter) static value of the input resistance.
h_{ie} (real)	(Common emitter) real part of the small-signal value of the short-circuit input impedance at high frequency.
h_{ob}, h_{oe}, h_{oc}, h_{oj}	(Common base, common emitter, common collector, general) small-signal, output admittance, input ac open-circuited.
h_{rb}, h_{re}, h_{rc}, h_{rj}	(Common base, common emitter, common collector, general) small-signal, reverse voltage transfer ratio, input ac open-circuited.
I, i	Region of a device which is intrinsic and in which neither holes nor electrons predominate.

*Test conditions must be specified.

Symbol	Definition
I_B, I_C, I_E	Dc currents into base, collector, or emitter terminal.
I_b	Base current (rms)
i_b	Base current (instantaneous)
I_{BX}	Dc base current with both the emitter and collector junctions reverse biased.
I_c	Collector current (rms)
i_c	Collector current (instantaneous)
I_{CBO} (I_{CO})	*Dc collector current when collector junction is reverse biased and emitter is open-circuited.
I_{CEO}	*Dc collector current with collector junction reverse biased and base open-circuited.
I_{CER}	*Dc collector current with collector junction reverse biased and a resistor of value "R" between base and emitter.
I_{CES}	*Dc collector current with collector junction reverse biased and base shorted to emitter.
I_{CEV}	*Dc collector current with collector junction reverse biased and with a specified base-emitter voltage.
I_{CEX}	*Dc collector current with collector junction reverse biased and with a specified base-emitter circuit connection.
I_e	Emitter current (rms)
i_e	Emitter current (instantaneous)
I_{EBO} (I_{EO})	*Dc emitter current when emitter junction is reverse biased and collector is open-circuited.
I_{ECS}	*Dc emitter current with emitter junction reverse biased and base shorted to collector.
I_F	*Dc forward current.
i_F	Forward current (instantaneous).
I_P	Peak point current.
I_P/I_V	Peak to valley current ration.
I_R	Reverse current (dc).
i_R	Reverse current (instantaneous).

I_V	Valley point current.
L_c	Conversion loss – ratio of available signal power to the available intermediate frequency power.
L_S	Total series inductance.
N, n	Region of a device where electrons are the majority carriers.
η	Intrinsic stand-off ratio (unijunction).
NF	Noise figure.
P, p	Region of a device where holes are the majority carriers.
p_t (peak)	Peak collector power dissipation for a specified time duration, duty cycle and wave shape.
P_C	Average continuous collector power dissipation.
P_o	Power output.
pt (peak)	Peak total power dissipation for a specified time, duration, duty cycle and wave shape.
P_T	Average continuous total power dissipation.
Q_{SB}	Stored base charge.
r_b'	Base spreading resistance equals h_{ie} (real) when h_{ie} (imaginary) = 0.
r_{B1B20} (r_{BBO})	Device resistance between base 1 and base 2, emitter open-circuited (interbase resistance – unijunction).
$r_{CE(SAT)}$	Device resistance, collector to emitter, under saturation conditions (saturation resistance, steady state).
RE	Rectification efficiency (voltage).
R_{KJ}	Circuit resistance between terminals K and J.
R_L	Load resistance.
r_s	Small signal series resistance.
T_A	Operating temperature (ambient)
T_J	Junction temperature

T_{STG}	Storage temperature
V_{KJ}	Circuit voltage between terminals K and J.
V_P	Peak point voltage.
V_R	Dc reverse voltage.
V_{RT}	Dc voltage reach-through (formerly called punch-through C_{PT}). At collector voltages above reach-through $V_{RT} = V_{CB} - V_{EB}$. (V_{EB} normally defined as 1 volt).
V_V	Valley point voltage.
y_{fj}	Small signal short circuit forward transfer admittance.
z_{ij}	Input impedance.
z_{oj}	Output impedance.

NOTE: DC voltage and current terminologies (as listed herein) are valid only when measurements are made under non-oscillating conditions. Care must be exercised with avalanche transistors as they may oscillate when making these measurements and give erroneous readings.

ABBREVIATED DEFINITIONS OF TERMS

1. Absolute Maximum Ratings – the value when so specified is an "absolute limit" and the device is not guaranteed if it is exceeded.

2. Applied Voltage – voltage applied between a terminal and the reference point.

*3. Constant Current – one that does not produce a parameter value change greater than the required precision of the measurement when the generator impedance is halved.

*4. Constant Voltage – one that does not produce a parameter value change greater than the required precision of the measurement when the genrator impedance is doubled.

*5. Breakdown Voltage (BV) – that value of applied reverse voltage which remains essentially constant over a considerable range of current values, or where the incremental resistance = 0 at the lowest current in avalanche devices.

6. Limits – the minimum and maximum values specified.

7. Noise Figure (NF) – at a selected input frequency, the noise figure (usually 10 log of base 10 of ratio) is the ratio of the total noise power per unit bandwidth at a corresponding output frequency delivered to the output termination, to the portion thereof engendered at the input frequency by the input termination, (whose noise temperature is standard 290°K).

*Test conditions must be specified.

8. Open Circuit — a condition such that halving the magnitude of the terminating impedance does not produce a change in the parameter measured greater than the required precision of the measurement.

9. Pulse — a flow of energy of short duration which conveys intelligence.

10. Pulse Average Time (t_w) — the time duration from a point on the leading edge which is 50% of the maximum amplitude to a point on the trailing edge which is 50% of the maximum amplitude.

11. Pulse Delay Time (t_d) — the time interval from a point on the leading edge of the input pulse which is 10% of its maximum amplitude to a point on the leading edge of the output pulse which is 10% of its maximum amplitude.

12. Pulse Fall Time (t_f) — the time duration during which the amplitude of its trailing edge decreases from 90 to 10% of the maximum amplitude.

13. Pulse Rise Time (t_r) — the time duration during which the amplitude of its leading edge increases from 10 to 90% of the maximum amplitude.

14. Pulse Storage Time (t_s) — the time interval from a point 10% down from the maximum amplitude on the trailing edge of the input pulse to a point 10% down from the maximum amplitude on the trailing edge of the output pulse.

15. Pulse Time (t_p) — the time interval from a point on the leading edge which is 90% of the maximum amplitude to a point on the trailing edge which is 90% of the maximum amplitude.

16. Short Circuit — a condition where doubling the magnitude of the terminating impedance does not produce a change in the parameter being measured that is greater than the required precision of the measurement.

17. Small Signal — a signal is considered small when halving its magnitude does not produce a change in the parameter being measured that is greater than the required precision of the measurement.

18. Spike — an unintended flow of electrical energy of short duration.

19. Supply Voltage (V_{BB}, V_{CC}, V_{EE}) — the potential of the circuit power source.

20. Thermal Equilibrium — a condition where doubling the test time does not produce a change in the parameter that is greater than the required precision of the measurement.

21. Thermal Resistance (Θ) — the temperature rise per unit power dissipation of the junction above the device case or ambient temperature under conditions of steady-state operation (where applicable, "case" means device mounting surface).

22. Thermal Response Time (γ_r) — the time required for the junction temperature to reach 90% of the final value of junction temperature change caused by a step function in power dissipation when the device case or ambient temperature is held constant.

23. Thermal Time Constant (γ_t) — the time required for the junction temperature to reach 63.2% of the final value of junction temperature change caused by step function in power dissipation when the device case or ambient temperature is held constant.

24. Base Voltage (V_{BJ}) — the voltage between the base terminal and the reference point (J).

25. Collector Voltage (V_{CJ}) — the voltage between the collector terminal and the reference point (J).

26. Cut-off Current (I_{KJO}, I_{KJR}, I_{KJS}, I_{KJV}, I_{KJX}) — the measured value of (K) electrode dc current when it is reverse-biased by a voltage less than the breakdown voltage and the other electrode(s) is (are) dc open-circuited (I_{KJO}) or

1. returned to the reference electrode (J) through a given resistance (I_{KJR})
2. dc short circuited to the reference electrode (J) (I_{KJS})
3. reverse-biased by a specified voltage (I_{KJV})
4. under a specified set of conditions different from the above (I_{KJX}).

27. Depletion Layer Capacitance (C dep) — the transition capacitance of a reverse-biased pn junction. (Small signal as well as dc conditions to be stated).

28. Diffusion Capacitance (C dif) — the transition capacitance of a forward biased (with an appreciable current flow) pn junction.

29. Emitter Voltage (V_{EJ}) — the voltage between the emitter terminal and the reference point (J).

30. Floating Potential (V_{KJF}) — the dc voltage between the open circuit terminal (K) and the reference point (J) when a dc voltage is applied to the third terminal and the reference terminal.

31. Input Capacitance (C_{ij}) — the shunt capacitance at the input terminals.

32. Input Terminals — the terminals to which input voltage and current are applied.

33. Inverse Electrical Characteristics [$X_{KJ\,(INV)}$] — those characteristics obtained when the collector and emitter terminals are interchanged.

34. Large-signal Short Circuit Forward-current Transfer Ratio (h_{FJ}) — ratio of the change in output current (ΔI_o) to the corresponding change in input current (ΔI_I).

35. Large-signal Transconductance (G_{MJ}) — the ration of the change in output current (ΔI_o) to the corresponding change in input voltage (ΔV_I).

36. Large-signal Power Gain (G_P) — the ratio of the ac output power to the ac input power under the large signal conditions. Usually expressed in decibels (db). (ac conditions must be specified).

37. Maximum Frequency of Oscillation (f_{osc} or f_{max}) — the highest frequency at which a device will oscillate in a particular circuit.

38. Output Capacitance (C_{oj}) — the shunt capacitance at the output terminals.

39. Output Terminals — the terminals at which the output voltage and current may be measured.

40. Power Gain Cut-off Frequency (f_{pj}) — that frequency at which the power output has dropped 3 db from its value at a reference test frequency ($G_P(f)$ = constant) with constant input power.

41. Reach Through Voltage (V_{RT}) (formerly referred to as "punch through voltage") — that value of reverse voltage at which the reverse-biased pn junction spreads sufficiently to electrically contact any other junction or contact, and thus act as a short circuit.

42. Real Part of Small-signal Short-circuit Input Impedance [h_{ij}(real)] — the real part of the ratio of ac input voltage to the ac input current with zero ac output voltage.

43. Reference Point (electrical) – the terminal that is common to both the input and output circuits.

44. Saturation Resistance [$r_{KJ(SAT)}$] – the ratio of saturation voltage to the measurement (K) electrode dc current.

45. Saturation Voltage [$V_{KJ(SAT)}$] – the dc voltage between the measurement electrode (K) and the reference electrode (J) for the saturation conditions specified.

46. Small-signal Open-circuit Forward Transfer Impedance (z_{fj}) – the ratio of the ac output voltage to the ac input current with zero ac output current.

47. Small-signal Open-circuit Input Impedance (z_{ij}) – the ratio of the ac input voltage to the ac input current with zero ac output current.

48. Small-signal Open-circuit Output Admittance (h_{oj}) – the ratio of the ac output current to the ac voltage applied to the output terminals with zero ac input current.

49. Small-signal Open-circuit Output Impedance (z_{oj}) – the ratio of the ac voltage applied to the output terminals to the ac output current with zero ac input current.

50. Small-signal Open-circuit Reverse Transfer Impedance (z_{rj}) – the ratio of the ac input voltage to the ac output current with zero ac input current.

51. Small-signal Open-circuit Reverse Voltage Transfer Ratio (h_{rj}) – the ratio of the ac input voltage to the ac output voltage with zero ac input current.

52. Small-signal Power Gain (G_p) – the ratio of the ac output power to the ac input power. Usually expressed in db.

53. Small-signal Short-circuit Forward Current Transfer Ratio (h_{fj}) – the ratio of the ac output current to the ac input current with zero ac output voltage.

54. Small-signal Short-circuit Forward Current Transfer Ratio Cut-off Frequency (f_{hfj}) – the frequency in cycles per second (cps) at which the absolute value of this ratio is 0.707 times its value at the test frequency specified ($G_p(f)$ = constant).

55. Small-signal Short-circuit Forward Transfer Admittance (y_{fj}) – the ratio of the ac output current to the ac input voltage with zero ac output voltage.

56. Small-signal Short-circuit Input Impedance (h_{ij}) – the ratio of the ac input voltage to the ac input current with zero ac output voltage.

57. Forward Voltage (V_{FP}) – highest value of positive voltage at which the forward current equals the maximum specified peak point current ($I_F = I_P$).

58. Peak Point Current (I_P) – value of the static current flowing at the lowest positive voltage at which $d_I/d_V = 0$.

59. Peak Point Voltage (V_P) –the lowest positive voltage at which $d_I/d_V = 0$.

60. Peak to Valley Ratio I_P/I_V – the ratio of peak point current to valley point current.

61. Valley Point Current (I_V) – the value of the static current flowing at the second lowest positive voltage at which $d_I/d_V = 0$.

62. Valley Point Voltage (V_V) – the second lowest positive voltage at which $d_I/d_V = 0$.

Part 2–Specifications

This portion of Chapter 19 consists of three parts:

Since a semiconductor device, such as a transistor, can be specified and characterized in any number of ways and under a variety of *test conditions* it is at best difficult to offer detailed data on all types in a book of this nature. The presentation of detailed information describing an individual device is more the purpose of the specification sheet (see Part 1 of this chapter). Seasoned circuit designers will always refer to the semiconductor device manufacturer's specification sheet as a prime source of electrical and physical data when designing. But this usually comes after device "selection."

If the circuit designer is to approach his design intelligently, he must first know what devices are available to do the circuit job he has in mind; it is at this point that the following selection charts will be valuable since they allow him to take a broad look over the manufacturer's line of products (in this case G. E. Semiconductors) with the hope of filling his device requirements thus leading to circuit design success.

To find General Electric — *Turn to page*

*For other General Electric Product information see Chapter 20.

SILICON TRANSISTORS

ECONOMY NPN Planar (See Outline Drawing No. 1)

Small Signal Amplifiers — Audio to 30mc (16A Product Line)

Type	h_{FE} $V_{CE}=4.5v$ $I_C=2$ ma	h_{fe} $V_{CE}=10v$ $I_C=2$ ma F=1 kc	V_{CEO} $I_C=1$ ma Volts	P_T milliwatts	C_{OB} $V_{CE}=10v$ pfd	f_t Typical mc	Comments
2N2711	30-90	—	18	200	7	120	RF Converter, IF, Audio Driver & Output for AM & CB Radio.
2N2712	75-225	—					
2N2715(16D)	30-90	—	18	200	4	120	RF Converter, IF for AM & CB Radio.
2N2716(16D)	75-225	—					
2N2921	—	35-70	25	200	7	120	Higher Collector Voltage and 2 to 1 AC Beta (h_{fe}) Spread for Consumer and Industrial Applications.
2N2922	—	55-110					
2N2923	—	90-180					
2N2924	—	150-300					
2N2925	—	235-470					
2N2926	—	35-470	18	200	7	120	Low Cost Spread Type.
2N3390	400-800	—	25	200	7	120	Optimized Types for Ultra High Beta, Low Noise, 2 to 1 DC Beta (h_{FE}) Spreads, High Collector Voltage For Consumer & Industrial Applications.
2N3391	250-500	—					
2N3391A	250-500	—					
2N3392	150-300	—					
2N3393	90-180	—					
2N3394	55-110	—					
2N3395	150-500	—					Combines 2N3391 and 2N3392
2N3396	90-500	—					Combines 2N3392 and 2N3393.
2N3397	55-500	—					Combines 2N3391, 2, 3, 4.
2N3398	55-800	—					Combines 2N3390, 1, 2, 3, 4.

High Frequency Amplifiers and Oscillators — 10 mc to 950 mc Epitaxial (16G Product Line)

Type	h_{FE}	h_{fe}	V_{CEO}	P_T	C_{OB}	f_t	Comments
16G1	20 Min	—	$V_{CBO}=18$	200	1.3	1000	TV & FM Tuner, IF and UHF Oscillators.
16G2			$V_{CBO}=30$				

High Frequency Amplifier — 10 mc-250 mc, for Forward AGC (16K Product Line)

Type	h_{FE}	h_{fe}	V_{CEO}	P_T	C_{OB}	f_t	Comments
16K	60 Typ. @ $I_C=4$ ma.	—	30	200	1.1	1000	Forward AGC, VHF RF and IF Amplifiers (TV & FM).

High Frequency Amplifiers and Oscillators — 262.5 kc to 100 mc Epitaxial (16L Product Line)

Type	h_{FE}	h_{fe}	V_{CEO}	P_T	C_{OB}	f_t	Comments
16L2	20-40	—	30	200	2.5	250	Very Low 2 mc Noise for AM RF Stages.
16L3	35-70	—				300	
16L4	60-120	—				350	
16L22	20-40	—	30	200	2.5	250	Low 2 mc Noise for AM Converter Stages.
16L23	35-70	—				300	
16L24	60-120	—				350	
16L25	100-320	—	30	200	2.5	400	High h_{FE} for IF Stages.
16L42	20-40	—	18	200	2.5	250	General Purpose Types for FM and TV.
16L43	35-70	—				300	
16L44	60-120	—				350	
16L62	20-40	—	30	200	2.5	250	High Frequency Applications in FM and TV.
16L63	35-70	—				300	
16L64	60-120	—				350	

Large Signal Amplifiers and Medium Speed Switch — Epitaxial (16N Product Line)

Type	h_{FE}	h_{fe}	V_{CEO}	P_T	C_{OB}	f_t	Comments
2N2713(16B)	30-90	—	18	200	7.0	120	Medium Power & Voltage, Low V_{SAT}, h_{FE} Hold-up to 200 ma.
2N2714(16B)	75-225	—					
2N3402	75-225	—	25	900 (Attached Heatsink See Dwg. No. 2)	8.0	120	High Power, Medium, Voltage Low V_{SAT}, h_{FE} Hold-up to 500 ma.
2N3403	180-540	—					
2N3404	75-225	—	50		8.0	120	High Power, High Voltage, Low V_{SAT}, h_{FE} Hold-up to 500 ma.
2N3405	180-540	—					
2N3414	75-225	—	25	360	8.0	120	Medium Power, Medium Voltage, Low V_{SAT}, h_{FE} Hold-up to 500 ma.
2N3415	180-540	—					
2N3416	75-225	—	50	360	8.0	120	Medium Power, High Voltage, Low V_{SAT}, h_{FE} Hold-up to 500 ma.
2N3417	180-540	—					

High Speed Switch — Low Storage Time, Typical ≅30 nsec. Epitaxial, Gold Doped (16J Product Line)

Type	h_{FE}	h_{fe}	V_{CEO}	P_T	C_{OB}	f_t	Comments
16J1	30 Min @ $I_C=10$ ma.	—	14	200	4.0	350	Similar to 2N914.
16J2							Similar to 2N708.

GROWN DIFFUSED — NPN Passivated

(See Outline Drawing No. 3)

Type	h_{fe}	h_{FE}	BV_{CBO}	I_{CBO}	C_{OB}	P_T	Comments
	V_{CB}=5 v I_E=1 ma f=1 kc	TYPICAL V_{CE}=5 v I_C=1 ma	MINIMUM I_{CBO}= 50 μa I_E=0 volts	MAXIMUM V_{CB}=30 v I_E=0 T_A=25°C μa	TYPICAL V_{CB}=20v I_E=−1 ma f=1 mc. pf	MAXIMUM Power Diss. mw	
2N332	9-22	14	45	1.0	4	150	Audio Amplifiers Astable Oscillators Chopper Circuits Flip-flop Circuits Logic Circuits RF Amplifiers
2N332A	9-22	14	45	.5	4	500	
2N333 (13)	18-44	27	45	1.0	4	150	
2N333A	18-44	27	45	.5	4	500	
2N334	18-90	36	45	1.0	4	150	
2N334A	18-90	36	45	.5	4	500	
2N335 (13)	37-90	45	45	1.0	4	150	
2N335A	37-90	45	45	.5	4	500	
2N335B	37-90	45 (12)	60	.5	4	500	
2N336 (13)	76-333	75	45	1.0	4	150	
2N336A	76-333	75	45	.5	4	500	
2N337 (13)	55 (1)	20-55 (11)	45	1.0 (6)	2	125	
2N337A	55 (1)	20-55 (11)	45	.5	2	500	
2N338 (13)	99 (1)	45-150 (11)	45	1.0 (6)	2	125	
2N338A	99 (1)	45-150 (11)	45	.5	2	500	

Type	h_{fe}	h_{FE}	BV_{CBO}	I_{CBO}	C_{OB}	P_T	Comments
2N470	10-25	—	15	.5	2	200	Audio Amplifiers Astable Oscillators Chopper Circuits Flip-flop Circuits Logic Circuits RF Amplifiers
2N471	10-25	—	30	.5	2	200	
2N471A	10-25	—	30	.5	2	200	
2N472	10-25	—	45	.5	2	200	
2N472A	10-25	—	45	.5	2	200	
2N473	20-50	—	15	.5	2	200	
2N474	20-50	—	30	.5	2	200	
2N474A	20-50	—	30	.5	2	200	
2N475	20-50	—	45	.5	2	200	
2N475A	20-50	—	45	.5	2	200	
2N478	40-100	—	15	.5	2	200	
2N479	40-100	—	30	.5	2	200	
2N479A	40-100	—	30	.5	2	200	
2N480	40-100	—	45	.5	2	200	
2N480A	40-100	—	45	.5	2	200	
2N541	80-200	—	15	.5	2	200	
2N542	80-200	—	30	.5	2	200	
2N542A	80-200	—	30	.5	2	200	
2N543	80-200	—	45	.5	2	200	
2N543A	80-200	—	45	.5	2	200	
2N1248	—	15 min (14)	6	0.01 (15)	2	30	
2N1276	9-22	10 (11)	40	1.0	2	150	
2N1277	18-44	20 (11)	40	1.0	2	150	

continued next page

Type	h_{fe}	h_{FE}	BV_{CBO}	I_{CBO}	C_{OB}	P_T	Comments
		TYPICAL	MINIMUM	MAXIMUM	TYPICAL	MAXIMUM	
	V_{CB}=5v I_E=1 ma f=1kc	V_{CE}=5v I_C=1 ma	I_{CBO}= 50 μa I_E=0	V_{CB}=30v I_E=0 T_A=25°C	V_{CB}=20v I_E=−1 ma f=1 mc.	Power Diss.	
			volts	μa	pf	mw	
2N1278	37-90	33(11)	40	1.0	2	150	Audio Amplifiers Astable Oscillators Chopper Circuits Flip-flop Circuits Logic Circuits RF Amplifiers
2N1279	76-333	80(11)	40	1.0	2	150	
2N1417	30-200	—	15	1.0(14)	2	150	
2N1418	30-200	—	30	10	2	150	
4C28	9-19	15	40(4)	2.0	4	150	Audio amplifiers Low cost industrial switches
4C29	18-40	30	40(4)	2.0	4	150	
4C30	37-80	55	40(4)	2.0	4	150	
4C31	76-300	115	40(4)	2.0	4	150	
4D20	See h_{FE}	15-50(10)	40(4)	1.0(8)	2	150	
4D21	See h_{FE}	40-135(10)	40(4)	1.0(8)	2	150	
4D22	See h_{FE}	120-250(10)	40(4)	1.0(8)	2	150	
4D24	See h_{FE}	15-50(10)	15(5)	1.0(7)	2	125	
4D25	See h_{FE}	40-135(10)	15(5)	1.0(7)	2	125	
4D26	See h_{FE}	120-250(10)	15(5)	1.0(7)	2	125	
(See Outline Drawing No. 4)							
2N2673	9-22	8-22	60	0.1	3	250	Audio Amplifiers Astable Oscillators Chopper Circuits, Logic Circuits Flip-flop Circuits, RF Amplifiers
2N2674	18-44	12-40	60	0.1	3	250	
2N2675	37-90	22-76	60	0.1	3	250	

Type	h_{fe}	h_{FE}	BV_{CBO}	I_{CBO}	C_{OB}	P_T	Comments
2N2676	76-333	45-290	60	0.1	3	250	Audio Amplifiers Astable Oscillators Chopper Circuits, Logic Circuits Flip-flop Circuits, RF Amplifiers
2N2677	19-120(9)	20-55(11)	45	0.1	2	250	
2N2678	39-250(9)	45-150(11)	45	0.1	2	250	

NOTES:
(1) Typical h_{fe} @ V_{CB} = 20 V, I_E = 1 ma.
(4) I_{CBO} = 100 μa, I_E = 0.
(5) BV_{CEO} @ I_{CEO} = 100 μa.
(6) V_{CB} = 20 V, I_E = 0
(7) V_{CB} = 15 V, I_E = 0
(8) V_{CB} = 12 V, I_E = 0
(9) V_{CB} = 20 V, I_E = 1 ma.
(10) Pulsed measurement.
(11) V_{CE} = 5V, I_C = 10 ma.
(12) V_{CE} = 10 V, I_C = 5 ma.
(13) Also available in military types.
(14) V_{CE} = 3V, I_C = .02 ma.
(15) V_{CB} = 3V, I_E = 0, T_A = 25°C.

POWER — NPN Passivated Mesa(5)

Type	Dwg. No.	h_{FE}(9)	V_{CEO}	V_{EBO}	I_{CBO}	Power P_T	Dissipation P_T	$V_{CE\,(SAT)}$(9)	Comments
			MINIMUM		MAXIMUM				
		V_{CE}=10v I_C=200 ma	I_C=250μa	I_E=250μa	V_{CB}=30v T_J=150°C	Free Air @25°C	Case Temp @25°C	I_C=200 ma I_B=40 ma	
			Volts	Volts	μa	Watts	Watts	Volts	
2N497(6)	5	12-36	60	8	250	0.8	4	5	Audio Amplifiers Blocking Oscillators DC to AC Inverters Linear Amplifiers Magnetic Tape Bias and Erase Oscillators Power Oscillators Power Switching Pulse Amplifiers Regulated Power Supplies Servo Amplifiers Servo Drivers Solenoid Drivers High Voltage Series Regulator
2N497A	5	12-36	60	8	250	1.0	5	2	
2N498(6)	5	12-36	100	8	250	0.8	4	5	
2N498A	5	12-36	100	8	250	1.0	5	2	
2N656(6)	5	30-90	60	8	250	0.8	4	5	
2N656A	5	30-90	60	8	250	1.0	5	2	
2N657(6)	5	30-90	100	8	250	0.8	4	5	
2N657A	5	30-90	100	8	250	1.0	5	2	
2N2017	5	50-200	60	8	250	1.0	5	2	
2N2106	5	12-36	60(1)	8	200(2)	1.0	5	5	
2N2107	5	30-90	60(1)	8	200(2)	1.0	5	2	
2N2108	5	75-200	60(1)	8	200(2)	1.0	5	2(3)	
2N2726	5	30-90	200(12)	10	100	1.0	5	2	
2N2727	5	75-150	200(12)	10	100	1.0	5	2	

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Type	Dwg. No.	h_{FE}[9] V_{CE}=10v I_C=200 ma	MINIMUM V_{CEO} I_C=250μa Volts	MINIMUM V_{EBO} I_E=250μa Volts	MAXIMUM I_{CBO} V_{CB}=30v T_J=150°C μa	MAXIMUM Power P_T Free Air @25°C Watts	MAXIMUM Dissipation P_T Case Temp @25°C Watts	MAXIMUM V_{CE} (SAT)[9] I_C=200 ma I_B=40 ma Volts	Comments
7A30	5	12-36	40	8	10[7]	1.0	5	1.0 Typ.	(Same applications as on previous page)
7A31	5	30-90	30	8	10[7]	1.0	5	1.0 Typ.	
7A32	5	75-200	30	8	10[7]	1.0	5	1.0 Typ.	
7A35	5	50-200	40[1]	15[13]	10[7]	1.0	5	2[3]	
2N1047	6	12-36	80	6	15[7]	1.0	40	7.5[8]	(Same applications as above but at higher power conditions)
2N1047A	6	12-36	80	6	350	1.0	40	7.5[8]	
2N1047B	6	12-36	80	6	200	1.0	40	2.0[8]	
2N1048	6	12-36	120	6	15[7]	1.0	40	7.5[8]	
2N1048A	6	12-36	120	6	350	1.0	40	7.5[8]	
2N1048B	6	12-36	120	6	200	1.0	40	2.0[8]	
2N1049	6	30-90	80	6	15[7]	1.0	40	7.5[8]	
2N1049A	6	30-90	80	6	350	1.0	40	7.5[8]	
2N1049B	6	30-90	80	6	200	1.0	40	2.0[8]	
2N1050	6	30-90	120	6	15[7]	1.0	40	7.5[8]	
2N1050A	6	30-90	120	6	350	1.0	40	7.5[8]	
2N1050B	6	30-90	120	6	200	1.0	40	2.0[8]	
2N1067	7	15-75	60	12[15]	1000[11]	—	5.0	—	
2N1068	7	15-75[10]	60	12[15]	1000[11]	—	10	—	
				V_{CEX} I_C=250 ma V_{BE}=−1.5v T_J=150°C			Case Temp.[4] @100°C		
2N2196	8	30-90	60[1]	80	250	2.0	10	2	
2N2197	8	75-200	60[1]	80	250	2.0	10	2[3]	
2N2201	8	30-90	100	120	200	2.0	10	1.7	
2N2202	12	30-90	100	120	200	1.0	10	1.7	
2N2203	13	30-90	100	120	200	1.0	10	1.7	
2N2204	14	30-90	100	120	200	1.0	10	1.7	
2N2239	8	30-200	50[16]	8[17]	250	1.0	10	3	(Same applications as above but at higher power conditions)
2N2995	13	30-90	100	120	200	1.5	10	1.7	
7B1	8	12-36	60	80	200	2.0	10	1.7	
7B2	8	30-90	60	80	200	2.0	10	1.7	
2N2611	8	12-36	100	120	200	2.0	10	1.7	
7B13	8	75-200	60		250	2.0	10	2	
7B33	8	30-90	200[12]	100[14]	200	2.0	10	2	
7B34	8	75-150	200[12]	100[14]	200	2.0	10	2	
7C1	9	12-36	60	80	200	1.0	10	1.7	
7C2	9	30-90	60	80	200	1.0	10	1.7	
7C3	9	12-36	100	120	200	1.0	10	1.7	
7C13	9	75-200	60		250	1.0	10	2	
7D1	10	12-36	60	80	200	1.0	10	1.7	
7D2	10	30-90	60	80	200	1.0	10	1.7	
7D3	10	12-36	100	120	200	1.0	10	1.7	
7D13	10	75-200	60		250	1.0	10	2	
7D33	10	30-90	200[12]	100[14]	200	1.0	10	2	
7D34	10	75-150	200[12]	100[14]	200	1.0	10	2	
7E1	11	12-36	60	80	200	1.0	10	1.7	
7E2	11	30-90	60	80	200	1.0	10	1.7	
7E3	11	12-36	100	120	200	1.0	10	1.7	
7E13	11	75-200	60		250	1.0	10	2	
7F1	12	12-36	60	80	200	1.0	4.0	1.7	
7F2	12	30-90	60	80	200	1.0	4.0	1.7	
7F3	12	12-36	100	120	200	1.0	4.0	1.7	
7F4	12	30-90	100	120	200	1.0	4.0	1.7	
7F13	12	75-200	60	—	250	1.0	4.0	2	
7G1	13	12-36	60	80	200	1.5	10	1.7	
7G2	13	30-90	60	80	200	1.5	10	1.7	
7G3	13	12-36	100	120	200	1.5	10	1.7	
7G13	13	75-200	60	—	250	1.5	10	2	
7G33	13	30-90	200[12]	100[14]	200	1.5	10	2	

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Type	Dwg. No.	h_{FE}(9) V_{CE}=10v I_C=200 ma	MINIMUM V_{CEO} I_C=250μa Volts	V_{EBO} I_E=250μa Volts	I_{CBO} V_{CB}=30v T_J=150°C μa	MAXIMUM Power P_T Free Air @25°C Watts	Dissipation P_T Case Temp @25°C Watts	V_{CE} (SAT)(9) I_C=200 ma I_B=40 ma Volts	Comments
7G34	13	75-150	200(12)	100(14)	200	1.5	10	2	

NOTES: (1) V_{CER} (I_C=16 ma, R=1KΩ) (2) T_J=125°C (3) I_B=10 ma (4) See outline drawing for attachment to heatsink. (5) Typ. f_t for all types≈15 MC (6) Available as JAN types (MIL-S-19500/74A) (7) T_J=25°C (8) I_C=500 ma, I_B=100 ma (9) Pulsed Measurement: 300 μsec. pulse width, 2% duty cycle. (10) V_{CE}=4V, I_C=750 ma (11) T_J=175°C (12) V_{CER} (I_C=50 ma, R=5KΩ) (13) I_E=1 μa (14) I_C=100 μa (15) I_E=100 μa (16) V_{CER} (I_C=250μa, R=5KΩ) (17) V_{EBO} (I_E=250μa)

Triple-Diffused NPN Passivated

Type	Dwg. No.	h_{FE} V_{CE}=15v I_C=2 amp.	h_{FE} V_{CE}=5v I_C=500 ma	MINIMUM V_{CEO} Volts	I_{CES} @150°C ma	MAXIMUM I_C Amps	Power P_T Free Air @25°C Watts	Dissipation P_T Case Temp @100°C Watts	V_{CE} (SAT) I_C=2 amps I_B=250 ma Volts	V_{CE} (SAT) I_C=1 amp I_B=100 ma Volts
2N1616	14	15 min.	—	60	10@60(1)	5	3	60	—	—
2N1617	14	15-75	—	80	10@80(1)	5	3	60	—	—
2N1618	14	15-75	—	100	10@80(1)	5	3	60	2	—
2N1724	14	20-90	—	80	2@60V	5	3	50	1	—
2N1724A	14	50-150	—	120	2@100V	5	3	50	6	—
2N1725	14	30-90	—	80	2@60V	5	3	50	1	—
2N2150	15	—	20-60	80	.1@120V	2	2	30	—	1.25
2N2151	15	—	40-120	80	.1@120V	2	2	30	—	1.25
2N3220	15	—	20-60	80	.1@100	2	2	30	—	1.25
2N3221	15	—	40-120	80	.1@100	2	2	30	—	1.25
2N3222	15	—	20-60	60	.1@80	2	2	30	—	1.25
2N3223	15	—	40-120	60	.1@80	2	2	30	—	1.25

NOTES: (1) I_{CBO}.

AMPLIFIERS NPN Planar, Typical $f_t \cong$ 130 mc
(See Outline Drawing No. 5)

Type(2)	h_{FE} I_C=150 ma V_{CE}=10v	Min. V_{CER} R_{BE}≦10Ω I_C=100 ma Volts	Max. V_{CE} (SAT) I_C=150 ma I_B=15 ma Volts	V_{BE} (SAT) I_C=150 ma I_B=15 ma Volts	h_{fe} f=1 kc I_C=1 ma V_{CE}=5v Min. Max.	MAXIMUM I_{CBO} T_J=150°C V_{CB} Volts	μa	V_{EBO} I_E=100 μa Volts	POWER DISS. P_T Free Air @25°C Watts	P_T Case Temp. @100°C Watts	MINIMUM h_{FE} I_C=10 ma V_{CE}=10v	I_C=10 ma V_{CE}=10v T_J=−55°C	I_C=0.1 ma V_{CE}=10v	I_C=500 ma V_{CE}=10v	I_C=1000 ma V_{CE}=10v	Comments
2N1889	40-120	80	5.0	1.3	30-100	75	15	7	0.8	1.7	35	20	20	—	—	High Voltage 2N1613.
2N1890	100-300	80	5.0	1.3	50-200	—	—	7	0.8	1.7	—	—	—	—	—	Higher voltage 2N1711.
2N1972	—	30	2(7)	1.1(7)	40	30	100	5	0.6	1.0	70	40	—	—	—	
2N1973	75 Min.(6)	80	1.2(7)	0.9(7)	76-200	75	15	7	0.8	1.7	—	—	—	—	—	
2N1974	35 Min.(6)	80	1.2(7)	0.9(7)	36-90	75	15	7	0.8	1.7	—	—	—	—	—	
2N1975	15 Min.(6)	80	1.2(7)	0.9(7)	18-50	75	15	7	0.8	1.7	—	—	—	—	—	
2N1983	—	30	0.25(5)	—	70-210	30	200	5	0.6	1.0	—	—	—	—	—	High beta for high gain, low noise amplifiers. (Industrial Types)
2N1984	—	30	0.25(5)	—	35-100	30	200	5	0.6	1.0	—	—	—	—	—	Amplifier Circuits. (Industrial Types)
2N1985	—	30	0.25(5)	—	15-45	30	200	5	0.6	1.0	—	—	—	—	—	Amplifier Circuits. (Industrial Types)
2N2049	—	50	0.4(4)	0.8(4)	75	60	10	7	0.8	1.7	—	—	60	—	—	High beta for high gain, low noise amplifiers NF=3db.
(See Outline Drawing No. 16)																
2N870	40-120	80	5.0	1.3	30-100	75	15	7	.5	1.0	35	20	20	—	—	TO-18 Version of 2N1889.
2N871	100-300	80	5.0	1.3	50-200	—	—	7	.4	.75	—	—	—	—	—	TO-18 Version of 2N1890.
2N910	75 Min.(6)	80	1.2(7)	0.9(7)	76-200	75	15	7	.4	.75	—	—	—	—	—	TO-18 Version of 2N1973.
2N911	35 Min.(6)	80	1.2(7)	0.9(7)	36-90	75	15	7	.4	.75	—	—	—	—	—	TO-18 Version of 2N1974.
2N912	15 Min.(6)	80	1.2(7)	0.9(7)	18-50	75	15	7	.4	.75	—	—	—	—	—	TO-18 Version of 2N1975.

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Typical $f_t \cong$ 130 mc (See Outline Drawing No. 16)

Type	h_{FE} Min.–Max.	@I_C ma	@V_{CE} Volts	MINIMUM h_{fe} V_{CE}=10v I_C=4 ma f=100 mc	MINIMUM V_{CEO} Volts	@I_C ma	MINIMUM V_{EBO} Volts	@I_E μa	MAXIMUM V_{BE} (SAT) I_C=10 ma I_B=1 ma Volts	MAXIMUM V_{CE} (SAT) I_C=10 ma I_B=1 ma Volts	MAXIMUM I_{CBO} T_J=150°C na	@V_{CB} Volts	MAXIMUM V_{BE} (SAT) I_C=3 ma I_b=1.5	MAXIMUM V_{CE} (SAT) I_C=3 ma I_b=1.5	C_{ob} pf	@V_{CB} Volts	Comments
2N929	40-120	.01	5.0	—	45	10	5	100	0.6-1(2)	1.0(2)	10	45	—	—	5(TYP)		These devices are intended for applications requiring high gain at low current.
2N930	100-300	.01	5.0	—	45	10	5	100	0.6-1(2)	1.0(2)	10	45	—	—	5(TYP)		
2N2483	40-120	.01	5.0	—	60	10	6	10	—	.35(3)	10	45	—	—	5(TYP)		
2N2484	100-500	.01	5.0	—	60	10	6	10	—	.35(3)	10	45	—	—	5(TYP)		

Typical $f_t \cong$ 130 mc (See Outline Drawing No. 16)

Type	h_{FE} Min.–Max.	@I_C ma	@V_{CE} Volts	MINIMUM h_{fe} V_{CE}=10v I_C=4 ma f=100 mc	MINIMUM V_{CEO} Volts	@I_C ma	MINIMUM V_{EBO} Volts	@I_E μa	MAXIMUM V_{BE} (SAT) I_C=10 ma I_B=1 ma Volts	MAXIMUM V_{CE} (SAT) I_C=10 ma I_B=1 ma Volts	MAXIMUM I_{CBO} T_J=150°C na	@V_{CB} Volts	MAXIMUM V_{BE} (SAT) I_C=3 ma I_b=1.5	MAXIMUM V_{CE} (SAT) I_C=3 ma I_b=1.5	C_{ob} pf	@V_{CB} Volts	Comments
2N759	36-90	1.0	5.0	—	45	1.0	8	100	—	1.0	200	30	—	—	8	5	These devices are well suited for applications where the 2N335 and 2N336 have been used and higher frequency devices or smaller packages are required.
2N760	76-333	1.0	5.0	—	45	1.0	8	100	—	1.0	200	30	—	—	8	5	
2N915	40-160	10	5.0	—	50	10	5	100	0.9	1.0	30	60	—	—	3.5	10	These devices are intended for non-saturating switching circuits, amplifier and oscillator circuits.
2N916	50-200	10	1.0	—	25	30	5	10	0.9	0.5	10	15	—	—	6	5	

NPN Planar Epitaxial Typical $f_t \cong$ 900 mc (See Outline Drawing No. 17)

Type	h_{FE} Min.–Max.	@I_C ma	@V_{CE} Volts	MINIMUM h_{fe} V_{CE}=10v I_C=4 ma f=100 mc	MINIMUM V_{CEO} Volts	@I_C ma	MINIMUM V_{EBO} Volts	@I_E μa	MAXIMUM V_{BE} (SAT) I_C=10 ma I_B=1 ma Volts	MAXIMUM V_{CE} (SAT) I_C=10 ma I_B=1 ma Volts	MAXIMUM I_{CBO} T_J=150°C na	@V_{CB} Volts	MAXIMUM V_{BE} (SAT) I_C=3 ma I_b=1.5	MAXIMUM V_{CE} (SAT) I_C=3 ma I_b=1.5	C_{ob} pf	@V_{CB} Volts	Comments
2N917	20	3	1	5	15	3	3	10	—	—	1	15	.87	.5	1.7	10	These devices are intended for use in ultra-high frequency amplifiers and oscillators, and in non-saturated switching.
2N918	20	3	1	6	15	3	3	10	—	—	10	15	1.0	.4	1.7	10	

Kovar Tab (See Outline Drawing No. 18)

Type	h_{FE} Min.–Max.	@I_C ma	@V_{CE} Volts	h_{fe}	V_{CEO} Volts	@I_C ma	V_{EBO} Volts	@I_E μa	V_{BE} (SAT)	V_{CE} (SAT)	I_{CBO} na	@V_{CB} Volts	V_{BE} (SAT)	V_{CE} (SAT)	C_{ob} pf	@V_{CB} Volts	Comments
10C573	—			—	45	1.0	6	100	—	—	15	30	—	—	8	10	Kovar tab version of 2N759.
10C574	—			—	45	1.0	6	100	—	—	15	30	—	—	8	10	Kovar tab version of 2N760.

NOTES: (1) h_{fe} (2) I_B=0.5 ma. (3) I_B=0.1 ma. (4) I_C=10 ma. and I_B=1 ma. (5) I_C=5 ma and I_B=0.5 ma. (6) h_{FE}=I_C=10 ma, V_{CE}=10V. (7) I_C=50 ma, I_B=5 ma.

SWITCHES AND AMPLIFIERS[1,3]— NPN Planar Epitaxial

Available in Seven Different Package Configurations: Three Power Packages, TO-5, TO-46, TO-50, and Kovar Tab

Type	Dwg. No.	h_{FE} I_C=150 ma V_{CE}=10v	Min. V_{CER} R_{BE}=10Ω I_C=100 ma Volts	MAXIMUM V_{CE} (SAT) I_B=15 ma I_C=150 ma Volts	MAXIMUM V_{BE} (SAT) I_C=150 ma I_B=15 ma Volts	Max. I_{CBO} T_J=150°C V_{CB} Volts	Max. I_{CBO} T_J=150°C μa	V_{EBO} I_E=100 μa Volts	POWER DISS. P_T Free Air @25°C Watts	POWER DISS. P_T Case Temp @25°C Watts	MINIMUM h_{FE} I_C=10 ma V_{CE}=10v	MINIMUM h_{FE} I_C=10 ma V_{CE}=10v T_J=−55°C	MINIMUM h_{FE} I_C=0.1 ma V_{CE}=10v	MINIMUM h_{FE} I_C=500 ma V_{CE}=10v	MINIMUM h_{FE} I_C=1000 ma V_{CE}=10v	Comments
2N2192 2N2350 11C702	5 4 19	100-300	40[2]	0.35	1.3	30	15	5	0.8 0.4 0.3	2.8 5.0 1.0	75	35	15	35	15	Similar to 2N1711, but lower $V_{CE(SAT)}$.
2N2192A 2N2350A 11C1B1 11C1F1 11C201B20	5 4 8 12 20	100-300	40[2]	0.25	1.3	30	15	5	0.8 0.4 1.5 1.15 1.0	2.8 5.0 5.0 3.1 5.0	75	35	15	35	15	Similar to 2N1711, but lower $V_{CE(SAT)}$.
2N2193 2N2351 11C704	5 4 19	40-120	50[2]	0.35	1.3	60	25	8	0.8 0.4 0.3	2.8 5.0 1.0	30	20	15	20	15	Similar to 2N1613, but lower $V_{CE(SAT)}$.
2N2193A 2N2351A 11C3B1 11C3F1 11C203B20	5 4 8 12 20	40-120	50[2]	0.25	1.3	60	25	8	0.8 0.4 1.5 1.15 1.0	2.8 5.0 5.0 3.1 5.0	30	20	15	20	15	Similar to 2N1613, but lower $V_{CE(SAT)}$.
2N2194 2N2352	5 4	20-60	40[2]	0.35	1.3	30	25	5	0.8 0.4	2.8 5.0	15	—	—	12	—	Similar to 2N696, but lower $V_{CE(SAT)}$.
2N2194A 2N2352A 11C5B1 11C5F1 11C205B20	5 4 8 12 20	20-60	40[2]	0.25	1.3	30	25	5	0.8 0.4 1.5 1.15 1.0	2.8 5.0 5.0 3.1 5.0	15	—	—	12	—	Similar to 2N696, but lower $V_{CE(SAT)}$.
2N2195 2N2353	5 4	20 min.	25[2]	0.35	1.3	30	50	5	0.6 .35	2.8 3.0	—	—	—	—	—	Industrial Types.
2N2195A 2N2353A 11C7B1 11C7F1 11C207B20	5 4 8 12 20	20 min.	25[2]	0.25	1.3	30	50	5	0.6 .35 1.5 1.15	2.8 3.0 5.0 3.1	—	—	—	—	—	Industrial Types.
2N2243 2N2364	5 4	40-120	80	.35	1.3	60	15	7	.8 .4	2.8 5.0	30	20	15	20	—	Similar to 2N1893 but lower $V_{CE(SAT)}$.
2N2243A 2N2364A 11C710 11C10B1 11C10F1 11C210B20	5 4 19 8 12 20	40-120	80	.25	1.3	60	15	7	.8 .4 .3 1.5 1.15 1.0	2.8 5.0 1.0 5.0 3.1 5.0	30	20	15	20	—	Similar to 2N1893 but lower $V_{CE(SAT)}$.
2N2868 2N2909 11C11B1 11C11F1 11C211B20	5 4 8 12 20	40-120	40	.25	1.3	30	15	5	.8 .4 1.5 1.15 1.0	2.8 5.0 5.0 3.1 5.0	30	20	—	20	—	—
11C1536	3	40-120	30[2]	.3	1.3	30	25	6	0.8	2.8	—	—	—	15	—	—
4JD12X043 4JD12X047	21 21	Two 2N2193 transistors in a six lead TO-5 package. Two 2N2195 transistors in a six lead TO-5 package.														

Kovar Tab (See Outline Drawing No. 18)

Type	Dwg. No.	h_{FE}	V_{CER}	V_{CE} (SAT)	V_{BE} (SAT)	V_{CB}	I_{CBO}	V_{EBO}	P_T Free Air	P_T Case	I_C=10 ma	I_C=10 ma T_J=−55°C	I_C=0.1 ma	I_C=500 ma	I_C=1000 ma	Comments
11C551[6]		100-300[4]	—	0.25[5]	0.9[5]	30	15	5	100mw	—	100-300	—	75	—	—	Kovar Tab of 2N2192, A
11C553[6]		40-120[4]	—	0.25[5]	0.9[5]	30	15	7	100mw	—	40-120	—	30	—	—	Kovar Tab of 2N2193, A
11C557[6]		30-150[4]	—	0.25[5]	0.9[5]	30	50	5	100mw	—	30-150	—	—	—	—	Kovar Tab of 2N2195, A

NOTES: Test Conditions in Italics

(1) Typical f_t for all types ≈ 130 Mc.
(2) V_{CEO}
(3) For switching and amplifier applications.
(4) $h_{FE} = I_C = 10$ ma, $V_{CE} = 10V$.
(5) $I_C = 50$ ma, $I_B = 5$ ma.
(6) Storage Temperature on all types is −65°C to +300°C. Operating Temperature on all types is −65°C to +200°C.

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NPN Planar Passivated[1,3] (See Outline Drawing No. 5)

Type[2]	hFE Ic=150 ma VCE=10v	Min. VCER RBE≦10Ω Ic=100 ma Volts	Max. VCE (SAT) Ic=150 ma IB=15 ma Volts	Max. VBE (SAT) Ic=150 ma IB=15 ma Volts	hfe f=1 kc Ic=1 ma VCE=5v Min. Max.	MAXIMUM ICBO TJ=150°C VCB Volts	MAXIMUM ICBO TJ=150°C μa	VEBO IE=100 μa Volts	POWER DISS. PT Free Air @25°C Watts	POWER DISS. PT Case Temp. @100°C Watts	MINIMUM hFE Ic=10 ma VCE=10v	MINIMUM hFE Ic=10 ma VCE=10v TJ=−55°C	MINIMUM hFE Ic=0.1 ma VCE=10v	MINIMUM hFE Ic=500 ma VCE=10v	MINIMUM hFE Ic=1000 ma VCE=10v	Comments
2N696[4]	20-60	40	1.5	1.3	—	*30*	100	5	0.6	1.0	—	—	—	—	—	
2N697[4]	40-120	40	1.5	1.3	—	*30*	100	5	0.6	1.0	—	—	—	—	—	
2N698	20-60	80	5.0	1.3	15	*75*	15	7	0.8	1.7	—	—	—	—	—	High Voltage 2N696.
2N699	40-120	80	5.0	1.3	35-100	*60*	200	5	0.6	1.0	—	—	—	—	—	High Voltage 2N697.
2N1613	40-120	50	1.5	1.3	30-100	*60*	10	7	0.8	1.7	35	20	20	20	—	Lower leakage 2N697.
2N1711	100-300	50	1.5	1.3	50-200	*60*	10	7	0.8	1.7	75	35	35	40	—	High beta 2N1613.
2N1837	40-120	50	.8	1.3	—	*30*	50	8	0.6	1.0	—	—	—	—	—	
2N1893	40-120	100	5.0	1.3	30-100	*90*	15	7	0.8	1.7	35	20	20	—	—	High voltage 2N1613.
(See Outline Drawing No. 16)																
2N717	20-60	40	1.5	1.3	—	*30*	100	5	.4	.75	—	—	—	—	—	TO-18 Version of 2N696.
2N718	40-120	40	1.5	1.3	—	*30*	100	5	.4	.75	—	—	—	—	—	TO-18 Version of 2N697.
2N718A	40-120	50	1.5	1.3	30-100	*60*	10	7	0.8	1.7	—	—	—	—	—	TO-18 Version of 2N1613.
2N719	40-120	80	5.0	1.3	35-100	*60*	200	5	.5	1.0	—	—	—	—	—	TO-18 Version of 2N698.
2N719A	20-60	80	5.0	1.3	15	*75*	15	7	.4	.75	—	—	—	—	—	TO-18 Version of 2N698.
2N720	40-120	80	5.0	1.3	35-100	*60*	200	5	.5	1.0	—	—	—	—	—	TO-18 Version of 2N699.
2N720A	40-120	100	5.0	1.3	30-100	*90*	15	7	.4	.75	35	20	20	—	—	TO-18 Version of 2N1893.
2N956	100-300	50	1.5	1.3	50-200	*60*	10	7	.5	1.0	75	35	35	40	—	TO-18 Version of 2N1711.

Kovar Tab (See Outline Drawing No. 18)

Type	hFE	VCER	VCE (SAT)	VBE (SAT)	hfe	VCB	μa	VEBO	PT Free Air	PT Case	hFE	hFE	hFE	hFE	hFE	Comments
11B551	20-60[5]	—	0.7[6]	0.9[6]	—	*30*	25	5	100mw	—	—	—	—	—	—	Kovar tab of 2N696.
11B552	40-120[5]	—	0.7[6]	0.9[6]	—	*30*	25	5	100mw	—	—	—	—	—	—	Kovar tab of 2N697.
11B554	40-120[5]	—	0.7[6]	0.9[6]	—	*40*	15	7	100mw	—	—	—	—	—	—	Kovar tab of 2N1613.
11B555	100-300[5]	—	0.7[6]	0.9[6]	—	*40*	15	7	100mw	—	—	—	—	—	—	Kovar tab of 2N1711.
11B556	40-120[5]	—	1.3[6]	0.9[6]	—	*40*	15	7	100mw	—	—	—	—	—	—	Kovar tag of 2N1893.
11B560	40-120[5]	—	1.3[6]	0.9[6]	—	*30*	25	5	100mw	—	—	—	—	—	—	Kovar tab of 2N699.

NOTES: Test Conditions in Italics.

(1) Typical f_t for all types ≈ 130 Mc.
(2) Storage temperature on all types is −65° to +300°C. Operating junction temperature on all types is −65° to +200°C.
(3) For switching and amplifier applications.
(4) Also available in military types. (5) h_{FE} = I_C = 10 ma, V_{CE} = 10V. (6) I_C = 50 ma, I_B = 5 ma.

HIGH SPEED SWITCHES[1,3]— NPN Planar Epitaxial (See Outline Drawing No. 16)

Type	hFE Min. Max.	@Ic ma	@VCE Volts	MINIMUM VCER Volts	@Ic ma	@RBE ohms	MINIMUM VCEO Volts	@Ic ma	MINIMUM VEBO Volts	@IE μa	MAXIMUM VBE (SAT) Ic=10 ma IB=1 ma Volts	MAXIMUM VCE (SAT) Ic=10 ma IB=1 ma Volts	MAXIMUM ICBO TJ=150°C @VCB Volts	MAXIMUM ICBO μa	MAXIMUM ton nsec	MAXIMUM toff nsec	MAXIMUM Cob pf	@VCB Volts	Comments
2N706	20 Min.	*10*	*1.0*	20	*30*	*10*	—		3	*100*	0.9	0.6	*15*	30	—	—	6	10	Economy Units.
2N706A	20-60	*10*	*1.0*	20	*10*	*10*	15	*10*	5	*10*	0.9	0.6	*15*	30	40	75	5	5	Economy units. High speed.
2N708	30-120	*10*	*1.0*	20	*30*	*10*	15	*30*	5	*10*	0.8	0.4	*20*	15	40	70	6	10	Low leakage current. High speed.
2N709	20-120	*10*	*0.5*	—	—	—	6	*10*	4	*10*	0.85[6]	0.3[6]	*5*	5[7]	15	15	3	5	Very high speed switch.
2N753	40-120	*10*	*1.0*	20	*10*	*10*	15	*10*	5	*10*	0.9	0.6	*15*	30	40	75	5	5	High beta. High speed.

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Type	hFE Min. @Ic (ma)	hFE Max. @VCE (Volts)	VCER Volts @Ic (ma)	VCER Volts @RBE (ohms)	MINIMUM VCEO Volts @Ic (ma)	VEBO Volts @IE (μa)	MAXIMUM VBE (SAT) Ic=10 ma IB=1 ma Volts	VCE (SAT) Ic=10 ma IB=1 ma Volts	ICBO TJ=150°C @VCB Volts μa	ton nsec	toff nsec	Cob pf	@ VCB Volts	Comments
2N834	*10* 25 Min.	*1.0*	*10μa* 30(1)	*0*	— —	*100* 5	0.9	0.25	*20* 30	35	75	4	10	Low saturation voltage.
2N914	*10* 30-120	*1.0*	*30* 20	*10*	*30* 15	*10* 5	0.8	0.25	*20* 15	40	40	6	10	High speed. Low saturation voltage.
2N2369	*10* 40-120	*1.0*	— —	—	*10* 15	*10* 4.5	0.85	0.25	*20* 30	12	18	4	5	High speed switching.
2N2481	*10* 40-120	*1.0*	*1μa* 30(2)	*0*	*30* 15	*100* 5	0.82	0.25	*20* 15	40	45	5	5	U.S. Navy Specification.

Kovar Tab (See Outline Drawing No. 18)

Type	hFE Min. @Ic (ma)	hFE Max. @VCE (Volts)	VCER Volts @Ic (ma)	VCER Volts @RBE (ohms)	VCEO Volts @Ic (ma)	VEBO Volts @IE (μa)	VBE (SAT) Volts	VCE (SAT) Volts	ICBO Volts μa	ton nsec	toff nsec	Cob pf	@ VCB Volts	Comments
10B551	*10* 30-120	*1.0*	*10* 20	*10*	*10* 15	*100* 5	0.85	0.25	*15* 25	45	50	6	10	Kovar tab version of 2N914.
10B553	*10* 30-120	*1.0*	*10* 20	*10*	*10* 15	*100* 5	0.85	0.4	*15* 25	40	70	—	—	Kovar tab version of 2N706.
10B555	*10* 20 Min.	*1.0*	*10* 20	*10*	*10* 15	*100* 3	0.9	0.6	*15* 30	—	—	—	—	Kovar tab version of 2N706A.
10B556	*10* 20-60	*1.0*	*10* 20	*10*	*10* 15	*100* 3	0.9	0.6	*15* 30	40	75	—	—	Kovar tab version of 2N708.

NOTES: Test Conditions in Italics.
(1) Typical f_t for all types ≈ 130 Mc.
(2) Storage temperature on all types is −65° to +300°C. Operating junction temperature on all types is −65° to +200°C.
(3) For switching and amplifier applications. (4) Storage temperature −55° C to +200° C. Operating temperature −55° C to + 125°C.
(5) T_J = 125°C. (6) I_C = 3 ma, I_B = .15 ma.

GERMANIUM TRANSISTORS

NPN RATE GROWN (See Outline Drawing No. 22)

Type	hFE VCE=1 v Ic=1 ma	MINIMUM BVCEO Ic=300 μa volts	MAXIMUM ICBO IE=0 VCB=15 v μa	Power Gain @ 455 kc db	MAXIMUM PT Power Dissipation mw	TYPICAL fhfb mc	Comments
2N78	45-135	15	3	26.0-31.0	65	9	Preamplifier switch. Lamp driver. Schmitt trigger. Waveform restoration. DC level detection.
2N78A(7)	45-135	20	3	26.0-31.0	65	9	Applications same as 2N78.
2N167A(7)	17-90(1)	30	1.5	—	75	9	Trigger circuits. Gate circuits. Logic circuits.
2N169	34-200	15(3)	5	23.5	65	9	Reflex circuits. IF amplifiers. DC coupled audio amplifiers.
2N169A	34-200	25(3)	5	23.5	65	9	General purpose low level switch(4).
2N292	8-51	15(3)	5	21.0-26.0	65	5	IF amplifiers.
2N293	8-51	15(3)	5	23.5-28.0	65	8	IF amplifiers.
2N1086	17-200	9(3)	3(5)	23.0-29.0(6)	65	9	Autodyne Converter. Mixer-oscillator.
2N1086A	17-200	9(3)	3(5)	23.0-27.0(6)	65	9	Autodyne Converter. Mixer-oscillator.
2N1087	17-200	9(3)	3(5)	25.0-29.0(6)	65	9	Autodyne Converter. Mixer-oscillator.
2N1694	15-45(2)	20	1.5	—	75	9	Decade counter. Low level switch. Amplifiers.

NOTES:
(1) I_C = 8 ma., V_{CE} = 1 V.
(2) I_C = 2 ma., V_{CE} = 1 V.
(3) BV_{CER}, R = 10K.
(4) Max $V_{CE(SAT)}$ = 0.4 V.
(5) V_{CB} = 5 V.
(6) Conversion Gain @ 1600 kc.
(7) Also available in military types.

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PNP ALLOY

Types	Dwg. No.	h_{FE} V_{CE}=1v I_C=20 ma	TYPICAL f_{hfb} mc	MINIMUM BV_{CER} @ I_C=600 μa R_{BE}=10K Volts	MAXIMUM I_{CBO} μa	MAXIMUM @ V_{CB} Volts	MAXIMUM P_T Power Dissipation mw	Comments
2N43A (10)	23	34-65	1.3	30	16	*45*	240	See 2N525. Not recommended for new designs.
2N44A (10)	23	18-43	1.0	30	16	*45*	240	See 2N524.
2N186A	23	19-31	0.8	25	16	*25*	200	See 2N508, 2N1175 and 2N1413 series.
2N187A	23	25-42	1.0	25	16	*25*	200	
2N188A	23	34-65	1.2	25	16	*25*	200	
2N189	23	25-42	0.8	25	16	*25*	200	
2N190	23	34-65	1.0	25	16	*25*	200	
2N191	23	53-121	1.2	25	16	*25*	200	
2N192	23	72-176	1.5	25	16	*25*	200	
2N241A	23	50-125	1.3	25	16	*25*	200	
2N319	24	25-42	2.0	20	16	*25*	225	Audio driver and audio output.
2N320	24	34-65	2.5	20	16	*25*	225	
2N321	24	53-121	3.0	20	16	*25*	225	
2N322	24	34-65	3.0	16	16	*16*	200	
2N323	24	53-121	3.5	16	16	*16*	200	
2N324	24	72-198	4.0	16	16	*16*	200	
2N394	24	20-150 (2)	7.0	15	6	*10*	150	Medium speed switch.
2N395	24	20-150 (2)	6.0	15	6	*15*	200	Medium speed switch.
2N396	24	30-150 (2)	8.0	20	6	*20*	200	Industrial/Military-medium beta, medium speed switch.
2N396A (10)	24	30-150 (2)	8.0	20 (5)	6	*20*	200	Same as 2N396. Mil-S-19500/64B.
2N397	24	40-150 (2)	12.0	15	6	*15*	200	Industrial/Military-medium speed switch.
2N404 (10)	24	—	8.0	24 (6)	5	*12*	150	Medium speed switch—wide beta spread. MIL-T-19500/20.
2N404A	24	—	8.0	35 (6)	5	*20*	150	Same as 2N404.
2N413	24	20-100 (2)	6.0	18 (5)	5	*12*	150	General purpose medium speed switch.
2N414	24	30-120 (2)	7.0	15 (5)	5	*12*	150	Same as 2N413.
2N461	24	32-199 (4)	4.0	35 (9)	15	*45*	200	General purpose.
2N508	24	100-200	4.5	16	7	*16*	200	High gain, low noise preamplifiers.
2N508A	24	100-200	4.5	25	7	*25*	200	
2N524	24	25-42	2.5	30	10	*30*	225	Military/industrial.—Audio amplifier and medium speed switch. Specified h_{FE} hold-up, high temperature I_{CO}, and low temperature h_{FE}. Guaranteed reliability index. MIL-T-19500/60B.
2N525	24	34-65	3.0	30	10	*30*	225	
2N526 (10)	24	53-90	3.5	30	10	*30*	225	
2N527	24	72-121	4.0	30	10	*30*	225	
2N1057	23	34-90	1.3	30 (7)	16	*45*	240	See 2N1924 series. Not recommended for new designs.
2N1097	24	34-90	3.0	16	16	*16*	200	Audio driver and audio output.
2N1098	24	25-90	3.0	16	16	*16*	200	
2N1144	23	34-90	1.3	16	16	*16*	175	See 2N1097, 2N1098, or 2N1413 series. Not recommended for new designs.
2N1145	23	25-90	1.3	16	16	*16*	175	
2N1175	24	70-140	4.0	25	12	*30*	200	General purpose industrial and consumer preamplifier.
2N1175A	24	70-140	4.0	25	12	*30*	200	General purpose industrial and consumer, high gain, low noise preamplifiers. Guaranteed noise figure.
2N1303 (10)	24	20 Min. (2)	7.0	25 (6)	6	*25*	150	Medium speed switch. MIL-S-19500/126A.
2N1305 (10)	24	40-200 (2)	8.0	20 (6)	6	*25*	150	
2N1307 (10)	24	60-300 (2)	12.0	15 (6)	6	*25*	150	
2N1413	24	25-42	3.2	25	12	*30*	200	General purpose industrial and consumer audio amplifier and medium speed switch.
2N1414	24	34-65	3.6	25	12	*30*	200	
2N1415	24	53-90	4.0	25	12	*30*	200	
2N1614	23	18-43	1.3	40 (8)	25	*65*	240	See 2N1924 series. Not recommended for new designs.
2N1924	24	34-65	3.0	40	10	*45*	225	Military/industrial audio amplifier and medium speed switch. High voltage, specified h_{FE} hold-up, low temperature h_{FE}, and high temperature I_{CO}. Guaranteed reliability index.
2N1925	24	53-90	3.5	40	10	*45*	225	
2N1926	24	72-121	4.0	40	10	*45*	225	

NOTES:

Test conditions in Italics.

(1) All specs. at 25°C unless noted otherwise.

(2) V_{CE} = 1V, I_C = 10 Ma.

(3) V_{CE} = .25V, I_B = 1 Ma.

(4) V_{CB} = 5V, I_E = 1 ma, f = 1 Kc,

(5) BV_{CEO}.

(6) V_{RT}.

(7) V_{RT} = 45V.

(8) V_{RT} = 60 V.

(9) R = 1 K.

(10) Also available as military types.

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HIGH FREQUENCY*— PNP Prolongated Exterior Base (PEB)

(See Outline Drawing No. 25)

Types[1,2]	MAXIMUM V_{CER}[3] Volts	V_{CBO} Volts	V_{EBO} Volts	P_C mw	MAXIMUM I_{CBO} μa AT	V_{CB} Volts	MIN. h_{FE}[4]	TYPICAL[4] f_T mc	f_{max} mc	G_P at f db	mc	NF at f R_{GEN}=50 ohm db	mc	Comments
154T1	−12	−12	−1	80	10	−10	30	140		45	455kc			Mixer-oscillator, IF amplifier in AM receivers.
155T1	−12	−12	−1	80	10	−10	30	150		35	10.7			Mixer-oscillator, IF amplifier (455KC and 10.7 mc).
156T1	−12	−12	−1	80	10	−10	15	150		13	100			Mixer-oscillator (100 mc) IF amplifier.
157T1	−12	−12	−1	80	10	−10	15	160		14	100			RF amplifier (100 mc).
159T1	−14	−14	−0.7	80	10	−12	15	330	800	34	44			IF amplifier (35-50 mc).
160T1	−14	−14	−0.7	80	10	−12	15	345	1000	25	100			RF amplifier, Mixer-oscillator
161T1	−14	−14	−0.7	80	10	−12	15	345	1000	19	150	6	200	RF amplifier, Mixer-oscillator.
162T1	−14	−14	−0.7	80	10	−12	15	360	1400	18	200	5	200	Low noise RF amplifier.
501T1	−20	−20	−1	80	10	−20	30	345	1000	27	100	4	100	G_P=16 db at f=200 mc.
503T1	−20	−20	−1	80	10	−20	15	345	1000	16	200	5	200	
504T1	−20	−20	−1	80	10	−20	100	300						Video frequency amplifier.
505T1	−20	−20	−1	80	10	−20	30	330	800	34	36			Large output impedance.
508T1	−20	−20	−1	80	10	−20	15	330	800	28	60			

*Made in France for General Electric by the Societe Europeenne des Semiconducteurs (SESCO).
(1) All specs at 25°C unless noted otherwise.
(2) Storage temperature on all types is −65 to +100°C. Operating junction temperature on all types is −65 to +85°C.
(3) $R_B < 100\ R_E$ for types 154T1 through 157T1. $R_B \leq 50\ R_E$ for all other types.
(4) V_{CE} = −6 volts, I_C = −1 ma for 154T1 through 157T1. For all other types V_{CE} = −9 volts, I_C = −2 ma.

SPECIAL SILICON PRODUCTS

REFERENCE AMPLIFIERS (See Outline Drawing No. 26)

Type	CIRCUIT CHARACTERISTICS K_T Max. Temperature Coefficient	Temperature Range	V_{ref} Reference Voltage	GMC Min. Trans-Conductance	TRANSISTOR CHARACTERISTICS h_{FE}	I_{CBO} Max. μa	BV_{CEO} Min. Volts	Zener Characteristics R_Z Max. Ohms
	TEST CONDITIONS				TEST CONDITIONS			
	V_{CB}=3v @ I_C=.5 ma @ R_B=1 K @ I_Z=0				V_{CE}=3v I_C=.5 ma	V_{CB}=30v	I_C=1 ma	I_Z=.5 ma
RA1 RA1A RA1B RA1C	.02%/°C .005%/°C .002%/°C .001%/°C	0°C to +70°C	7.0V ±10%	3000 μmho	10 Minimum 120 Maximum	1.0	45	200
RA2 RA2A RA2B	.02%/°C .005%/°C .002%/°C	−55°C to +150°C	7.0V ±5%	6000 μmho	40 Minimum 120 Maximum	0.1	45	200
	TEST CONDITIONS				TEST CONDITIONS			
	V_{CB}=3v @ I_C=.1 ma @ R_B=1 K @ I_Z=5 ma				V_{CE}=3v I_C=.1 ma	V_{CB}=45v	I_C=1 ma	I_Z=5 ma
RA3 RA3A RA3B	.02%/°C .005%/°C .002%/°C	−55°C to +150°C	7.0V ±5%	2000 μmho	30 Minimum 90 Maximum	0.1	60	65

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SILICON CONTROLLED SWITCHES (SCS)[4]

Grown Diffused (See Outline Drawing No. 27)

Type	Anode Blocking Voltage	Continuous DC Forward Current 100°C Ambient	Peak Recurrent Forward Current 100 μsec 100°C	Peak Gate Current	Dissipation[5]	MAX. ANODE RATINGS I_B $V_{AC}=+40v$, $R_{GC}=10K$, 150°C	I_R $V_{AC}=-40v$, $R_{GC}=10K$, 150°C	V_F $I_A=50$ ma	I_H $V_{AC}=40v$, $R_{GC}=10K$	MAX. GATE RATINGS I_{GC} $V_{GC}=-2.5v$	I_{GA} $V_{GA}=40v$	Max. I_{GFA} $V_{AC}=40v$, $R_{GC}=0$, $R_L=800$ ohms	GATE INPUT TO FIRE V_{GFA} $V_{AC}=40v$, $R_{GC}=0$, $R_L=800$ ohms	Max. I_{GFC} $V_{AC}=40v$, $R_L=800$ ohms	V_{GFC} $V_{AC}=40v$, $R_L=800$ ohms
	Volts	ma	amp	ma	mw	μa	μa	Volts	ma	μa	μa	ma	Volts	μa	Volts
3N58[1]	40	100	0.5	50	150	20	20	1.5	1.5	20				1.0	0.4 to 0.65
3N59[2]	40	100	0.5	50	150	20		1.5	1.5		20 (150°C)	1.5	−0.6 to −1.2		
3N60[3]	40	100	0.5	50	150	20	20	1.5	1.5	20	0.2 (25°C)	1.5	−0.6 to −1.2	1.0	0.4 to 0.65

NOTES:
(1) For this characterization G_A is electrically open. This corresponds to the conventional SCR configuration.
(2) For this characterization, G_C is connected to C. This corresponds to the complementary SCR configuration.
(3) This characterization is for SCR, complementary SCR[6], and Binistor circuit configurations. The 3N60 meets all specifications for the 3N58 and 3N59.
(4) See Chapter 16, G-E 7th Edition *Transistor Manual*,
(5) Derate at 2.4 mw per °C.
(6) See General Electric *Silicon Controlled Rectifier Manual.*

Planar (See Outline Drawing No. 28)

Type	Anode Blocking Voltage	Continuous DC Forward Current	Peak Recurrent Forward Current 100μsec	Peak Cathode Gate Current	Dissipation	CUTOFF CHARACTERISTICS I_B @V_{AC}	I_B $R_{GC}=10$ K, 150°C	CONDUCTING CHARACTERISTICS V_F @I_F	V_F Maximum	I_H $R_{GC}=10$ K	MAXIMUM GATE RATINGS V_{GC} $I_{GC}=20μa$	V_{GA} $I_{GA}=1μa$	GATE TRIGGERING CHARACTERISTICS I_{GTC} ($V_{AC}=40v$, $R_L=800Ω$, $R_{GA}=\infty$)	V_{GTC} ($V_{AC}=40v$, $R_L=800Ω$, $R_{GA}=\infty$)	I_{GTA} ($V_{AC}=40v$, $R_L=800Ω$, $R_{GC}=10K$)	V_{GTC} ($V_{AC}=40v$, $R_L=800Ω$, $R_{GC}=10K$)
	Volts	ma	amp	ma	mw	Volts	μa	ma	Volts	ma	Volts	Volts	μa	Volts	ma	Volts
3N81	65	200	1.0	500	400	65	20	200	2.0	1.5	5	65	1.0	.4 to .65	1.5	−.4 to −.8
3N82	100	200	1.0	500	400	100	20	200	2.0	1.5	5	100	1.0	.4 to .65	1.5	−.4 to −.8
3N83	70	50	0.1	50	200	70	20*	50	1.4	4.0†	5	70	150†	.4 to .80	—	—
3N84	40	175	0.5	100	320	40	20*	175	1.9	2.0	5	40	10	.4 to .65	—	—
3N85	100	175	0.5	100	320	100	20*	175	1.9	2.0	5	100	10	.4 to .65	—	—
3N86	65	200	1.0	500	400	65	20	200	2.0	0.2	5	65	1.0	.4 to .65	0.1	−.4 to −.8

NOTES: *Measured @125°C.
†Measured in special test circuit (See specification sheet).

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UNIJUNCTIONS

TYPES			R_{BB}	η	I_V	I_P	I_{EO}		V_{OB1}	
Cube Structure Dwg. No. 29	Bar Structure Dwg. No. 30	Bar Structure Dwg. No. 31	Interbase Resistance $V_{BB}=3v$ $I_E=0$ Kohms	Intrinsic Standoff Ratio $V_{BB}=10v$	Min. Valley Current ma	Max. Peak Point Emitter Current μa	Max Emitter Reverse Current μa	 $T_J=25°C$ $@V_{B2E}$	Min. Base One Peak Pulse Voltage Volts	Comments
—	2N2417 2N2417A 2N2417B	2N489(1) 2N489A 2N489B	4.7-6.8	.51-.62	8	12 12 6	2 2 0.2	60 60 30	— 3 3	
—	2N2418 2N2418A 2N2418B	2N490(1) 2N490A 2N490B	6.2-9.1	.51-.62	8	12 12 6	2 2 0.2	60 60 30	— 3 3	
—	2N2419 2N2419A 2N2419B	2N491(1) 2N491A 2N491B	4.7-6.8	.56-.68	8	12 12 6	2 2 0.2	60 60 30	— 3 3	"A" versions are guaranteed in recommended circuit to trigger G.E. SCR's over range $T_A = -55°C$ to 125°C
—	2N2420 2N2420A 2N2420B	2N492(1) 2N492A 2N492B	6.2-9.1	.56-.68	8	12 12 6	2 2 0.2	60 60 30	— 3 3	
—	2N2421 2N2421A 2N2421B	2N493(1) 2N493A 2N493B	4.7-6.8	.62-.75	8	12 12 6	2 2 0.2	60 60 30	— 3 3	
	2N2422 2N2422A 2N2422B —	2N494 2N494A 2N494B 2N494C	6.2-9.1	.62-.75	8	12 12 6 2	2 2 0.2 .02	60 60 30 30	— 3 3 3	"B" versions in addition to SCR triggering guarantees lower I_{EO} and I_P for long timing periods with a smaller capacitor.
—	5G514 5G515 5G516	2N1671 2N1671A 2N1671B	4.7-9.1	.47-.62	8	25 25 6	12 12 0.2	30 30 30	— 3 3 Ind Types	
—	—	2N2160	4.0-12.0	.47-.80	8	25	12	30	3	Low cost UJT.
2N2646	—	—	4.7-9.1	.56-.75	4	5	12	30	3	Low cost UJT.
2N2647	—	—	4.7-9.1	.68-.82	8	2	0.2	30	6	For long timing periods and trigger high current SCR'S.
5E35	—	—	4.7-9.1	.62-.82	Frequency 360-440		12	30	Duty Cycle 45-55	Multivibrators—guaranteed performance at 25° C.
5E36	—	—	4.7-9.1	.62-.82	380-420		1.0	30	47-53	See specification sheet for details
			R_{BB} $V_{BB}=1.5V$ $I_E=0$ Kohms	V_P $V_{BB}=1.5V$ Volts	I_V $V_{BB}=1.5V$ ma	I_P Max. $V_{BB}=1.5V$ μa	I_{EO} Max. $V_{B2E}=30V$ $I_{B1}=0$ μa			
2N2840	—	—	4.7-9.1	1.3-1.5	.2- 7	10	1	—		Low voltage applications.

NOTES: (1) Available as USAF TYPES MIL-T-19500/75.

FUNCTIONAL DEVICES (ACTIVE DISCRETE)

CHOPPERS — NPN Five-terminal Packages Containing Two Matched Pellets

Type	Dwg. No.	MAXIMUM: V_O (Offset Voltage) $I_{B1}=I_{B2}=1$ ma, $I_{E1}=I_{E2}=0$, μ volts	MINIMUM: V_{EEO} $I_{E1E2}=1$ ma, $I_{B1}=I_{B2}$, volts	MAXIMUM: r_s $I_{B1}=1$ ma, $I_{EE}=0.1$ ma, ohms	MAXIMUM: I_{CBO} or I_{CBO2} V_{CB1} or $V_{CB2}=25$v, na
2N2356	32	(1) 300 @ −55°C to +125°C	20	40	10
2N2356A	32	(1) 50 @ −55°C to +125°C	20	40	10
2N3082	33	(2) 350 @ −55°C to +125°C	20	40	10
2N3083	33	(2) 75 @ −55°C to +125°C	20	40	10
4JD12X013	Special	Dual (Four transistor) version of 2N2356			
4JD12X070	Special	Dual (Four transistor) version of 2N2356A			

NOTES: (1) $I_{B1} = I_{B2} = 1$ma (2) $I_{B1} = I_{B2} = 0.25$ma

DARLINGTONS — NPN Four-terminal Package Containing Two Pellets Connected in Darlington Configuration (See Outline Drawing No. 5)

Types	V_{CEO} MINIMUM	h_{FE} MIN.	h_{FE} MAX.	h_{FE} MIN.	h_{FE} MAX.	h_{FE} MINIMUM	I_{CBO}@PV_{CB} MAXIMUM	
	$I_C=30$ ma volts	$I_C=100$ ma		$I_C=10$ ma		$I_C=1$ ma	na	volts
2N997	40	7000	70,000	4000	—	—	10	60
2N998	60(1)	2000	—	1600	8000	800	10	90
2N999	60	7000	70,000	4000	—	—	10	60
2N2785	40(1)	2000	20,000	1200	—	600	50	30

NOTES: (1) V_{CEO} at 20 ma.

DIFFERENTIAL AMPLIFIERS — NPN Six-terminal Packages Containing Two Isolated Pellets

TYPE Dwg. No. 21	Dwg. No. 34	Dwg. No. 35	Dwg. No. 36	V_{CEO} Min. volts	h_{FE}@100 μa Min.	h_{FE}@100 μa Max.	h_{FE1}/h_{FE2} @$I_C=100$ μa	h_{FE}@1 ma Min.	h_{FE}@1 ma Max.	h_{FE1}/h_{FE2} $I_C=1$ ma	Δ V_{BE} 10 μa	Δ V_{BE} 1 ma	MAXIMUM I_{CBO}@V_{CB} na	MAXIMUM I_{CBO}@V_{CB} volts
2N2060	—	—	—	60(1)	30	—	0.9-1.0	30	—	—	—	5	2	80
2N2223	—	—	—	60	25	—	0.8-1.0	—	—	—	—	15(3)	10	80
2N2480	—	—	—	40	20	—	0.8-1.0	30	250	0.8-1.0	—	10	50	60
2N2480A	2N3513	2N3514	2N3515	40	35	—	0.8-1.0	50	200	0.8-1.0	—	5	20	60
2N2652	—	—	—	60	35	—	.85-1.0	50	200	0.85-1.0	—	3	10	60
2N2652A	2N3516	2N3517	2N3518	60	35	—	0.9-1.0	50	200	0.9-1.0	—	3	2	60
12A8	—	—	—	30	30	—	0.6-1.0	—	—	—	—	15(3)	25	30
2N2453	—	2N3519	2N3520	30	80(1)	—	—	150	600	0.9-1.0	3	5	5	30
2N2910	—	—	—	25	70	—	0.8-1.0	80	—	0.8-1.0	10	10	—	—
2N2913	—	—	—	45	100	—	—	150	—	—	—	—	10	45
2N2914	—	—	—	45	225	—	—	300	—	—	—	—	10	45
2N2915	—	—	—	45	100	—	0.9-1.0	150	—	—	5	5	10	45
2N2916	—	—	—	45	225	—	0.9-1.0	300	—	—	5	5	10	45
2N2917	—	—	—	45	100	—	0.8-1.0	150	—	—	10	10	10	45
2N2918	—	—	—	45	225	—	0.8-1.0	300	—	—	10	10	10	45
2N2919	—	—	—	60	100	—	0.9-1.0	150	—	—	5	5	2	45
2N2920	—	—	—	60	225	—	0.9-1.0	300	—	—	5	5	2	45
2N3521	2N3522	2N3523	2N3524	45	155(1)	500	0.8-1.0(1)	200	600(2)	0.8-1.0	5	10	10	45
4JD12X084A	See outline drawing No. 36			Network package (Matched 2N914 pellets @ $I_C=1$ ma. & 10 ma. h_{FE} ± 20%. V_{BE} ± 5mv.)										

NOTES: (1) At $I_C=10$ μa. (2) At $I_C=10$ ma. (3) At 0.1 ma.

SPECIFICATIONS 19

SILICON DIODES

SIGNAL DIODES — Planar Epitaxial

Type	Dwg. No.	MAXIMUM Forward Voltage V_F@ Indicated Fwd, Current Volts	MAXIMUM Reverse Current @ Indicated Voltage I_R 25°C μa	100°C μa	125°C μa	150°C μa	Min. SAT. Voltage or Min. Breakdown Voltage V @ Indicated Reverse Current Volts	Total Capacitance @ Indicated Voltage pf	Reverse Recovery Time t_{rr} @ Noted Condition nsec	MAXIMUM Power Dissipation @ 25°C. mw	MAXIMUM Forward Current Steady State DC ma	Comments
1N251	37	1.0, 5 ma	0.2,-10V 20.0,-20V	10.0,-10V	—	—	40	—	150[5]	150	—	
1N252	37	1.0, 10 ma	0.1,-5V 20.0,-12V	—	10.0,-5V	—	30	—	150[6]	150	—	
1N625	37	1.0, 4 ma	1,-20V	30.0,-20V	—	—	30	—	1000[1]	200	20	
1N626	37	1.0, 4 ma	1,-35V	30.0,-35V	—	—	50	—	1000[1]	200	20	
1N659	37	1.0, 6 ma	5,-50V	25.0,-50V	—	—	50	2.7,-10V	300[4]	250	100	
1N659A	37	1.0, 10 ma	0.025,-50V	—	—	5.0,-50V	75	2.7,-10V	300[4]	250	100	
1N789	37	1.0, 10 ma	1,-20V	30,-20V	—	—	30	—	500[2]	500	180	
1N790	37	1.0, 10 ma	5,-20V	30,-20V	—	—	30	—	250[2]	500	180	
1N791	37	1.0, 50 ma	5,-20V	30,-20V	—	—	30	—	500[2]	500	250	
1N793	37	1.0, 10 ma	1,-50V	30,-50V	—	—	60	—	500[2]	500	180	
1N794	37	1.0, 10 ma	5,-50V	30,-50V	—	—	60	—	250[2]	500	180	
1N795	37	1.0, 50 ma	5,-50V	30,-50V	—	—	60	—	500[2]	500	250	
1N811	37	1.0, 1 ma	1.0,-10V 20.0,-15V	—	10.0,-10V	—	30	—	250[5]	150	40	
1N812	37	1.0, 2 ma	0.1,-10V 20.0,-20V	—	10.0,-10V	—	40	—	250[5]	150	60	
1N813	37	1.0, 5 ma	0.5,-5V 20.0,-10V	—	10.0,-5V	—	20	—	250[5]	150	75	
1N814	37	1.0, 2 ma	0.1,-20V 20.0,-30V	—	10.0,-20V	—	50	—	250[5]	150	60	
1N815	37	1.5, 100 ma	0.5,-5V 20.0,-10V	—	10.0,-5V	—	20	—	250[5]	150	120	
1N891	37	1.0, 50 ma	0.1,-50V	25.0,-50V	—	—	60	—	300[3]	200	—	
1N903	37	1.0, 10 ma	0.1,-40V	10.0,-40V	—	—	40	1.0,-6V	4.0[8]	250	110	
1N903A	37	1.0, 20 ma	0.1,-40V	10.0,-40V	—	—	40	1.0,-6V	4.0[8]	250	75	
1N904	37	1.0, 10 ma	0.1,-30V	10.0,-30V	—	—	30	1.0,-6V	4.0[8]	250	110	
1N904A	37	1.0, 20 ma	0.1,-30V	10.0,-30V	—	—	30	1.0,-6V	4.0[8]	250	110	
1N905	37	1.1, 10 ma	0.1,-20V	10.0,-20V	—	—	20	1.0,-6V	4.0[8]	250	110	
1N905A	37	1.0, 20 ma	0.1,-20V	10.0,-20V	—	—	20	1.0,-6V	4.0[8]	250	110	
1N906	37	1.0, 10 ma	0.1,-20V	10.0,-20V	—	—	20	2.5,-6V	4.0[8]	250	110	
1N906A	37	1.0, 20 ma	0.1,-20V	10.0,-20V	—	—	20	2.5,-6V	4.0[8]	250	110	
1N907	37	1.0, 10 ma	0.1,-30V	10.0,-30V	—	—	30	2.5,-6V	4.0[8]	250	110	
1N907A	37	1.0, 20 ma	0.1,-30V	10.0,-30V	—	—	30	2.5,-6V	4.0[8]	250	110	
1N908	37	1.0, 10 ma	0.1,-40V	10.0,-40V	—	—	40	2.5,-6V	4.0[8]	250	110	
1N908A	37	1.0, 20 ma	0.1,-40V	10.0,-40V	—	—	40	2.5,-6V	4.0[8]	250	110	
1N914 1N4148 1N4531	37 38 39	1.0, 10 ma	0.025,-20V	—	—	50.0,-20V	100	4.0,-0V	4.0[9]	250 500 500	110	
1N914A	37	1.0, 20 ma	0.025,-20V	5.0,-20V	—	50.0,-20V	100	4.0,-0V	4.0[9]	250	110	
1N914B	37	1.0, 100 ma	0.025,-20V	—	—	50.0,-20V	100	4.0,-0V	4.0[9]	250	110	
1N915	37	1.0, 50 ma	0.025,-10V	—	—	—	75	4.0,-0V	10.0[11]	250	—	
1N916 1N4149	37 38	1.0, 10 ma	0.025,-20V	—	—	50.0,-20V	100	2.0,-0V	4.0[9]	250 500	110	
1N916A	37	1.0, 20 ma	0.025,-20V	—	—	50.0,-20V	100	2.0,-0V	4.0[9]	250	110	
1N916B	37	1.0, 20 ma	0.025,-20V	—	—	50.0,-20V	100	2.0,-0V	4.0[9]	250	110	
1N917	37	1.0, 10 ma	0.05,-10V	25.0,-20V	—	—	50	2.5,-0V	3.0[11]	250	—	
1N925	37	1.0, 5 ma	1.0,-10V	20.0,-10V	—	—	40	4.0,-0V	150[5]	500	180	
1N926	37	1.0, 5 ma	0.1,-10V	10.0,-10V	—	—	40	4.0,-0V	150[5]	500	180	
1N927	37	1.0, 10 ma	0.1,-10V 5.0,-50V	10.0,-10V 25.0,-50V	—	—	65	4.0,-0V	150[5]	500	180	
1N997	37	1.0, 10 ma	0.025,-12V	—	—	—	40	—	150[5]	150	—	
1N3062	37	1.0, 20 ma	0.1,-50V	—	—	—	75, 5μa	1.0,-0V	2.0[9]	250	—	
1N3063 1N4305	37 41	0.85,10ma(cc)	0.1,-50V	—	—	100,-50V	75, 5μa	2.0,-0V	2.0[9]	250 500	—	
1N3064 1N4454 1N4532	37 38 39	1.0,10ma(cc)	0.1,-50V	—	—	100,-50V	75, 5μa	2.0,-0V	4.0[11]	250 500 500	—	
1N3065	37	1.0,20ma(cc)	0.1,-50V	—	—	100,-50V	75, 5μa	1.5,-0V	2.0[9]	250	—	
1N3066	37	1.0, 10 ma	0.1,-50V	—	—	100,-50V	75, 5μa	1.0,-0V	2.0[9]	250	—	
1N3067	37	1.0, 5 ma	0.1,-20V	—	—	100,-20V	30, 5μa	4.0,-0V	2.0[9]	250	—	

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Type	Dwg. No.	Forward Voltage V_F@ Indicated Fwd. Current Volts	MAXIMUM Reverse Current @ Indicated Voltage I_R 25°C μa	100°C μa	125°C μa	150°C μa	Min. SAT. Voltage or Min. Breakdown Voltage V @ Indicated Reverse Current Volts	Total Capacitance @ Indicated Voltage pf	Reverse Recovery Time t_{rr} @ Noted Condition nsec	MAXIMUM Power Dissipation @ 25°C. mw	Forward Current Steady State DC ma	Comments
1N3068	37	1.0, 5 ma	0.1,-20V	—	—	100,-20V	30, 5μa	6.0,-0V	50.0(10)	250	—	
1N3124	37	1.0, 20 ma	0.1,-40V	10.0,-40V	—	—	40	2.0,-6V	4.0(8)	125	50	
1N3206	37	1.0, 10 ma	0.025,-20V 5.0,-80V	—	—	50,-20V	100	4.0,-0V	4.0(11)	150	—	
1N3600 1N4150	37 38	1.0,200ma(cc)	0.1,-50V	—	—	100,-50V	50	2.5,-0V	6.0(12)	500	—	
1N3604 1N4151	37 38	1.0, 50 ma	0.05,-50V	—	—	50,-50V	75, 5μa	2.0,-0V	2.0(9)	250 500	115	Very high speed, high conductance, computer diode. Subminiature package.
1N3605 1N4152 1N4533	37 38 39	See Table 1	0.05,-30V	—	—	50,-30V	40, 5μa	2.0,-0V	2.0(9)	250 500 500	115	Controlled conductance, very high speed diode. Sub-Subminiature package.
1N3606 1N4153 1N4534	37 38 39	See Table 1	0.05,-50V	—	—	50,-50V	75, 5μa	0.0,-0V	2.0(9)	250 500 500	115	
1N3607	40	1.0, 50 ma	0.05,-50V	—	—	50,-50V	75, 5μa	2.0,-0V	2.0(9)	150	115	Very high speed, high conductance diode in microminiature package.
1N3608	40	See Table 1	0.05,-30V	—	—	50,-30V	40, 5μa	2.0,-0V	2.0(9)	150	115	
1N3609	40	See Table 1	0.05,-50V	—	—	50,-50V	75, 5μa	2.0,-0V	2.0(9)	150	115	Controlled conductance, very very high speed diode in microminiature package.
1N3873 1N3873/HR	37 37	0.85,20ma(cc)	0.1,-50V	—	—	40,-50V	50	4.0,-0V	4.0(11)	250	200	Very high speed, electrically identical to the Polaris G-321 high reliability diode.
1N4009 1N4154 1N4536	37 38 39	1.0, 30 ma	0.1,-25V	—	—	100,-25V	35, 5μa	4.0,-0V	2.0(9)	250 500 500	115	Economy type.

Type	Dwg. No.	Forward Voltage	25°C	100°C	125°C	150°C	Min. SAT./Breakdown	Total Capacitance	Reverse Recovery	Power Dissipation	Forward Current	Comments
1N4043 1N4306 1N4307	40 43 43	1.0, 30 ma	0.1,-25V	—	—	100,-25V	35, 5μa	4.0,-0V	2.0(9)	150	115	
These types appear under section "Matched Pairs and Quads".												

Kovar Tab

Type	Dwg. No.	Forward Voltage	25°C	100°C	125°C	150°C	Min. SAT./Breakdown	Total Capacitance	Reverse Recovery	Power Dissipation	Forward Current	Comments
KSD101	44	1 @ 30 ma	0.1,-25V	—	—	50-25V	35	4	2(9)	—	—	

Stabistors (1, 2, or 3 diode pellets in a series)

Type	Dwg. No.	Forward Voltage	25°C	100°C	125°C	150°C	Min. SAT./Breakdown	Total Capacitance	Reverse Recovery	Power Dissipation	Forward Current	Comments
1N4156	42	See Table 2	0.05,-20V	—	—	50,-20V	30, 5μa	25.0,-0V	—	400	—	DHD Stabistor with controlled conductance and stored charge of 50 pc Min. @I_F=1 ma.
1N4157	41	See Table 3	0.05,-20V	—	—	50,-20V	30, 5μa	20.0,-0V	—	400	—	
1N4453	38	See Table 4	0.05,-20V	—	—	50,-20V	30, 5μa	30.0,-0V	—	400	—	

TABLE 1			TABLE 2			TABLE 3		TABLE 4	
I_F	V_F		I_F	V_F		V_F		V_F	
ma	Min. mv	Max. mv	ma	Min. mv	Max. mv	Min. mv	Max. mv	Min. mv	Max. mv
0.1	0.490	0.550	0.01	0.74	1.09	1.19	1.54	.430	.550
0.25	0.530	0.590	0.1	0.97	1.22	1.52	1.77	.510	.630
1.0	0.590	0.670	1.0	1.21	1.41	1.85	2.05	.600	.710
2.0	0.620	0.700	10.0	1.38	1.58	2.12	2.32	.690	.800
10.0	0.700	0.810	100.0	1.54	1.84	2.36	2.66	.800	.920
20.0	0.740	0.880	—	—	—	—	—	—	—

NOTES:

(1) Recovery to 400K, switching from 30 ma forward to −35 volts. IBM Y circuit.
(2) Recovery to 200K, switching from 5 ma forward to −40 volts. JAN 256 circut.
(3) Recovery to 80K, switching from 5 ma forward to −40 volts. JAN 256 circuit.
(4) Recovery to 400K, switching from 30 ma forward to −35 volts. JAN 256 circuit.
(5) Recovery to 20K, switching from 5 ma forward to −10 volts. JAN 256 circuit.
(6) Recovery to 40K, switching from 5 ma forward to −10 volts. JAN 256 circuit.
(7) Recovery to 40K, switching from 10 ma forward to −10 volts. JAN 256 circuit.
(8) Recovery to 1.0 ma reverse, switching from 10 ma forward to −5.0 volts R_L=100 ohms.
(9) Recovery to 1.0 ma reverse, switching from 10 ma forward to −6.0 volts. R_L=100 ohms.
(10) Recovery to 1.0 ma reverse, switching from 30 ma forward to 30 ma reverse. R_L=150 ohms.
(11) I_F=I_R=10 ma, recovery to 1 ma.
(12) I_F=10 ma, I_R=1 ma, recovery to 0.1 ma.

Diffused Junction Diodes* (See Outline Drawing No. 37)

Types	MAXIMUM (25°C. unless otherwise specified) Continuous Peak Inverse Voltage Volts	Transient Peak Inverse Voltage Volts	Forward Current ma 25°C	Forward Current ma 100°C	Surge Current (1 Second) Amps	Reverse Current At P.I.V. 25°C μa	Reverse Current At P.I.V. 100°C μa	Forward Voltage V_F Volts	Total Capacitance V_R=−12 volts pf
62J2 through 66J2	200-600	270-720	400	150	2.5	1-0.5	65-50	1.25 at 400 ma	9

* Made in France for General Electric by the Societe Europeenne Des Semiconducteurs (SESCO).

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Subminiature Point Contact Diodes* (See Outline Drawing 37)

Types	MAXIMUM Peak Inverse Voltage Volts	MAXIMUM Average Forward Current[1] ma	MAXIMUM Surge Current[2] ma	MAXIMUM Reverse Current I_R 25°C μa	MAXIMUM Reverse Current I_R 150°C μa	TOTAL CAPACITANCE V_R= −2 volts pf	TOTAL CAPACITANCE V_R= −40 volts pf
12P2 through 19P2	200-10	40	120	0.5	100	0.4	0.3
23J2 through 28J2	200-10	60	120	0.2[3]	100	0.4	0.3

NOTES: *Made in France for General Electric by the Societe Europeenne Des Semiconducteurs (SESCO).
(1) For types 12P2 and 19P2 this parameter is 60 ma
(2) For types 12P2 and 19P2 this parameter is 180 ma
(3) For 90% of the production, the inverse current is less than 0.1 μa.

Matched Pairs and Quads (See Outline Drawing No. 43)

Type	MAXIMUM Forward Voltage V_F Volts	MAXIMUM Reverse Current I_R 25°C μa	MAXIMUM Reverse Current I_R 150°C μa	Min. Breakdown Voltage V I_R=5 μa Volts	ΔV_F—Max. Forward Voltage difference between diodes in pairs or quads (T_A=−55°C to +125°C) I_F=0.1 to 10 ma mv	ΔV_F I_F=10 to 50 ma mv	MAX. Forward Current Steady State DC ma	Comments
MP-1 (1N4306)	See above*	.05 @ 50V	50 @ 50V	75	10	20		(MP-1 was formerly 1N4306) Matched pairs in molded package. (Silicon Signal Diodes)
MP-2	1.0 @ 10 ma	.10 @ 30V	100 @ 30V	40	10	50		
MQ-1 (1N4307)	See above*	.05 @ 50V	50 @ 50V	75	10	20		(MQ-1 was formerly 1N4307) Matched quads in molded package. (Silicon Signal Diodes)
MQ-2	1.0 @ 10 ma	.10 @ 30V	100 @ 30V	40	10	50		

*

Type	I_F ma	Forward Voltage V_F Min.	Forward Voltage V_F Max.
MP-1 and MQ-1	.100	.440	.550
	1	.560	.670
	10	.670	.810
	100	.750	1.000

Snap-off Diodes (See Outline Drawing No. 37)

Type	Power Dissipation 25°C mw	Peak Surge Current 1 μs amperes	MINIMUM Breakdown Voltage I_R=5μamps B_V Volts	MAXIMUM Capacitance V_R=0V, f=1 mc C_o pf	MINIMUM Stored Charge Q_f pc/ma	TYP. Snap-off time T_S=2 nsec. I_F=20 ma t_{sp} nsec.	MAX. Snap-off time (I_F=20 ma) nsec.	TYP. Snap-off time T_S=2 nsec. I_F=100 ma tsp nsec.	MAX. Snap-off time (I_F=100 ma) nsec.
SSA-550[2]/554[3]	250	2	12	1.5	20	0.3	0.5		
SSA-551[2]/555[3]	250	2	8	4.0	20	0.3	0.5		
SSA-552[2]/556[3]	250	2	12	1.5	1.0			0.2[1]	0.4
SSA-553[2]/557[3]	250	2	8	4.0	1.0			0.2[1]	0.4

NOTES: (1) Limited by resolution time of test equipment. (2) DO-7 package. (3) Micro Silicon Diode—see Specifications 75. 28 for outline dimensions.

Microphoto Diodes*[1] — NPN (See Outline Drawing No. 45)

Type	MAX.[2] Bias Volts	MAX.[2] P_C mw	MAX. DARK CURRENT at 24 vdc μa	TYPICAL DARK CURRENT at 24 vdc μa	TYPICAL SENSITIVITY[3, 4] at 250 ft. —c. μa/ft. —c.	TYPICAL SENSITIVITY[3, 4] at 1000 ft. —c. μa/ft. —c.	TYPICAL PHOTOCURRENT DECAY TIMER μsec.
31F2	40	50	0.1	0.02	0.2	0.8	1
32F2	40	50	0.1	0.02	0.5	1.5	1
33F2	40	50	0.1	0.02	0.9	2.2	1
34F2	40	50	0.1	0.02	1.6	5.0	1

NOTES: *Made in France for General Electric by the Societe Europeenne Des Semiconducteurs (SESCO).
(1) All specs at 25°C unless noted otherwise.
(2) Storage temperature on all types is −65 to +125°C. Operating temperature on all types is −65 to +100°C.
(3) Light source—Tungsten Filament Lamp Operated at a Color Temperature of 2870°K.
(4) Maximum Sensitivity wave length 0.9 to 1.0 microns.

GERMANIUM DIODES

SIGNAL DIODES — Point-Contact[1] [4] (See Outline Drawing No. 37)

Type No.	PRV	Max. Cont. Reverse Voltage	Maximum Forward Current — ma			Min. Forward Current @ +1V ma	Maximum Reverse Current				Comments
			Average	Recurrent Peak	1 sec. Surge		Volts	μa	Volts	μa	
1N34	75	60	50	150	500	5.0	−10	50	−50	800	General purpose
1N34A	75	60	50	150	500	5.0	−10	30	−50	500	
1N35[2]	75	60	50	150	500	7.5	−10	10			Matched pair of 1N34A
1N38	120	100	50	150	500	3.0	−3	6	−100	500	
1N38A	120	100	50	150	500	4.0	−3	6	−100	500	High reverse voltage
1N38B	100		50	150	500	4.0	−3	6	−100	500	
1N48	85	70	40	150	400	4.0	−50	833			
1N51	50	40	20	100	300	2.5	−50	1660			
1N52	85	70	40	150	400	4.0	−50	150			
1N52A		50	40	150	400	5.0	−50	100			General purpose detector
1N54	50	35	40	150	500	5.0	−10	10			
1N54A	75	50	40	150	500	5.0	−10	7	−50	60	
1N58	120	100	40	150	500	5.0	−100	600			
1N58A	120	100	40	150	500	5.0	−100	600			High reverse voltage
1N63	125	100	40	150	400	4.0	−50	50			
1N65	85	70	40	150	400	2.5	−50	200			
1N67	100	80	35	100	500	4.0	−5	5	−50	50	General purpose
1N67A	100	80	30	100	300	4.0	−5	5	−50	50	
1N68A	130	100	30	100	500	3.0	−100	625			High reverse voltage
1N69	75	60	40	125	400	5.0	−10	50	−50	850	
1N69A	75	60	40	125	400	5.0	−10	30	−50	500	
1N70	125	100	30	90	350	3.0	−10	25	−50	300	General purpose
1N70A	125	100	30	90	350	3.0	−10	25	−50	300	
1N75	125	100	40	150	400	2.5	−50	50			

Type No.	PRV	Max. Cont. Reverse Voltage	Average	Recurrent Peak	1 sec. Surge	Min. Forward Current @ +1V ma	Volts	μa	Volts	μa	Comments
1N81	50	40	40	90	350	3.0	−10	10			
1N81A	50	40	30	90	350	3.0	−10	10			General purpose
1N90	75	60	30	150	500	5.0	−50	500			
1N116	75	60	30		250	5.0	−50	100			Low leakage
1N126	75	60	30	90	350	5.0			−50	850	General purpose
1N126A	75	60	30	90	350	5.0	−10	50	−50	300	
1N127	125	100	30	90	300	3.0			−50	300	
1N127A	125	100	30	90	300	3.0	−10	25	−50	200	General purpose
1N128	50	40	30	90	300	3.0	−10	10			
1N191	90	70	30	90	300	5.0	−10	25	−50	125	Computer diode
1N192	80	55	30	90	300	5.0	−10	20	−50[5]	100[5]	
1N198	100	80	30	90	300	4.0	−10	10	−50	250[6]	High temp. "JAN" diode
1N198A	100	80	30	90	300	4.0	−10	10	−50[6]	250[6]	High temp. low leakage
1N636	60	45	30			2.5	−10	10			Low leakage
1P541[3]	45	30	10	100	200	1.5 mA @ 1V .1 mA @ .3V	−1.5	2.8	−10	18	A.M. detector
1P542[3]	The 1P542 is a matched pair of 1P541										F.M. ratio detector

NOTES:
(1) Made in Canada by Canadian General Electric.
(2) Each diode current at +1V matched to within 10%.
(3) The 1P541 and 1P542 are very similar to the 1N541 and 1N542 electrically but are in a smaller case.
(4) All measurements at 25°C unless otherwise specified.
(5) Measured at 55°C.
(6) Measured at 65°C.

Bonded-Junction Diodes[1] (See Outline Drawing No. 37)

Type No.	PRV	Max. Cont. Reverse Voltage	Maximum Forward Current — ma			Min. Forward Current @ +1V ma	Maximum Reverse Current				Comments
			Average	Recurrent Peak	1 sec. Surge		Volts	μa	Volts	μa	
1N56A	50	40	60	200	1.000	15			−30	300	General purpose
1N96A	75	60	70	250	400	40			−50	500	
1N97A	100	80	30		250	20	−5	8	−50	100	
1N98A	100	80	70	250	400	40	−5	8	−50	100	High conductance
1N99A	100	80	30		300	20	−5	5	−50	50	
1N100A	100	80	70	250	400	40	−5	5	−50	50	
1N117A	75	60	40		300	20			−50	100	General purpose

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Type No.	PRV	Max. Cont. Reverse Voltage	Maximum Forward Current — ma			Min. Forward Current @ + 1V ma	Maximum Reverse Current				Comments
			Average	Recurrent Peak	1 sec. Surge		Volts	μa	Volts	μa	
1N118A	75	60	70	250	400	40			−50	100	
1N273	35	30	80		450	100	−20	20			
1N279	39	30	80		450	100	−20	200			High conductance
1N281	75	60	75		400	100	−10	30	−50	500	
1N292	75	60	70		150	100			−50	200	
1N298A	85	70	30		300	3.5	−5	10	−40(2)	250(2)	Computer diode
1N309	40	30	100			100	−20	100			High conductance
1N313		100	40		500	20	−20	10	−100	50	Low leakage diode
1N449	40	30	60			50	−10	10	−30	30	High conductance
1N497	30	20	60			100	−20	20			Low leakage
1N774	70	60	50		450	100	−10	15	−50	150	High conductance
1N776	30	20	45		400	50	−10	200	−30	500	
1N777	70	60	50		450	100	−10	25(3)	−50(3)	125(3)	Switching diode

NOTES: (1)Measured at 75°C unless otherwise specified. (2)Measured at 50°C. (3)Measured at 55°C.

Video Detector Diodes** (See Outline Drawing No. 37)

Type No.	PRV	Maximum Reverse Current		Max. Average Rectified Forward Current (ma)
		Volts	μa	
1N60	30	−10	67	50
1N60A	40	−10	60	50
1N60C	50	−10	67	50
1N64	25	−10	100	50
1N87A	30	−1.5	30	50
1N295A	40	−10	200	35
1N616	30	−10	100	50

** Made in Canada by Canadian General Electric.

TUNNEL DIODES — General Purpose

Type	Dwg. No.	Peak Point Current I_P ma	MAXIMUM		Peak Voltage V_P mv	Max. Series Resist. R_S Ohms	Negative Conductance —G mhos × 10^{-3}	Typical Resistive Cutoff Frequency f_{ro} KMC	Comments
			Valley Point Current I_V ma	Capacitance C pf					
1N2939	46	1.0 ± 10%	0.14	15	65 Typ.	4.0	6.6 Typ.	2.2	General purpose switching, oscillator, amplifier and converter circuits. Nominal series inductance, Ls, is 4 nh. TO-18 package.
1N2939A	46	1.0 ± 2.5%	0.14	10	60 ± 10	4.0	6.6 Typ.	2.6	
1N2940	46	1.0 ± 10%	0.22	10	65 Typ.	4.0	6.6 Typ.	2.2	
1N2940A	46	1.0 ± 2.5%	0.22	7	65 ± 10	4.0	6.6 Typ.	2.6	
1N2941	46	4.7 ± 10%	1.04	50	65 Typ.	2.0	30 Typ.	2.6	
1N2941A	46	4.7 ± 2.5%	1.04	30	65 ± 10	2.0	30 Typ.	3.9	
1N2969	46	2.2 ± 10%	0.48	25	65 Typ.	3.0	16 Typ.	2.5	
1N2969A	46	2.2 ± 2.5%	0.48	15	65 ± 10	3.0	16 Typ.	3.3	
1N3149	46	10.0 ± 10%	2.2	90	65 Typ.	1.5	60 Typ.	2.6	
1N3149A	46	10.0 ± 2.5%	2.2	50	65 ± 10	1.5	60 Typ.	3.1	
1N3150	46	22.0 ± 10%	4.8	150	65 Typ.	1.0	100 Typ.	2.2	
1N3712 (TD-1)	47	1.0 ± 10%	0.18	10	65 Typ.	4.0	8 Typ.	2.3	General purpose switching, oscillator, amplifier and converter circuits. Miniature axial package with series inductance, Ls, of 0.5 nh. MIL qualified units available for "A" versions.
1N3713 (TD-1A)	47	1.0 ± 2.5%	0.14	5	65 ± 7	4.0	8.5 ± 1	3.2	
1N3714 (TD-2)	47	2.2 ± 10%	0.48	25	65 Typ.	3.0	18 Typ.	2.2	
1N3715 (TD-2A)	47	2.2 ± 2.5%	0.31	10	65 ± 7	3.0	19 ± 3	3.0	
1N3716 (TD-3)	47	4.7 ± 10%	1.04	50	65 Typ.	2.0	40 Typ.	1.8	
1N3717 (TD-3A)	47	4.7 ± 2.5%	0.60	25	65 ± 7	2.0	41 ± 5	3.4	
1N3718 (TD-4)	47	10.0 ± 10%	2.20	90	65 Typ.	1.5	80 Typ.	1.6	
1N3719 (TD-4A)	47	10.0 ± 2.5%	1.40	50	65 ± 7	1.5	85 ± 10	2.8	
1N3720 (TD-5)	47	22.0 ± 10%	4.80	150	65 Typ.	1.0	180 Typ.	1.6	
1N3721 (TD-5A)	47	22.0 ± 2.5%	3.10	100	65 ± 7	1.0	190 ± 30	2.6	
TD-9	47	0.5 ± 10%	0.10	5	60 Typ.	6.0	4.0 Typ.	1.3	

Ultra-High Speed Switching (See Outline Drawing No. 48)

Type	Peak Point Current I_P ma	MAXIMUM Valley Point Current I_V ma	MAXIMUM Capacitance C pf	VOLTAGE Peak Point V_P mv	VOLTAGE Forward $I_F=0.25\ I_P$ V_{FS} mv	VOLTAGE Forward $I_F=I_P$ V_{FP} mv	Typical Series Resistance R_S ohms	Typical Rise Time t_r psec.	Comments
TD-251	2.2 ± 10%	0.31	3.0	70 Typ.	420 Min.	500-650	5.0	430	Extremely high speed memory circuits, logic circuits, pulse generators and threshold detectors. Housed in a subminiature epoxy package with series conductance, Ls, of 1.5 nh.
TD-251A	2.2 ± 10%	0.31	1.0	110 Max.	420 Min.	500-650	7.0	160	
TD-252	4.7 ± 10%	0.60	4.0	80 Typ.	435 Min.	500-650	3.5	320	
TD-252A	4.7 ± 10%	0.60	1.0	120 Max.	435 Min.	500-650	4.0	74	
TD-253	10.0 ± 10%	1.40	9.0	75 Typ.	450 Min.	500-650	1.7	350	
TD-253A	10.0 ± 10%	1.40	5.0	80 Typ.	450 Min.	520-650	2.0	190	
TD-253B	10.0 ± 10%	1.40	2.0	120 Max.	450 Min.	550-650	2.5	68	
TD-254	22.0 ± 10%	3.80	18.0	90 Typ.	520 Typ.	600 Typ.	1.8	185	
TD-254A	22.0 ± 10%	3.80	4.0	120 Max.	460 Min.	550-650	2.0	64	
TD-255	50.0 ± 10%	8.50	25.0	110 Typ.	530 Typ.	625 Typ.	1.4	100	
TD-255A	50.0 ± 10%	8.50	5.0	130 Typ.	480 Min.	640 Typ.	1.5	35	
TD-256	100 ± 10%	17.50	35.0	150 Typ.	530 Typ.	650 Typ.	1.1	57	
TD-256A	100 ± 10%	17.50	6.0	180 Typ.	500 Min.	660 Typ.	1.2	22	

Microwave (See Outline Drawing No. 49)

Type	Typical Peak Point Current I_P ma	Negative Resistance —R ohms	Maximum Junction Capacitance C_j pf	Maximum Series Resistance R_S ohms	Minimum Resistive Cutoff Frequency f_{ro} GC	Comments
TD-401	2.0	65-75	2.60	5	5	High performance microwave pill package with series inductance, Ls, of 0.1 nh and package capacitance, C_P, of 0.1 Pf. Units can be stud mounted on request.
TD-402	2.0	65-75	1.30	5	10	
TD-403	2.0	65-75	0.89	5	15	
TD-404	2.0	65-75	0.67	5	20	
TD-405	2.0	65-75	0.54	6	25	
TD-406	2.0	65-75	0.45	6	30	
TD-407	2.0	65-75	0.40	6	35	
TD-408	2.0	65-75	0.35	6	40	

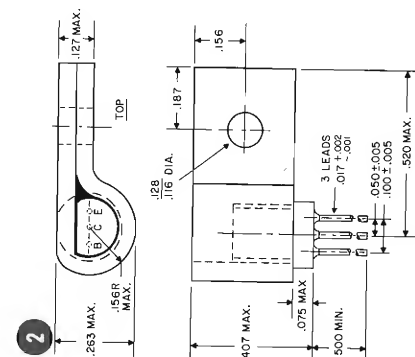
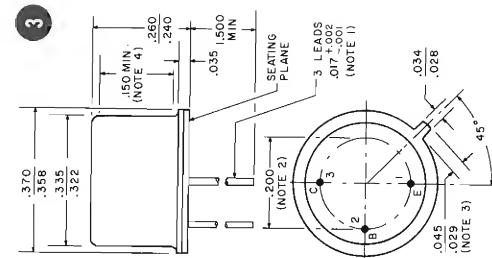
Back Diodes

Type	Dwg. No.	MAXIMUM Peak Point Current I_P ma	MAXIMUM Total Capacitance C pf	MINIMUM Reverse Voltage V_{R1} ($I_R=I_P$ max) mv	MINIMUM Reverse Voltage V_{R2} ($I_R=1$ ma) mv	Forward Current I_{F1} ($V_{F1}=90 \pm 10$ mv) ma	Typical Forward Voltage V_{F2} ($I_{F2}=3\ I_{F1}$) mv	Comments
BD-1	50	1.0	20	440	440	10.0	120	BD-1 through -7 are general purpose types for use in mixer, detectors and switching circuits housed in miniature axial package. BD-400 series are microwave versions featuring low capacitance and a pill package with a series inductance Ls, of 0.1 nh.
BD-2	50	0.5	10	420	465	5.0	130	
BD-402	49	0.5	3	420	465	5.0	130	
BD-3	50	0.2	10	400	465	2.0	170	
BD-403	49	0.2	1	400	465	2.0	170	
BD-4	50	0.1	10	380	465	1.0	170	
BD-404	49	0.1	1	380	465	1.0	170	
BD-5	50	0.05	10	350	465	0.5	160	
BD-405	49	0.05	1	350	465	0.5	160	
BD-6	50	0.02	10	330	465	0.2	160	
BD-406	49	0.02	2	330	465	0.2	160	
BD-7	50	0.01	10	300	465	0.1	160	
1N4090	48	0.2	1.5	430	500	2.0 ($V_{F1}=100 \pm 20$ MV)	170	Low noise mixer.

GALLIUM ARSENIDE TUNNEL DIODES (See Outline Drawing No. 50)

Type	Peak Point Current I_P ma	MAXIMUM Valley Point Current I_V ma	MAXIMUM Capacitance C pf	Peak Voltage V_P mv	Forward Voltage ($I_F=I_P$) V_{FP} mv	Negative Conductance —G mhos $\times 10^{-3}$	Max. Series Resist. R_S ohms	Comments
1N3118	10±10%	1.10	20	160 typ.	900 min.	40	5	Oscillator circuits where wide voltage swing is required. Series inductance, Ls, is 4 nh. TO-18 package.

NOTES:

TRANSISTOR OUTLINE DRAWINGS

4
DIMENSIONS WITHIN JEDEC OUTLINE TO-46
NOTE 1: Lead diameter is controlled in the zone between .050 and .250 from the seating plane. Between .250 and end of lead a max. of .021 is held.
NOTE 2: Leads having maximum diameter (.019) measured in gaging plane .054 + .001 − .000 below the seating plane of the device shall be within .007 of true position relative to a maximum width tab.
NOTE 3: Measured from max. diameter of the actual device.
ALL DIMEN. IN INCHES AND ARE REFERENCE UNLESS TOLERANCED
5
DIMENSIONS WITHIN JEDEC OUTLINE TO-5
NOTE 1: Lead diameter is controlled in the zone between .050 and .250 from the seating plane. Between .250 and end of lead a max. of .021 is held.
NOTE 2: Leads having maximum diameter (.019) measured in gaging plane .054 + .001 − .000 below the seating plane of the device shall be within .007 of true position relative to a maximum width tab.
NOTE 3: Measured from max. diameter of the actual device.
NOTE 4: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed .010.
ALL DIMEN. IN INCHES AND ARE REFERENCE UNLESS TOLERANCED
6
ALL DIMEN. IN INCHES AND ARE REFERENCE UNLESS TOLERANCED
NOTE 1: Lead diameter is controlled in the zone between .050 and .250 from the base seat. Between .250 and end of lead a max. of .021 is held.
NOTE 2: Insulated mounting hardware shown below is supplied. For this service a .187 clearance hole is recommended.
2 MICA WASHERS O.D. X .005 THK
FLAT WASHER .317 O.D. X .032 THK
INT. LOCK WASHER
TEFLON SPACER .182 O.D. X .040 THK
#6-32 NUT
CONNECTED TO CASE

7
DIMENSIONS WITHIN JEDEC OUTLINE TO-8
MOUNTING PLATE
#4-40 X 5/16 SCREW
PANEL: #31 DRILL (.120 DIA.)
LOCKWASHER O.D. .270 MAX
#4-40 NUT
GROUNDED TO CASE
INSULATED MOUNTING
#2-56 X 3/8 SCREW
SHOULDER WASHER
INSULATOR
#42 DRILL (.0935)
LOCKWASHER
#2-56NUT
NOTE 1: LEADS ARE GOLD PLATED UNLESS TINNING IS REQUESTED.
NOTE 2: INSULATED HARDWARE IS PROVIDED.
ALL DIMEN. IN INCHES AND ARE REFERENCE UNLESS TOLERANCED

8
ALL DIMENSIONS IN INCHES AND ARE REFERENCE UNLESS TOLERANCED
#4-40 NUT
#4 INT. L.W.
MAX. TORQUE 5.5 IN LBS. #4-40 X 5/16 SLOTTED PAN H SCR. FOR UP TO .125 THK PANEL
NOTE 1: Lead diameter is controlled in the zone between .050 and .250 from the base seat. Between .250 and end of lead a max. of .021 is held.
NOTE 2: All auxiliary metal hardware is stainless steel. All hardware shown will be shipped with device, including electrical isolation hardware shown below.

MAX TORQUE 3.2 IN LBS #2-56X 3/8 SLOTTED PAN H.SCR. FOR UP TO .160 THK. PANEL
INSULATED SHOULDER WASHER
INSULATED MOUNTING
#2-INT L.W.
MICA WASHER .003 THK. (SAME CONTOUR AS HEATSINK)
#2-56 NUT

9
NOTE 1: Lead diameter is controlled in the zone between .050 and .250 from the cap or base seat. Between .250 and end of lead a max. of .021 is held.
NOTE 2: Clearance is provided to bend all leads for overhead circuitry without interfering with heat sink mounting on chassis.
.035 MAX INSULATING TUBING
ALL DIMENSIONS IN INCHES AND ARE REFERENCE UNLESS TOLERANCED

13

#10-32 NUT, #10-32 NF 2A P.D.=.1697 MAX, MAX TORQUE 12 IN LBS; #10 WASHER .475 O.D. X .040 THK; TEFLON SPACER .272 O.D. X .050 THK; PANEL MAX 7/32 THK (NOTE 2); 2 MICA WASHERS .630 MAX O.D. X .004 THK; 3 LEADS .017 +.002 −.001 (NOTE 1)

NOTE 1: Lead diameter is controlled in the zone between .050 and .250 from the base seat. Between .250 and end of lead a max. of .021 is held.

NOTE 2: Provision is made for the device to be electrically insulated from mounting surface as shown above. For this service a clearance hole of .281 is recommended.

NOTE 3: All exposed metal parts are nickel plated.

ALL DIMENSIONS ARE REFERENCE UNLESS TOLERANCED
(3 LEADS 90° APART)

14

.415/.385 DIA. PIN CIRCLE; C (GROUNDED TO HOUSING); .044 MIN I.D.; .150 MAX; SEATING PLANE; ¼-28 UNF-2A (P.D. .2268 MAX) (NOTE 1); MICA WASHERS—.860 O.D. MAX. X .005 THK.; TEFLON SPACER—.315 O.D. X .050 THK.; PANEL - ⅛ THK. MAX. (NOTE 2); FLAT WASHER—.750 O.D. X .063 THK.; INT. LOCKWASHER; ¼ X 28 NUT

NOTES:
1. MAX. TORQUE TO BE APPLIED TO STUD IS 20 INCH POUNDS.
2. INSULATED MOUNTING HARDWARE IS SUPPLIED. FOR THIS SERVICE A .321 DIA. MAX. PANEL HOLE IS RECOMMENDED.

15

.210/.190 DIA. PIN CIRCLE; C (GROUNDED TO HOUSING); .041 MIN I.D.; .135 MAX; SEATING PLANE; #10-32 NF-2A (P.D. .1697 MAX.) (NOTE 1); MICA WASHERS—.630 O.D. MAX. X .004 THK.; TEFLON SPACER—.272 O.D. X .050 THK.; 3/16 THK MAX. PANEL (NOTE 2); #10 FLAT WASHER—.475 O.D. X .050 THK; INT. LOCKWASHER; #10-32 NUT

NOTES:
1. MAX. TORQUE TO BE APPLIED TO STUD IS 12 INCH POUNDS.
2. INSULATED MOUNTING HARDWARE IS SUPPLIED. FOR THIS SERVICE A .281 DIA. MAX. PANEL HOLE IS RECOMMENDED.

22

.530 / .395 — .375 / .335 — .036 MAX. — .320 / .300 — 1.5 MIN — BASE SEAT — .395 / .255 — .235 / .195 — .048 — .048 — .192

3 LEADS .017 +.002 −.001 (NOTE 1)

NOTE 1: Lead diameter is controlled in the zone between .050 and .250 from the base seat. Between .250 and end of lead a max. of .021 is held.

ALL DIMEN. IN INCHES AND ARE REFERENCE UNLESS TOLERANCED

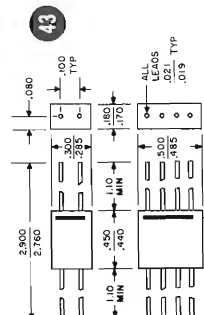
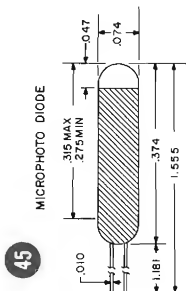
ALL LEADS ARE ISOLATED FROM CASE

SPECIAL SILICON PRODUCT OUTLINE DRAWINGS

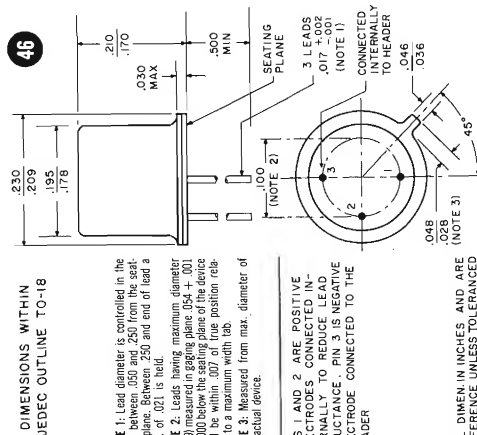
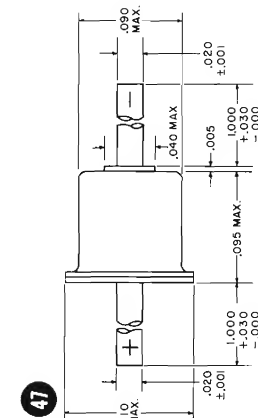
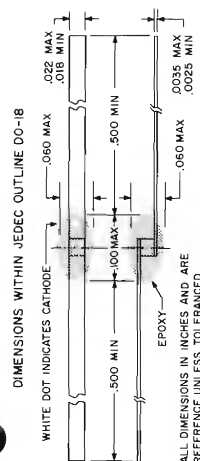
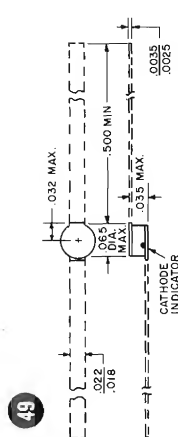
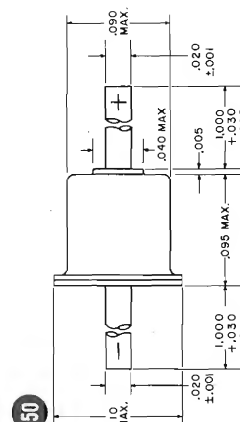
FUNCTIONAL DEVICE OUTLINE DRAWINGS

45
MICROPHOTO DIODE
.315 MAX
.275 MIN
.047
.074
.010
.374
1.555
1.181
ALL DIMENSIONS IN INCHES AND ARE REFERENCE UNLESS TOLERANCED

46
DIMENSIONS WITHIN JEDEC OUTLINE TO-18
.230
.209
.195
.178
.210
.170
.030 MAX
.500 MIN
SEATING PLANE
3 LEADS .017 +.002 -.001 (NOTE 1)
CONNECTED INTERNALLY TO HEADER
.046
.036
45°
.100 (NOTE 2)
.048
.028
(NOTE 3)
NOTE 1: Lead diameter is controlled in the zone between .050 and .250 from the seating plane. Between .250 and end of lead a max. of .021 is held.
NOTE 2: Leads having maximum diameter (.019) measured in gaging plane .054 + .001 − .000 below the seating plane of the device shall be within .007 of true position relative to a maximum width tab.
NOTE 3: Measured from max. diameter of the actual device.
PINS 1 AND 2 ARE POSITIVE ELECTRODES CONNECTED INTERNALLY TO REDUCE LEAD INDUCTANCE. PIN 3 IS NEGATIVE ELECTRODE CONNECTED TO THE HEADER
ALL DIMEN. IN INCHES AND ARE REFERENCE UNLESS TOLERANCED

44
.080 MAX
.060 MAX
C*
A**
EPOXY
GOLD FLASH KOVAR
.005
.250 MIN
.010 TYP
.006 TYP
.030 MAX
.100 MAX
.350 MIN
NOTE: BOTH 1-LEAD AND 2-LEAD VERSIONS ARE AVAILABLE. SUFFIX DESIGNATION DETERMINES NUMBER OF LEADS, i.e. KSD101-1 (1 LEAD)
* COMMON WITH TAB
** LEAD DIAMETER - .002

43
.080
.100 TYP
.300
.285
2.900
2.760
.180
.170
ALL LEADS .021 .019 TYP
.500
.485
1.10 MIN
.450
.440
CATHODE END
ALL DIMEN. IN INCHES AND ARE REFERENCE UNLESS TOLERANCED

48
DIMENSIONS WITHIN JEDEC OUTLINE DO-18
WHITE DOT INDICATES CATHODE
.022 MAX
.018 MIN
.060 MAX
.500 MIN
.100 MAX
.0035 MAX
.0025 MIN
EPOXY
ALL DIMENSIONS IN INCHES AND ARE REFERENCE UNLESS TOLERANCED

50
.090 MAX.
.020 ±.001
.040 MAX
.005
1.000 +.030 −.000
.095 MAX.
.110 MAX.
ALL DIMEN. IN INCHES AND ARE REFERENCE UNLESS TOLERANCED.

47
.090 MAX.
.020 ±.001
.040 MAX
.005
1.000 +.030 −.000
.095 MAX.
.110 MAX.
ALL DIMEN. IN INCHES AND ARE REFERENCE UNLESS TOLERANCED.
49
.032 MAX.
.065 DIA. MAX.
.500 MIN
.035 MAX.
.0035
.0025
.022
.018
CATHODE INDICATOR
1. ALL DIMENSIONS ARE IN INCHES AND REFERENCE UNLESS TOLERANCED.
2. UNIT WILL BE SUPPLIED WITH LEADS WHEN SPECIFIED. WHEN LEADS ARE SUPPLIED, THE DIMENSIONS ARE WITHIN JEDEC DO-20 OUTLINE.

REGISTERED JEDEC TRANSISTOR TYPES

For Explanation of Abbreviations, See Page 642.

JEDEC No.	Type	Use	MAXIMUM RATINGS: Pc mw @ 25°C	BVce BVcb*	Ic ma	Tj °C	ELECTRICAL PARAMETERS: MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ Vcb	Closest GE	Dwg. No.
2N22	Pt		120	−100	−20	55	1.9α							
2N23	Pt		80	−50	−40	55	1.9α							
2N24	Pt		120	−30	−25	50	2.2α							
2N25	Pt		200	−50	−30	60	2.5α							
2N26	Pt		90	−30	−40	55								
2N27	NPN		50	35*	100	85	100		1					
2N28	NPN		50	30*	100	85	100		.5					
2N29	NPN		50	35*	30	85	100		1		15	30		
2N30	Pt	Obsolete	100	30	7	40	2.2α		2T	17T				
2N31	Pt	Obsolete	100	30	7	40	2.2α		2T		150	25		
2N32	Pt	Obsolete	50	−40	−8	40	2.2α		2.7	21T				
2N32A	Pt	Obsolete	50	−40	−8	40	2.2α		2.7	21T				
2N33	Pt	Obsolete	30	−8.5	−7	40								
2N34	PNP	Obsolete	50	−25	−8	50	40		.6	40T			2N190	23
2N34A	PNP	Obsolete	50	−25	−8	50	40		.6	40T			2N190	23
2N35	NPN		50	25	8	50	40		.8	40T			2N169	22
2N36	PNP		50	−20	−8	50	45T			40T			2N191	23
2N37	PNP		50	−20	−8	50	30T			36T			2N190	23
2N38	PNP		50	−20	−8	50	15T			32T			2N189	23
2N38A	PNP		50	−20	−8	50	18T			34	−12	−3	2N189	23
2N41	PNP		50	−25	−15	50	40T			40T	−10	−12	2N190	23
2N43	PNP	AF	240	−30	−300	100	30	1	.5		−16	−45	2N43, 2N525	23, 24
2N43A	PNP	AF	240	−30	−300	100	30	1	.15		−16	−45	2N43A, 2N525	23, 24
2N44	PNP	AF	240	−30	−300	100	25T	1	.5		−16	−45	2N44, 2N524	23, 24
2N45	PNP	Obsolete	155	−25	−10	100	25T		.5	34	−16	−45	2N44	23
2N46	PNP		50	−25	−15	50	40T			4T	−10	−12	2N1414	24
2N47	PNP		50	−35*	−20	65	.975α				−5	−12	2N1414	24
2N48	PNP		50	−35*	−20	65	.970α				−5	−12	2N1414	24
2N49	PNP		50	−35*	−20	65	.975				−5	−12	2N1414	24
2N50	Pt		50	−15	−1	50	2α		3T					
2N51	Pt		100	−50	−8	50	2.2α				−350	−7		
2N52	Pt		120	−50	−8	50								
2N53	Pt			−50	−8									
2N54	PNP		200	−45	−10	60	.95α			40T			2N1098 16V	24
2N55	PNP		200	−45	−10	60	.92α			39T			2N1097 16V	24
2N56	PNP		200	−45	−10	60	.90α			38T			2N320	3
2N59	PNP		180	−25*	−200	85	90T*	−100		35T	−15	−20	2N1415	24
2N59A	PNP		180	−40*	−200	85	90T*	−100		35T	−15	−20	2N1415	24
2N59B	PNP		180	−50*	−200	85	90T*	−100		35T	−15	−20		

JEDEC No.	Type	Use	MAXIMUM RATINGS: Pc mw @ 25°C	BVce BVcb*	Ic ma	Tj °C	ELECTRICAL PARAMETERS: MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ Vcb	Closest GE	Dwg. No.
2N59C	PNP		180	−60*	−200	85	90T*	−100		35T	−15	−20		
2N60	PNP		180	−25*	−200	85	65T*	−100		35T	−15	−20	2N1415	24
2N60A	PNP		180	−40*	−200	85	65T*	−100		35T	−15	−20	2N1415	24
2N60B	PNP		180	−50*	−200	85	65T*	−100		35T	−15	−20	2N1925	24
2N60C	PNP		180	−60*	−200	85	65T*	100		35T	−15	−20	2N1926	24
2N61	PNP		180	−25*	−200	85	45T*	100		35T	−15	−20	2N1415	24
2N61A	PNP		180	−40*	−200	85	45T*	100		35T	−15	−20	2N1415	24
2N61B	PNP		180	−50*	−200	85	45T*	100		35T	−15	−20	2N1924	24
2N61C	PNP		180	−60*	−200	85	45T*	100		35T	−15	−20	2N1924	24
2N62	PNP		50	−35*	−20		.975αT							
2N63	PNP		100	−22	−10	85	22T	1		39T	−6	−6	2N1924	24
2N64	PNP		100	−15	−10	85	45T	1		41T	−6	−6	2N1415	24
2N65	PNP		100	−12	−10	85	90T	1		92T	−6	−6	2N324	3
2N66	PNP		1W	−40	.8A	80			.2		−300	−40		
2N67	PNP		2W	−25*	−1.5A	70				23T				
2N68	PNP		2W	−25*	−1.5A					23	−150 ma			
2N71	PNP		1W	−50	−250	60			.25	20				
2N72	Pt		50	−40	−20	55			2.5					
2N73	PNP		200	−50									2N1614	23
2N74	PNP		200	−50									2N1614	23
2N75	PNP		200	−20									2N1614	23
2N76	PNP	Obsolete	50	−20*	−10	60	.90α		1.0	34	−10	−20	2N322	3
2N77	PNP			−25*	−15	85	55		.70	44T	−10	−12	2N324	3
2N78	NPN	RF/IF	65	15	20	85	45*	1	5	27	3	15	2N78	22
2N78A	NPN	RF/IF	65	20	20	85	45*	1	5	29	3	15	2N78A	22
2N79	PNP		35	−30	−50		46		.7	44			2N321, 2N323	3, 3
2N80	PNP		50	−25	−8	100	80T				−30	−10	2N508, 2N1175	24, 24
2N81	PNP	Obsolete	50	−20	−15	100	20	1			−16	−30	2N1098	24
2N82	PNP		35 at 71° C	−20	−15	100	20	1			−16	−30	2N1098	24
2N94	NPN		30	20	5	75	40T	.5	3T	25T	3	10	2N169A	22
2N94A	NPN		30	20	5	75	40T	.5	6T	25T	3	10	2N169A	22
2N95	NPN		2.5W	25*	1.5	70	40		.4T	23T				
2N96	PNP		50	−30	−20	55	35		.5				2N1414	24
2N97	NPN		50	30	10	75	.85α		.5	38T	10	4.5	2N169 15V	22
2N97A	NPN		50	40	10	85	.85α		.5	38T	5	30	2N169A 25V	22
2N98	NPN		50	40	10	75	.95α		.8	47T	10	4.5	2N169A 25V	22
2N98A	NPN		50	40	10	85	.96α		.8	47T	10	4.5	2N169A 25V	22
2N99	NPN		50	40	10	75	.95α		2.0	47T	10	4.5	2N169A 25V	22
2N100	NPN		25	25	5	50	.99α		2.5	53T	10	4.5	2N170 6V	22
2N101	PNP		1W	−25*	−1.5	70				23T				
2N102	NPN		1W	25*	1.5	70				23T				
2N103	NPN		50	35	10	75	.60α		.75T	33T	50	35		

JEDEC No.	Type	Use	MAXIMUM RATINGS Pc mw @ 25°C	BVce BVcb*	Ic ma	Tj°C	ELECTRICAL PARAMETERS MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ Vcb	Closest GE	Dwg. No.
2N104	PNP		150	−30	−50	85	44		.7	33T	−10	−12	2N1415, 2N1414	24, 24
2N105	PNP		35	−25	−15	85	55	.7	.75	42	−5	−12	2N1415	24
2N106	PNP		100	−6	−10	85	25		.8	28	−12	−6	2N1097, 2N1098	24, 24
2N107	PNP	AF	50	−6	−10	60	20		.6		−10	−12	2N107, 2N1098	23, 24
2N108	PNP		50	−20	−15								2N322	3
2N109	PNP		150	−25	−70	85	75*			30T			2N1175	24
2N110	Pt		200	−50*	−50	85	32		1.5					
2N111	PNP		150	−15	200	85	15		3T	33T	−5	−12	2N394	24
2N111A	PNP		150	−15	−200	85	15		3T	33T	−5	−12	2N394	24
2N112	PNP		150	−15	−200	85	15		5T	35T	−5	−12	2N394	24
2N112A	PNP		150	−15	−200	85	15		5T	35T	−5	−12	2N394	24
2N113	PNP		100	−6	−5	85	45T		10T	33T			2N394	24
2N114	PNP		100	−6	−5	85	65T		20T				2N394	24
2N117	NPN		150	30*	25	150	.90α	1	1		10	30	2N332, 2N334	3, 3
2N118	NPN		150	30*	25	150	.95α	1	2		10	30	2N333, 2N335	3, 3
2N118A	NPN-G		150	45	25	150J	54T		7.50		10		2N335	3
2N119	NPN		150	30*	25	150	.974α	1	2		10	30	2N335, 2N336	3, 3
2N120	NPN		150	45*	25	175	.987α	1	7T		2	30		
2N122	NPN		8.75W		140A	150	3	100			10 ma	50		
2N123	PNP	Sw	150	−15	−125	85	30*	−10	5		−6	−20	2N123	23
2N124	NPN		50	10*	8	75	12*	5	3		2	5	2N293	22
2N125	NPN		50	10*	8	75	24*	5	5		2	5	2N167	22
2N126	NPN		50	10*	8	75	48*	5	5		2	5	2N167, 2N169	22, 22
2N127	NPN		50	10*	8	75	100*	5	5		2	5	2N167, 2N169	22, 22
2N128	PNP		30	−4.5	−5	85	.95	.5	45 f_{max}		−3	−5		
2N129	PNP		30	−4.5	−5	85	.92	.5	30 f_{max}		−3	−5		
2N130	PNP		85	−22	−10	85	22T			39T			2N1413, 2N1924	24, 24
2N130A	PNP		100	−40	−100	85	14	1	.7T	40T	−15	−20	2N1413, 2N1924	24, 24
2N131	PNP		85	−15	−10	85	45T			41T			2N1413, 2N1415	24, 24
2N131A	PNP		100	−30	−100	85	27	1	.8T	42T	−15	−20	2N1413, 2N1924	24, 24
2N132	PNP		85	−12	−10	85	90T			42T			2N1175	24
2N132A	PNP		100	−20	−100	85	56	1	1T	44T	−15	−20	2N1415	24
2N133	PNP		85	−15	−10	85	25			36T	−12	−15	2N1414	22
2N133A	PNP		100	−20	−100	85	50T	1	.8T	38T	−15	−20	2N1414, 2N1175	22, 24
2N135	PNP	Obsolete	100	−12	−50	85	20T		4.5T	29T			2N394	24
2N136	PNP	Obsolete	100	−12	−50	85	40T		6.5T	31T			2N394	24
2N137	PNP	Obsolete	100	−6	−50	85	60T		10T	33T			2N394	24
2N138	PNP		50	−12	−20	50	140T			30T			2N508	24
2N138A	PNP		150	−30	−100	85				29T			2N1098	24
2N138B	PNP		100	−30	−100	85				29T			2N1098	24
2N139	PNP		80	−16	−15	85	48	1	6.8	30	−6	−12	2N394	24
2N140	PNP		35	−16	−15	85	45	.4	7	27	−6	−12	2N394, 2N395	24, 24

JEDEC No.	Type	Use	MAXIMUM RATINGS Pc mw @ 25°C	BVce BVcb*	Ic ma	Tj°C	ELECTRICAL PARAMETERS MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ Vcb	Closest GE	Dwg. No.
2N141	PNP		4W	−30	−.8A	65	.975αT	50	.4T	18T	−100	−20		
2N142	NPN		4W	30	.8A	65	.975αT	−50	.4T	26T	−100	20		
2N143	PNP		4W	−30	−.8A	65	.975αT	50	.4T	26T	−100	−20		
2N144	NPN		4W	30	.8A	65	.975αT	50	.4T	26T	100	20		
2N145	NPN		65	20	5	75	30			30	3	9	2N293, 2N1121	22, 22
2N146	NPN		65	20	5	75	33			33	3	9	2N1121	22
2N147	NPN		65	20	5	75	36			36	3	9	2N1121	22
2N148	NPN		65	16	5	75				32	3	12	2N169	22
2N148A	NPN		65	32	5	75				32	3	12	2N169	22
2N149	NPN		65	16	5	75				35	3	12	2N169	22
2N149A	NPN		65	32	5	75				35	3	12	2N169	22
2N150	NPN		65	16	5	75				38	3	12	2N169	22
2N150A	NPN		65	32	5	75				38	3	12	2N169	22
2N155	PNP		8.5W	−30*	−3A	85			.15T	30	1 ma	−30		
2N156	PNP		8.5W	−30*	−3A	85	24*	.5A	.15T	33	1 ma	−30		
2N157	PNP		8.5W	−60*	−3A	85	20*	.5A	.1		1 ma	−60		
2N157A	PNP		8.5W	−90*	−3A	85	20*	.5A	.1		1 ma	−90		
2N158	PNP		8.5W	−60*	−3A	85	21*	.5A	.15T	37	1 ma	−60		
2N158A	PNP		8.5W	−80*	−3A	85	21*	.5A	.15		1 ma	−80		
2N160	NPN		150	40*	25	150	.9α	−1	4T	34T	5	40	2N332, 2N1276	3, 3
2N160A	NPN		150	40*	25	150	.9α	−1	4T	34T	5	40	2N332	3
2N161	NPN		150	40*	25	150	.95α	−1	5T	37T	5	40	2N333, 2N1277	3, 3
2N161A	NPN		150	40*	25	150	.95α	−1	5T	37T	5	40	2N333	3
2N162	NPN		150	40*	25	150	.95α	−1	8	38T	5	40	2N335, 2N1278	3, 3
2N162A	NPN		150	40*	25	150	.95α	−1	8	38T	5	40	2N335	3
2N163	NPN		150	40*	25	150	.975α	−1	6T	40T	5	40	2N335, 2N1278	3, 3
2N163A	NPN		150	40*	25	150	.975α	−1	6T	40T	5	40	2N335	3
2N164A	NPN		65	1.0*	20	85J	40T		8.00	30			2N1121	22
2N165	PNP-M		55	1.0*	20	75J	72T		5.00	26			2N169	22
2N166	NPN	Obsolete	25	6	20	50	32T	1	5T	24T	5	5	2N170	22
2N167	NPN	Sw	65	30	75	85	17*	8	5		1.5	15	2N167	22
2N167A	NPN	Sw	65	30	75	85	17*	8	5		1.5	15	2N167A	22
2N168	NPN	IF	55	15	20	75	20T	1	6T	28	5	15	2N293	22
2N168A	NPN	Obsolete	65	15	20	85	23*	1	5	28	5	15	2N1086, 2N1121	22, 22
2N169	NPN	IF	65	15	20	85	34*	1	8T	27	5	15	2N169	22
2N169A	NPN	AF	65	15	20	85	34*	1	8T	27	5	15	2N169A	22
2N170	NPN	IF	25	6	20	50	.95αT	1	4T	22T	5	5	2N170	22
2N172	NPN		65	16	5	75				22	3	9	2N293	22
2N173	PNP		40W	−60	−13A	95	85T*	1A	.6T	40T	−.5 ma	−40		
2N174	PNP		40W	−80	−13A	95	40T*	1A	.2T	39T	−10 ma	−60		
2N174A	PNP		85W	−80	−15A	95	40*	1.2A	.1		−8 ma	−80		
2N175	PNP		20	−10	−2	85	65	.5	2	43T	−12	−25	2N1175A	24

JEDEC No.	Type	Use	MAXIMUM RATINGS Pc mw @ 25°C	BVCE BVCB*	Ic ma	TJ°C	ELECTRICAL PARAMETERS MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE	Dwg. No.
2N176	PNP		3W	−12	−600	80				25T				
2N178	PNP		3W	−12	−600	80				29T				
2N179	PNP			−20	−60	88				32T				
2N180	PNP		150	−30	−25	75	60T		.7	37T			2N1415	24
2N181	PNP		250	−30	−38	75	60T		.7	34T			2N526	24
2N182	NPN		100	25*	10	85	25T*		2.5		3T	10		
2N183	NPN		100	25*	10	85	50T*		5		3T	10		
2N184	NPN		100	25*	10	85	100T*		10		3T	10		
2N185	PNP		150	−20	−150	75	35	−100		26	15	−20	2N323	3, 3
2N186	PNP	Obsolete	100	−25	200	85	24T*	−100	.8T	28	−16	−25	2N186A, 2N1413	23, 24
2N186A	PNP	AF Out	200	−25	200	85	24T*	−100	.8T	28	−16	−25	2N186A	23
2N187	PNP	Obsolete	100	−25	200	85	36T*	−100	1T	30	−16	−25	2N187A, 2N1413	23, 24
2N187A	PNP	AF Out	200	−25	200	85	36T*	−100	1T	30	−16	−25	2N187A	23
2N188	PNP	Obsolete	100	−25	−200	85	54T*	100	1.2T	32	−16	−25	2N188A, 2N1413	23, 24
2N188A	PNP	AF Out	200	−25	−200	85	54T*	100	1.2T	32	−16	−25	2N188A	23
2N189	PNP	AF	75	−25	−50	85	24T*	1	.8T	37	−16	−25	2N189, 2N1413	23, 24
2N190	PNP	AF	75	−25	−50	85	36T*	1	1.0T	39	−16	−25	2N190, 2N1414	23, 24
2N191	PNP	AF	75	−25	−50	85	54T*	1	1.2T	41	−16	−25	2N191, 2N1415	23, 24
2N192	PNP	AF	75	−25	−50	85	75T*	1	1.5T	43	−16	−25	2N192, 2N1175	23, 24
2N193	NPN		50	15		75	3.8	1	2		40	15	2N1086	22
2N194	NPN		50	15		75	4.8	1	2	15T	40	15	2N1086	22
2N194A	NPN		50	20	100	75	5	1	2	20	50	18	2N1087	22
2N206	PNP		75	−30	−50	85	47T		.8				2N1414	24
2N207	PNP		50	−12	−20	65	35	1	2T		−15	−12	2N1415, 2N323	24, 3
2N207A	PNP		50	−12	−20	65	35	1	2T		−15	−12	2N1415, 2N1175A	24, 24
2N207B	PNP		50	−12	−20	65	35	1	2T		−15	−12	2N1415, 2N1175A	24, 24
2N211	NPN		50	10	50	75	3.8	1	2		20	10	2N293, 2N1086	22, 22
2N212	NPN		50	10	50	75	7	1	4	22T	20	10	2N293, 2N1086	22, 22
2N213	NPN		50	25	100	75	70	1		39	200	40	2N169A	22
2N213A	NPN		150	25	100	85	100	1	10 Kc	38	50	20		
2N214	NPN		125	25	75	75	50	35	.6	26	200	40		
2N215	PNP		150	−30	−50	85	44		.7	33T	−10	−12	2N1415	24
2N216	NPN		50	15	50	75	3.5	1	2	26T	40	15	2N292, 2N1086	22, 22
2N217	PNP		150	−25	−70	85	75*			30T			2N321, 2N396	3, 24
2N218	PNP		80	−16	−15	85	48	1	6.8	30	−6	−12	2N394	24
2N219	PNP		80	−16	−15	85	75	.4	10	32	−6	−12	2N394	24
2N220	PNP		50	−10	−2	85	65		.8	43			2N323, 2N1175A	3, 24
2N223	PNP		100	−18	−150	65	39	−2	.6T		−20	−9	2N323	3
2N224	PNP		250	−25*	150	75	60*	−100	.5T		−25	−12	2N321, 2N1175	3, 24
2N225	PNP		250	−25*	150	75	60*	−100	.5T		−25	−12	2N321, 2N1175	3, 24
2N226	PNP		250	−30*	150	75	35*	−100	.4T		−25	−30	2N321, 2N1415	3, 24
2N227	PNP		250	−30*	150	75	35*	−100	.4T		−25	−30	2N321, 2N1415	3, 24

JEDEC No.	Type	Use	MAXIMUM RATINGS Pc mw @ 25°C	BVCE BVCB*	Ic ma	TJ°C	ELECTRICAL PARAMETERS MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE	Dwg. No.
2N228	NPN		50	25	50	75	50	35	.6	23	200	40	2N169	22
2N229	NPN		50	12	40	75	.9α	1	.55		200	5	2N169	22
2N231	PNP		9	−4.5	−3	55	19	−.5	20 f_{os}		−3	−5		
2N232	PNP		9	−4.5	−3	55	9	−.5	30 f_{os}		−6	−5		
2N233	NPN		50	10	50	75	3.0	1			100	10	2N292	22
2N233A	NPN		50	10	50	75	3.5	1			150	15	2N292	22
2N234	PNP		25W	−30	−3A	90			8 Kc	25	−1 ma T	−25		
2N234A	PNP		25W	−30	−3A	90			8 Kc	25	−1 ma T	−25		
2N235	PNP		25W	−40	−3A	90			7 Kc	30				
2N235A	PNP		25W	−40	−3A	90			7 Kc	30				
2N235B	PNP			40	3.0A	85					300	3		
2N236	PNP		25W	−40	−3A	95			6 Kc	30	−1 ma	−25		
2N236A	PNP		25W	−40	−3A	95			6 Kc	30	−1 ma	−25		
2N236B	PNP			40	3.0A	95					300	2		
2N237	PNP		150	45	20	85	50T		.50		10		2N525	24
2N238	PNP		50	−20		75				37	−20	−20	2N323	3
2N240	PNP		10	−6	−15		16	−.5	30 f_{os}		−3	−5		
2N241	PNP	Obsolete	100	−25	200	85	73T*	100	1.3T	35T	−16	−25	2N241A	23
2N241A	PNP	AF Out	200	−25	200	85	73T*	100	1.3T	35T	−16	−25	2N241A, 2N1415	23, 24
2N242	PNP		20W	−45	−2A	85			5 Kc	30	−5 ma	−45		
2N243	NPN		750	60*	60	150	.9	−5		30	1	30		
2N244	NPN		750	60*	60	150	.961	−5		30	1	30		
2N247	PNP		80	−12	−10	85	60		30	37	−20	−12		
2N248	PNP		30	−25	−5	85	20T*	.5	50T		−10	−12		
2N249	PNP		350	−25	−200	85	30	−100			−25	−25		
2N250	PNP		12W	−30	−2A	80	30*	−.5A			−1 ma	−30		
2N251	PNP		12W	−60	−2A	80	30*	−.5A		30	−2 ma	−60		
2N252	PNP		30	−16	−5	55				28	−10	−12		
2N253	NPN		65	12	5	75				32	3	9	2N293, 2N1121	22, 22
2N254	NPN		65	20	5	75					3	9	2N293, 2N1121	22, 22
2N255	PNP		1.5W	−15*	−3	85			.2T	19				
2N255A	PNP		20W	15	4A	85	25*	450			5 ma	15		
2N256	PNP		1.5W	−30*	−3	85			.2T	22				
2N256A	PNP		20W	25	4A	85	25*	450			5 ma	−25		
2N257	PNP		2W	−40*		85	55T	.5A	7 Kc	30	−2 ma	−40		
2N260	PNP		200	−10*	−50	150	16T	1	1.8T	38T	.001T	−6	2N332, 2N1276	3, 3
2N260A	PNP		200	−30*	−50	150	16T	1	1.8T	38T	.001T	−6	2N332	3
2N261	PNP		200	−75*	−50	150	10T	1	1.8T	36T	.001T	−6	2N332	3
2N262	PNP		200	−10*	−50	150	20T	1	6T	40T	.001T	−6	2N333	3
2N262A	PNP		200	−30*	−50	150	20T	1	6T	40T	.001T	−6	2N333	3
2N265	PNP		75	−25	−50	85	110T*	1	1.5T	45	−16	−25	2N265, 2N508	23, 24
2N267	PNP		80	−12	−10	85	60		30	37	−20	−12		

JEDEC No.	Type	Use	MAXIMUM RATINGS P_C mw @ 25°C	BV_{CE} BV_{CB}*	I_C ma	T_J°C	ELECTRICAL PARAMETERS MIN. h_{fe}-h_{FE}*	@ I_C ma	MIN. f_{hfb} mc	MIN. G_e db	MAX. I_{CO} (μa)	@ V_{CB}	Closest GE	Dwg. No.
2N268	PNP		2W	−80*		85			6 Kc	28	−2 ma	−80		
2N268A	PNP		2W	−60		90	20*	2A			−2 ma	−80		
2N269	PNP		120	−24	−100	85	35		4		−5	−12	2N404	24
2N270	PNP		150	−25	−75	85	70	150		35	−10	−25	2N321, 2N1415	3, 24
2N271	PNP		150	−10	−200	85	45T	1	10T	29T	−5	−12	2N394	24
2N271A	PNP		150	−10	−200	85	45T	1	10T	39T	−5	−12	2N394	24
2N272	PNP		150	−24	−100	85	60		1T	12T	−6T	−20	2N324	3
2N273	PNP		150	−30	−100	85	10	50		29	−6T	−20	2N1098	24
2N274	PNP		80	−12	−10	85	60T	1	30T	45T	−20	−12		
2N277	PNP		55W	−40	12A	95	85T	1.2A	.5T	34T	−.5 ma T	−30		
2N278	PNP		55W	−50	12A	95	85T	1.2A	.5T	34T	−.5 ma T	−20		
2N281	PNP		165	32	250	75J	70T*		.90		10		2N1415	24
2N285	PNP		25W	−40	3A	95			6 Kc	38	−1 ma	−25		
2N285A	PNP		25W	−40	3A	95			6 Kc	38	−1 ma	−25		
2N290	PNP		55W	−70	−12A	95	72T*	1.2A	.4T	37T	−1 ma T	−60		
2N291	PNP		180	−25	−200	85	30*	100		31	−25	−25	2N320, 2N1414	3, 24
2N292	NPN	IF	65	15	−20	85	8	1	5T	25.5	5	15	2N292	22
2N293	NPN	IF	65	15	−20	85	8	1	8T	28	5	15	2N293	22
2N297	PNP		35W	−50	−5A	95	40*	.5	5 Kc		3 ma	−60		
2N297A	PNP		35W	−50	−5A	95	40*	.5	5 Kc		3 ma	−60		
2N299	PNP		20	−4.5	−5	85			90 f_{os}	20	−3	−5		
2N300	PNP		20	−4.5	−5	85	11	.5	85 f_{os}		−3	−5		
2N301	PNP		11W	−20	−1.5A	91	70T*	1A		33T	−3 ma	−30		
2N301A	PNP		11W	−30	−1.5A	91	70T*	1A		33T	−3 ma	−30		
2N302	PNP		150	−10	−200	85	45T		7		−1T	−.12	2N186A	23
2N303	PNP		150	−10	−200	85	75T		14		−1T	−.12	2N186A	23
2N306	NPN		50	15		75	25	1	.6	34	50	20	2N292	22
2N307	PNP		10W	−35	−1A	75	20	200	3 Kc		15 ma	−35		
2N307A	PNP		17W	−35	−2A	75	20	200	3.5 Kc	22	7 ma	−35		
2N308	PNP		30	−20	−5	55				39	−10	−9		
2N309	PNP		30	−20	−5	55				41	−10	−9		
2N310	PNP		30	−30	−5	55	28T			37T	−10	−9		
2N311	PNP		75	−15		85	25				−60	−15	2N123	23
2N312	NPN		75	15		85	25				60	15	2N167	22
2N313	NPN	Obsolete	65	15	20	85	25		5	36 max			Use 2N292	22
2N314	NPN	Obsolete	65	15	20	85	25		8	39 max			Use 2N293	22
2N315	PNP		100	−15	−200	85	15	100	5T		−2	−5	2N396	24
2N315A	PNP-A		150	30		100S	35T*		5.00		25		2N396	24
2N316	PNP		100	−10	−200	85	20	200	12T		−2	−5	2N397	24
2N316A	PNP-A		150	30		100S	35T*		12.0		25		2N397	24
2N317	PNP		100	−6	−200	85	20	400	20T		−2	−5		
2N318	PNP	Photo	50	−12	−20				.75T					

JEDEC No.	Type	Use	MAXIMUM RATINGS P_C mw @ 25°C	BV_{CE} BV_{CB}*	I_C ma	T_J°C	ELECTRICAL PARAMETERS MIN. h_{fe}-h_{FE}*	@ I_C ma	MIN. f_{hfb} mc	MIN. G_e db	MAX. I_{CO} (μa)	@ V_{CB}	Closest GE	Dwg. No.
2N319	PNP	AF	225	−20	−200	85	34T*	−20	2T		−16	−25	2N319, 2N1413	3, 24
2N320	PNP	AF	225	−20	−200	85	50T*	−20	2.5T		−16	−25	2N320, 2N1414	3, 24
2N321	PNP	AF	225	−20	−200	85	80T*	−20	3.0T		−16	−25	2N321, 2N1415	3, 24
2N322	PNP	AF	140	−16	−100	60	45T	−20	2T		−16	−16	2N322	3
2N323	PNP	AF	140	−16	−100	60	68T	−20	2.5T		−16	−16	2N323	3
2N324	PNP	AF	140	−16	−100	60	85T	−20	3.0T		−16	−16	2N324	3
2N325	PNP		12W	−35	−2A	85	30*	−500	.15		−500	−30		
2N326	NPN		7W	35	2A	85	30*	500	.15		500	30		
2N327	PNP		335	−50*	−100	160	9	.1	.3T	30	−.1	−30		
2N327A	PNP		350	−50*	−100	160	9*	1	.2T		−.1	−30		
2N328	PNP		335	−35*	−100	160	18	1	.35T	32	−.1	−30		
2N328A	PNP		350	−50*	−100	160	18*	1	.3T		−.1	−30		
2N329	PNP		335	−30*	−100	160	36	1	.6T	34	−.1	−30		
2N329A	PNP		350	−50*	−100	160	36*	1	.5T		−.1	−30		
2N330	PNP		335	−45*	−50	160	9	1	.5	30	−.1	−30		
2N330A	PNP		350	−50*	−100	160	25T	1	.5	34T	−.1	−30		
2N331	PNP		200	−30*	−200	85	50T			44T	−16	−30	2N1415	24
2N332	NPN	Si AF	150	45*	25	200	9	1	10T	14T	2	30	2N332	3
2N332A	NPN	Si AF	500	45	25	175	9		2.5	11	.500	30	2N332A	3
2N333	NPN	Si AF	150	45*	25	200	18	1	12*	14T	2	30	2N333	3
2N333A	NPN	Si AF	500	45	25	175	18		2.5	11	.500	30	2N333A	3
2N334	NPN	Si AF	150	45*	25	200	18	1	8	13T	2	30	2N334	3
2N334A	NPN	Si AF	500	45	25	175	18		8.0	12	.500	30	2N334A	3
2N335	NPN	Si AF	150	45*	25	200	37	1	14*	13T	2	30	2N335	3
2N335A	NPN	Si AF	500	45	25	175	37		2.5	12	.500	30	2N335	3
2N335B	NPN	Si AF	500	60	25	175	37		2.5	12T	.500	30	2N335B	3
2N336	NPN	Si AF	150	45*	25	200	76	1	15*	12T	2	30	2N336	3
2N336A	NPN	Si AF	500	45	25	175	76		2.5	12	.500	30	2N336A	3
2N337	NPN	Si AF	125	45*	20	200	19	1	10		1	20	2N337	3
2N337A	NPN-G		500	45	20	200S	35T		30.0		.10		2N337A	3
2N338	NPN	Si AF	125	45*	20	200	39	1	20		1	20	2N338	3
2N338A	NPN-G		500	45	20	200S	75T		45.0		.10		2N338A	3
2N339	NPN		1W	55*	60	150	.9α	−5		30	1	30	2N656A	24
2N339A	NPN		1000	60		200S	53T				1.0		2N656A	24
2N340	NPN		1W	85*	60	150	.9α	−5		30	1	30	2N657A	34
2N340A	NPN		1000	85		150J	50T			30	1.0		2N657A	24
2N341	NPN		1W	125*	60	150	.9α	−5		30	1	30	2N657A	24
2N341A	NPN		1000	125		200S	53T			30	1.0		2N657A	24
2N342	NPN		1W	60*	60	150	.9α	−5		30	1	30	2N656A	24
2N342A	NPN-G		1000	85	60	150J	20T			30	1.0		2N657A	24
2N342B	GD		1000	85	60	150J	21T		6.00		50		2N335B, 2N657A	3, 24
2N343	NPN		1W	60*	60	150	.966α	−5		30	1	30	2N656A	24

JEDEC No.	Type	Use	MAXIMUM RATINGS P_C mw @ 25°C	BV_{CE} BV_{CB}*	I_C ma	T_J °C	ELECTRICAL PARAMETERS MIN. h_{fe}-h_{FE}*	@ I_C ma	MIN. f_{hfb} mc	MIN. Ge db	MAX. I_{CO} (μa)	@ V_{CB}	Closest GE	Dwg. No.
2N343B	GD		1000	65	60	150J	59T		6.00		100		2N335B, 2N656A	3, 24
2N344	PNP		40	−5	−5	85	11		30 f_{os}		−3	−5		
2N345	PNP		40	−5	−5	85	25		30 f_{os}		−3	−5		
2N346	PNP		40	−5	−5	85	10		60 f_{os}		−3	−5		
2N348	NPN-G		750	90	50	150J	24T		3.00	35	6.0		2N292	22
2N349	NPN-G		750	125	40	150J	19T		3.00	34	8.0		2N293	22
2N350	PNP		10W	−40*	−3A	90	20*	−700	5 Kc	30	−3 ma	−30		
2N351	PNP		10W	−40*	−3A	90	25*	−700	5 Kc	32	−3 ma	−30		
2N352	PNP		25W	−40	−2A	100	30	−1A	10 Kc	30	−5 ma	−1 @ 85°C		
2N353	PNP		30W	−40	−2A	100	40	−1A	7 Kc	30	−5 ma	−1 @ 85°C		
2N354	PNP		150	−25*	−50	140	9	1	8 f_{os}		−.1	−10		
2N355	PNP		150	−10*	−50	140	9	1	8 f_{os}		−.1	−10		
2N356	NPN		120	18	100	85	20	100	3T		5	5		
2N356A	NPN-A		150	30		100S	35T*		3.00		25			
2N357	NPN		120	15	100	85	20	200	6T		5	5		
2N357A	NPN-A		150	30		100S	40T*		6.00		25			
2N358	NPN		120	12	100	85	20	300	9T		5	5		
2N358A	NPN-A		150	30		100S	40T*		9.00		25			
2N359	PNP-A		150	20	400	85	300T		1.50	40	10		2N508	24
2N360	PNP-A		150		400	85	150T		1.20	37	10		2N1415	24
2N361	PNP-A		150	20	400	85	75T		1.00	34	10		2N1413	24
2N362	PNP-A		150	18	100	85	90T		2.00	42	15		2N324	3
2N363	PNP-A		150	32	100	85	50T		1.50	39	15		2N1414	24
2N364	NPN		150	30*	50	85	9	−1	1		10	30	2N1694	24
2N365	NPN		150	30*	50	85	19	−1	1		10	30	2N1694	24
2N366	NPN		150	30*	50	85	49	−1	1		10	30		
2N367	NPN		100	−30*	−50	75	9	1	.3		−30	−30	2N1413	24
2N368	PNP		150	−30*	−50	75	19	1	.4		−20	−30	2N1413	24
2N369	PNP		150	−30*	−50	75	49	1	.5		−20	−30	2N1415	24
2N370	PNP		80	−24*	−20	85	60T	1	30T	31M	−10	−12		
2N371	PNP		80	−24*	−20	85	.984T	1	30T	17.6M	−10	−12		
2N372	PNP		80	−24*	−20	85	60T	1	30T	12.5M	−10	−12		
2N373	PNP		80	−24*	−10	85	60T	1	30T	40T	−16	−12		
2N374	PNP		80	−24*	−10	85	60T	1	30T	40T	−16	−12		
2N375	PNP		45W	−60	−3A	95	35	1A	7 Kc		−3 ma	−60		
2N376	PNP		10W	−40*	−3A	90	60T	1A	5 Kc	35T				
2N377	NPN	Sw	150	20	200	100	20*	30	6T		5	1		
2N377A	NPN		150	40	200	100	20*	200	6T		40	40		
2N378	PNP		50W	−40	−5A	100	15*	2A	5 Kc		−500	−25		
2N379	PNP		50W	−80	−5A	100	20*	2A	5 Kc		−500	−25		
2N380	PNP		50W	−60	−5A	100	30*	2A	7 Kc		−500	−25		
2N381	PNP		200	−25	−200	85	50T	20	1.2T	31T	−10T	−25	2N320, 2N1924	3, 24

JEDEC No.	Type	Use	MAXIMUM RATINGS P_C mw @ 25°C	BV_{CE} BV_{CB}*	I_C ma	T_J °C	ELECTRICAL PARAMETERS MIN. h_{fe}-h_{FE}*	@ I_C ma	MIN. f_{hfb} mc	MIN. Ge db	MAX. I_{CO} (μa)	@ V_{CB}	Closest GE	Dwg. No.
2N382	PNP		200	−25	−200	85	75T	20	1.5T	33T	−10T	−25	2N321	3
2N383	PNP		200	−25	−200	85	100T	20	1.8T	35T	−10T	−25	2N321, 2N1175	3, 24
2N384	PNP		120	−30	−10	85	60T	1.5	100T	15	−16	−12		
2N385	NPN		150	25	200	100	30*	30	4		35	25		
2N385A	NPN-A		150	40	200	100J	70T		8.00		40			
2N386	PNP		12.5W	−60	−3A	100	20	−2.5A	7 Kc		−5 ma	−60		
2N387	PNP		12.5W	−80	−3A	100	20	−2.5A	6 Kc		−5 ma	−80		
2N388	NPN	Sw	150	20	200	100	60*	30	5		10	25		
2N388A	NPN		150	40	200	100	30*	200	5		40	40		
2N389	NPN		85W	60		200	12	1A			10 ma	60 @ 100°C		
2N392	PNP		70W	−60*	−5A	95	60	3A	6 Kc		−8 ma	−60		
2N393	PNP		50	−6	−50	85	20*	−50	40 f_{os}		−5	−5		
2N394	PNP	Sw	150	−10	−200	85	20*	−10	4		−6	−10	2N394	24
2N394A	PNP-A		150	30	200	100S	70T*		7.00		6.0		2N394A	24
2N395	PNP	Sw	200	−15	−200	100	20*	−10	3		−6	−15	2N395	24
2N396	PNP	Sw	200	−20	−200	100	30*	−10	5		−6	−20	2N396	24
2N396A	PNP	Sw	200	20	200	100	30*	10	5		−6	−20	2N396A	24
2N397	PNP	Sw	200	−15	−200	100	40*	−10	10		−6	−15	2N397	24
2N398	PNP		50	−105	−110	85	20*	−5 ma			−14	−2.5	2N1614	23
2N398A	PNP		150	105		100J	20T		1.00				2N1924	24
2N399	PNP		25W	−40	−3A	90			8 Kc	33T	−1 ma	−25		
2N400	PNP		25W	−40	3.0A	95	1			40	2 ma	−25		
2N401	PNP		25W	−40	−3A	90			8 Kc	30T	−1 ma	−25		
2N402	PNP		180	−20	−150	85	.96αT	1	.6T	37T	−15	−20	2N320, 2N1413	3, 24
2N403	PNP		180	−20	−200	85	.97αT	1	.85T	32	−15	−20	2N319, 2N1413	3, 24
2N404	PNP	Sw	120	−24	−100	85			4		−5	−12	2N404	24
2N404A	PNP-A	RCPS	150	40	150	100			8.00		20		2N404A	24
2N405	PNP		150	−18	−35	85	35T*	1	.65T	43T	−14	−12	2N322	3
2N406	PNP		150	−18	−35	85	35T*	1	.65T	43T	−14	−12	2N322	3
2N407	PNP		150	−18	−70	85	65T*	−50		33T	−14	−12	2N323	3
2N408	PNP		150	−18	−70	85	65T*	−50		33T	−14	−12	2N323	3
2N409	PNP		80	−13	−15	85	.98αT	1	6.7T	38T	−10	−13	2N394	24
2N410	PNP		80	−13	−15	85	.98αT	1	6.7T	38T	−10	−13	2N394	24
2N411	PNP		80	−13	−15	85	75T	.6		32T	−10	−13	2N397	24
2N412	PNP		80	−13	−15	85	75T	.6		32T	−10	−13	2N397	24
2N413	PNP	IF Sw	150	−18	−200		30		6T		−5	−12	2N413	24
2N413A	PNP		150	−15	−200	85	30T	1	2.5T	33T	−5	−12	2N394	24
2N414	PNP	IF Sw	150	−15	−200		60		7T		−5	−12	2N414	24
2N414A	PNP		150	−15	−200	85	60T	1	7T	35T	−5	−12	2N394, 2N414	24
2N415	PNP		150	−10	−200	85	80T	1	10T	30T	−5	−12	2N394	24
2N415A	PNP		150	−10	−200	85	80T	1	10T	39T	−5	−12	2N394	24
2N416	PNP		150	−12	−200	85	80T	1	10T	20T	−5	−12	2N394	24

JEDEC No.	Type	Use	MAXIMUM RATINGS Pc mw @ 25°C	BVCE BVCB*	Ic ma	TJ°C	ELECTRICAL PARAMETERS MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE	Dwg. No.
2N417	PNP		150	−10	−200	85	140T	1	20T	27T	−5	−12	2N394	24
2N418	PNP		25W	80	5A	100	40*	4A	400 Kc		15 ma	−60		
2N420	PNP		25W	45	5A	100	40*	4A	400 Kc	10 m	10 ma	−25		
2N420A	PNP		25W	70	5A	100	40*	4A	400 Kc		15 ma	−60		
2N422	PNP		150	−20	−100	85	50T	1	.8T	38T	−15	−20	2N320, 2N1175A	3, 24
2N425	PNP		150	−20	−400	85	20*	1	2.5		−25	−30	2N394	24
2N426	PNP		150	−18	−400	85	30*	1	3		−25	−30	2N395	24
2N427	PNP		150	−15	−400	85	40*	1	5		−25	−30	2N396	24
2N428	PNP		150	−12	−400	85	60*	1	10		−25	−30	2N397	24
2N438	NPN		100	25		85	20*	50	2.5		10	25		
2N438A	NPN		150	25		85	20*	50	2.5		10	25		
2N439	NPN		100	20		85	30	50	5		10	25		
2N439A	NPN		150	20		85	30*	50	5		10	25		
2N440	NPN		100	15		85	40*	50	10		10	25		
2N440A	NPN		150	15		85	40*	50	10		10	25		
2N444	NPN		120	15		85	15T		.5T		2T	10		
2N444A	NPN-A		150	40		100S	30T		.50		25			
2N445	NPN		100	12		85	35T		2T		2T	10		
2N445A	NPN-A		150	30		100S	90T*		2.00		25			
2N446	NPN		100	10		85	60T		5T		2T	10		
2N446A	NPN-A		150	30		100S	150T*		5.00		25			
2N447	NPN		100	6		85	125T		9T		2T	10		
2N447A	NPN-A		150	30		100S	200T*		9.00		25			
2N448	NPN	IF	65	15	20	85	8*	1	5T	23	5	15	2N292	22
2N449	NPN	IF	65	15	20	85	34*	1	8T	24.5	5	15	2N293	22
2N450	PNP	Sw	150	−12	−125	85	30*	−10	5		−6	−12	2N450, 2N394A	23, 24
2N456	PNP		50	−40	5A	95	130T*	1A			−2 ma	−40		
2N457	PNP		50	−60	5A	95	130T*	1A			−2 ma	−60		
2N458	PNP		50	−80	5A	95	130T*	1A			−2 ma	−80		
2N459	PNP		50	−60	5A	100	20*	2A	5 Kc		100 ma	−60		
2N460	PNP		200	−45*	−400	100	.94α	1	1.2T	34T	−15	−45	2N524	24
2N461	PNP		200	−45*	−400	100	.97α	1	1.2T	37T	−15	−45	2N461	24
2N462	PNP		150	−40*	−200	75	20*	−200	.5		−35	−35	2N1614, 2N527	23, 24
2N463	PNP		37.5W	−60	5A	100	20*	−2A	4 mc		−300	−40		
2N464	PNP		150	−40	−100	85	14	1	.7T	40T	−15	−20	2N1614, 2N527	23, 24
2N465	PNP		150	−30	−100	85	27	1	.8T	42T	−15	−20	2N1414, 2N1924	24, 24
2N466	PNP		150	−20	−100	85	56	1	1T	44T	−15	−20	2N321, 2N1175	3, 24
2N467	PNP		150	−15	−100	85	112	1	1.2T	45T	−15	−20	2N508	24
2N469	PNP		50			75	10	1	1T		−50	−6		
2N470	NPN-GD		200	15		175A	16T						2N335	3
2N471	NPN-GD		200	30		175A	16T						2N335	3
2N471A	NPN-GD		200	30		175A	25T						2N335	3

JEDEC No.	Type	Use	MAXIMUM RATINGS Pc mw @ 25°C	BVCE BVCB*	Ic ma	TJ°C	ELECTRICAL PARAMETERS MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE	Dwg. No.
2N472	NPN-GD		200	45		175A	16T						2N335	3
2N472A	PNP-A		200	45		100S	18T		8.00		50		2N335	3
2N473	NPN-GD		200	15		175A	30T		11.0				2N333	3
2N474	NPN-GD		200	30		175A	30T		11.0				2N333	3
2N474A	NPN-GD		200	30		175A	50T		11.0				2N333	3
2N475	NPN-GD		200	45		175A	30T		11.0				2N333	3
2N475A	NPN		200	45		200S	35T		8.00		50		2N533	3
2N478	NPN-GD		200	15		175A	60T		11.0				4C30	3
2N479	NPN-GD		200	30		175A	60T		11.0				4C30	3
2N479A	NPN-GD		200	30		175A	80T						2N335	3
2N480	NPN-GD		200	45		175A	60T		11.0		.50		2N335	3
2N480A	NPN-GD		200	45		175A	60T		11.0				2N335	3
2N481	PNP		150	−12	−20	85	50T	1	3T		−10	−12	2N395	24
2N482	PNP		150	−12	−20	85	50T	1	3.5T		−10	−12	2N395	24
2N483	PNP		150	−12	−20	85	60T	1	5.5T		−10	−12	2N394	24
2N484	PNP		150	−12	−20	85	90T	1	10T		−10	−12	2N394	24
2N485	PNP		150	−12	−10	85	50T	1	7.5T		−10	−12	2N394	24
2N486	PNP		150	−12	−10	85	100T	1	12T		−10	−12	2N394	24
2N489		Si Uni	SEE G-E SPECIFICATIONS SECTION										2N489	31
2N489A		Si Uni	SEE G-E SPECIFICATIONS SECTION										2N489A	31
2N489B		Si Uni	SEE G-E SPECIFICATIONS SECTION										2N489B	31
2N490		Si Uni	SEE G-E SPECIFICATIONS SECTION										2N490	31
2N490A		Si Uni	SEE G-E SPECIFICATIONS SECTION										2N490A	31
2N490B		Si Uni	SEE G-E SPECIFICATIONS SECTION										2N490B	31
2N491		Si Uni	SEE G-E SPECIFICATIONS SECTION										2N491	31
2N491A		Si Uni	SEE G-E SPECIFICATIONS SECTION										2N491A	31
2N491B		Si Uni	SEE G-E SPECIFICATIONS SECTION										2N491B	31
2N492		Si Uni	SEE G-E SPECIFICATIONS SECTION										2N492	31
2N492A		Si Uni	SEE G-E SPECIFICATIONS SECTION										2N492A	31
2N492B		Si Uni	SEE G-E SPECIFICATIONS SECTION										2N492B	31
2N493		Si Uni	SEE G-E SPECIFICATIONS SECTION										2N493	31
2N493A		Si Uni	SEE G-E SPECIFICATIONS SECTION										2N493A	31
2N493B		Si Uni	SEE G-E SPECIFICATIONS SECTION										2N493B	31
2N494		Si Uni	SEE G-E SPECIFICATIONS SECTION										2N494	31
2N494A		Si Uni	SEE G-E SPECIFICATIONS SECTION										2N494A	31
2N494B		Si Uni	SEE G-E SPECIFICATIONS SECTION										2N494B	31
2N495	PNP		150	−25	−50	140	9	1	8 f_{os}		−.1	−10		
2N496	PNP		150	−10	−50	140	9	1	8 f_{os}		−.1	−10		
2N497	NPN	Si AF	4W	60	500	200	12*	200			10	30	2N497	24
2N497A	NPN	Si AF	5W	60	500	200	12*	200			10	30	2N497A	24
2N498	NPN	Si AF	4W	100	500	200	12*	200			10	30	2N498	24
2N498A	NPN	Si AF	5W	100	500	200	12*	200			10	30	2N498A	24

JEDEC No.	Type	Use	MAXIMUM RATINGS: P_C mw @ 25°C	BV_{CE} BV_{CB}*	I_C ma	T_J°C	ELECTRICAL PARAMETERS: MIN. h_{fe}-h_{FE}*	@ I_C ma	MIN. f_{hfb} mc	MIN. Ge db	MAX. I_{CO} (μa)	@ V_{CB}	Closest GE	Dwg. No.
2N499	PNP		30 @ 45°C	−18	−50	85	6	2		10	100	−30		
2N500	PNP		50 @ 45°C	−15		85					100	−20		
2N501	PNP		25 @ 45°C	−15*	−50	85	20*	−10			100	−15		
2N501A	PNP		25 @ 45°C	−15*	−50	100	20*	−10		8	25	−15		
2N502	PNP		25 @ 41°C	−20		85	9	2	200	8	−100	−20		
2N502A	PNP		25 @ 45°C	−30*		100	9	2			100	−30		
2N503	PNP		25 @ 41°C	−20	−50	85	9	2	100	11	−100	−20	2N396	24
2N505	PNP		125	40	250	85J	40T		8.00				2N320, 2N413	3, 24
2N506	PNP		50	−40*	−100	85	25	−10	.6		−15	−30		
2N507	NPN		50	40	100	85	25	10	.6		15	30		
2N508	PNP	AF Out	140	−16	−100	85	125T*	−20	3.5T		−16	−16	2N508	24
2N509	PNP		225	−30*	−40	100	.96α	10	750T		−5	−20		
2N514	PNP		80W	−40	−25A	95	12*	−25			−2.0	−20		
2N514A	PNP		80W	−60	−25A	95	12*	−25			2.0	−30		
2N514B	PNP		80W	−80	−25A	95	12*	−25	7.0T		−2.0	−40		
2N515	NPN		50	18	10	75	4	1	2	23	50	18	2N293	22
2N516	NPN		50	18	10	75	4	1	2	25	50	18	2N293	22
2N517	NPN		50	18	10	75	4	1	2	27	50	18	2N1121	22
2N519	PNP		100	−15		85	15	1	.5		−2	−5	2N394	24
2N519A	NPN-A		150	25		100S	35T*		.50		25		2N394	24
2N520	PNP		100	−12		85	20	1	3		−2	−5	2N394	24
2N520A	PNP-A		150	25		100S	100T*		3.00		25		2N394	24
2N521	PNP		100	−10		85	35	1	8		−2	−5	2N397	24
2N521A	PNP-A		150	25		100S	150T*		8.00		25		2N397	
2N522	PNP		100	−8		85	60	1	15		−2	−5		
2N523	PNP		100	−6		85	80	1	21		−2	−5		
2N524	PNP	AF	225	−30	−500	100	16	−1	.8		−10	−30	2N524	24
2N525	PNP	AF	225	−30	−500	100	30	−1	1		−10	−30	2N525	24
2N526	PNP	AF	225	−30	−500	100	44	−1	1.3		−10	−30	2N526	24
2N527	PNP	AF	225	−30	−500	100	60	−1	1.5		−10	−30	2N527	24
2N528	PNP		2.5W	−40		100	20*	−0.5			−15	−30		
2N529	PNP-NPN		100	15		85	15	1	2.5T		5	5		
2N530	PNP-NPN		100	15		85	20	1	3T		5	5	2N394	24
2N531	PNP-NPN		100	15		85	25	1	3.5T		5	5	2N395	24
2N532	PNP-NPN		100	15		85	30	1	4T		5	5	2N395	24
2N533	PNP-NPN		100	15		85	35	1	4.5T		5	5		
2N534	PNP		25 @ 50°C	−50	−25	65	35	−1			−15	−50	2N1057, 2N1924	23, 24
2N535	PNP		50	−20	−20	85	35	−1	2T		−10	−12	2N1415, 2N1175A	24, 24
2N535A	PNP		50	−20	−20	85	35	−1	2T		−10	−12	2N1415, 2N1175A	24, 24
2N535B	PNP		50	−20	−20	85	35	−1	2T		−10	−12	2N508, 2N1175A	24, 24
2N536	PNP		50	−20	−30	85	100*	−30	1		−10	−12	2N508	24
2N538	PNP		10W @ 70°C	−80*		95	40	2A	8T Kc		−20 ma	−80		

JEDEC No.	Type	Use	MAXIMUM RATINGS: P_C mw @ 25°C	BV_{CE} BV_{CB}*	I_C ma	T_J°C	ELECTRICAL PARAMETERS: MIN. h_{fe}-h_{FE}*	@ I_C ma	MIN. f_{hfb} mc	MIN. Ge db	MAX. I_{CO} (μa)	@ V_{CB}	Closest GE	Dwg. No.
2N538A	PNP		10W @ 70°C	−80*		95	40	2A	8T Kc		−20 ma	−80		
2N539	PNP		10W @ 70°C	−80*		95	27	2A	7T Kc		−20 ma	−80		
2N539A	PNP		10W @ 70°C	−80		95	27	2A	7T Kc		−20 ma	−80		
2N540	PNP		10W @ 70°C	−80		95	18	2A	6T Kc		−20	−80		
2N540A	PNP		10W @ 70°C	−80		95	18	2A	6T Kc		−20	−80		
2N544	PNP		80	−24*	−10	85	60T	1	30T	30.4	−16	−12		
2N545	NPN-GD		5000	60		175A	25T*		4.00				2N497A	24
2N546	NPN-GD		5000	30		175A	25T*		4.00				2N497A	24
2N547	NPN-GD		5000	60		175A	35T*		4.00				2N656A	24
2N548	NPN-GD		5000	30		175A	35T*		4.00				2N656A	24
2N549	NPN-GD		5000	60		175A	35T*		4.00				2N656A	24
2N550	NPN-GD		5000	30		175A	35T*		4.00				2N656A	24
2N551	NPN-GD		5000	60		175A	30T*		4.00				2N656A	24
2N552	NPN-GD		5000	30		175A	30T*		4.00				2N656A	24
2N553	PNP		12W @ 71°C	−80*	−4A	95	40	−.5A	20 Kc		−2 ma	−60		
2N554	PNP		10W @ 80°C	−40*	−3A	90	30T*	−.5A	8T Kc	20	−50T	−2		
2N555	PNP		10W @ 80°C	−30	−3A	90	20	−.5A	5 Kc	34T	−7 ma	−30		
2N556	NPN		100	25*	200	85	35*	1						
2N557	NPN		100	20*	200	85	20*	1						
2N558	NPN		100	15*	200	75	60*	1						
2N559	PNP		150	−15	−50	100	25*	10			−50	−5 @ 65°C		
2N560	NPN			.50			20*	−100			.10	−20	2N1613	3
2N561	PNP		50W	−50	−5A	100	65T	−1A	.5	24.6	−500	−30		
2N563	PNP		150	−25	−300	85	10*	1	.8T		−5	−10	2N44	23
2N564	PNP		120	−25	−300	85	10*	1	.8T		−5	−10	2N524	24
2N565	PNP		150	−25	−300	85	30*	1	1T		−5	−10	2N43	23
2N566	PNP		120	−25	−300	85	30*	1	1T		−5	−10	2N525	24
2N567	PNP		150	−25	−300	85	50*	1	1.5T		−5	−10	2N43, 2N526	23, 24
2N568	PNP		120	−25	−300	85	50*	1	1.5T		−5	−10	2N526	24
2N569	PNP		150	−20	−300	85	70*	1	2T		−5	−10	2N241A, 2N1175	23, 24
2N570	PNP		120	−20	−300	85	70*	1	2T		−5	−10	2N527, 2N1415	23, 24
2N571	PNP		150	−10	−300	85	100*	1	3T		−5	−10	2N508	24
2N572	PNP		120	−10	−300	85	100*	1	3T		−5	−10	2N508	24
2N574	PNP		25W @ 75°C	−60*	−15A	95	10*	−10A	6T Kc		−7 ma	−60		
2N574A	PNP		25W @ 75°C	−80*	−15A	95	10*	−10A	6T Kc		−20 ma	−80		
2N575	PNP		25W @ 75°C	−60*	−15A	95	19*	−10A	5T Kc		−7 ma	−60		
2N575A	PNP		25W @ 75°C	−80*	−15A	95	19*	−10A	5T Kc		−20 ma	−80		
2N576	NPN		200	20	400	100	80T*	30	5T		20	20		
2N576A	NPN		200	20	400	100	20*	400	5T		40	40		
2N578	PNP		120	−14	−400	85	10*	1	3		−5	−12	2N394	24
2N579	PNP		120	−14	−400	85	20*	1	5		−5	−12	2N396	24
2N580	PNP		120	−14	−400	85	30*	1	10		−5	−12	2N397	24

JEDEC No.	Type	Use	MAXIMUM RATINGS Pc mw @ 25°C	BVce BVcb*	Ic ma	Tj °C	ELECTRICAL PARAMETERS MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE	Dwg. No.
2N581	PNP		80	−15	−100	85	20*	−20	4		−6	−6	2N394	24
2N582	PNP		120	−14	−100	85	40*	−20	14		−5	−12	2N397	24
2N583	PNP		150	−15	−200	85	20*	−20	4		−6	−6	2N394	24
2N584	PNP		120	−14	−100	85	40*	−20	14		−5	−12	2N397	24
2N585	NPN		120	24	200	85	20*	20	3		8	12		
2N586	PNP		250	−45*	−250	85	35T*	−250			−16	−45	2N525, 2N1925	24, 24
2N587	NPN		150	20	200		20*	200			50	40		
2N588	PNP		30 @ 45°C	−15	−50	85					15	−15		
2N591	PNP		50	−32	−20	100	70T	2	.7T	41T	−6.5	−10	2N324, 2N526	3, 24
2N592	PNP		125	−20		85	20*	1	.4T		−5	−5	2N1414	24
2N593	PNP		125	−30		85	30*	.5	.6T		−5	−5	2N1414	24
2N594	NPN		100	20		85	20*	1	1.5		5	5		
2N595	NPN		100	15		85	35*	1	3		5	5		
2N596	NPN		100	10		85	50*	1	5		5	5		
2N597	PNP		250	−40	−400	100	40*	−100	3		−25	−45	2N526, 2N527	24, 24
2N598	PNP		250	−20	−400	100	50*	−100	5		−25	−30	2N508	24
2N599	PNP		250	−20	−400	100	100*	−100	12		25	−30		
2N600	PNP		750	−20	−400	100	50*	−100	5		−25	−30		
2N601	PNP		0.75	−20	−400	100	2.5	3	12		25	−30	2N395	24
2N602	PNP		120	−20		85	20*	.5			−8	−10	2N396	24
2N603	PNP		120	−20		85	30*	.5			−8	−10		
2N604	PNP		120	−20		85	40*	.5			−8	−10	2N397	24
2N605	PNP		120	−15		85	40T	−1		20	−10	−12	2N394	24
2N606	PNP		120	−15		85	60T	−1		25	−10	−12	2N395	24
2N607	PNP		120	−15		85	80T	−1		30	−10	−12	2N396	24
2N608	PNP		120	−15		85	120T	−1		35	−10	−12	2N396	24
2N609	PNP		180	−20	−200	85	90T*	100		30T	−25	−20	2N321, 2N324	3, 3
2N610	PNP		180	−20	−200	85	65T*	100		28T	−25	−20	2N320, 2N323	3, 3
2N611	PNP		180	−20	−200	85	45T*	100		26T	−25	−20	2N320, 2N322	3, 3
2N612	PNP		180	−20	−150	85	.96αT	1	.6T	37	−25	−20	2N319, 2N1098	3, 24
2N613	PNP		180	−20	−200	85	.97αT	1	.85T	32	−25	−20	2N320, 2N1097	3, 24
2N614	PNP		125	−15	−150	85	4.5T	.5	3T	26T	−6	−20	2N395	24
2N615	PNP		125	−15	−150	85	7.5T	.5	5T	34T	−6	−20	2N395	24
2N616	PNP		125	−12	−150	85	25T	.5	9T	20T	−6	−15	2N394	24
2N617	PNP		125	−12	−150	85	15T	.5	7.5T	30T	6	−15	2N394	24
2N618	PNP		45W	−80*	−3A	90	60*	—1A	5 Kc		−3 ma	−60		
2N622	NPN		400	50*	50	160	25T*	.5	.3	34T	.1	30		
2N624	PNP		100	−20	−10	100	20	2	12.5	20T	−30	−30		
2N625	NPN		2.5W	30		100	30*	50			100	−40		
2N631	PNP		170	−20	−50	85	150T	10	1.2T	35T	−25	−20	2N508	24
2N632	PNP		150	−24	−50	85	100T	10	1T	25T	−25	−20	2N324, 2N1175	3, 24
2N633	PNP		150	−30	−50	85	60T	10	.8T	25T	−25	−20	2N323, 2N1415	3, 24

JEDEC No.	Type	Use	MAXIMUM RATINGS Pc mw @ 25°C	BVce BVcb*	Ic ma	Tj °C	ELECTRICAL PARAMETERS MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE	Dwg. No.
2N634	NPN	Sw	150	20	300	85	15*	200	5		5	5		
2N634A	NPN	Sw	150	20	300	85	40*	10	5		6	25		
2N635	NPN	Sw	150	20	300	85	25*	200	10		5	5		
2N635A	NPN	Sw	150	20	300	85	80*	10	10		6	25		
2N636	NPN	Sw	150	20	300	85	35*	200	15		5	5		
2N636A	NPN	Sw	150	15	300	85	100*	10	15		6	25		
2N637	PNP		25W	−40	−5A	100	30*	−3A			1 ma	−25		
2N637A	PNP		25W	−70	−5A	100	30*	−3A			5 ma	−60		
2N637B	PNP		25W	−80	−5A	100	30*	−3A			5 ma	−60		
2N638	PNP		25W	−40	−5A	100	20*	−3A			1 ma	−25		
2N638A	PNP		25W	−70	−5A	100	20*	−3A			5 ma	−60		
2N638B	PNP		25W	−80	−5A	100	20*	−3A			5 ma	−60		
2N639	PNP		25W	−40	−5A	100	15*	−3A			1 ma	−25		
2N639A	PNP		25W	−70	−5A	100	15*	−3A			5 ma	−60		
2N639B	PNP		25W	−80	−5A	100	15*	−3A			5 ma	−60		
2N640	PNP		80	−34*	−10	85	.984αT	−1	42T	28T	−5	−12		
2N641	PNP		80	−34*	−10	85	.984αT	−1	42T	28T	−7	−12		
2N642	PNP		80	−34*	−10	85	.984αT	−1	42T	28T	−7	−12		
2N643	PNP		120	−29	−100	85	20*	−5	20		−10	−7		
2N644	PNP		120	−29	−100	85	20*	−5	40		−10	−7		
2N645	PNP		120	−29	−100	85	20*	−5	60		−10	−7		
2N647	NPN		100	25	50	85	70T*	−50		54T	14	25		
2N649	NPN		100	18	50	85	65T*	−50		54T	14	12		
2N650	PNP-A		200	45	250	100J	40T		2.00	42	15		2N1924	24
2N650A	PNP-A		200	45	500	100C			.75		50		2N1924	24
2N651	PNP-A		200	45	250	100J	75T		2.50	44	15		2N1925	24
2N652	PNP-A		200	45	250	100J	160T		3.00	46	15		2N1925	24
2N652A	PNP-A		200	45	500	100C	160T		1.25		50		2N1926	24
2N653	PNP-A		200	30	250	100J	40T		2.00	42	15		2N1926	24
2N654	PNP-A		200	30	250	100J	75T		2.50	44	15		2N1414	24
2N655	PNP-A		200	30	250	100J	160T		3.50	46	15		2N1175	24
2N656	NPN	Si AF	4W	60	500	200	30*	200			10	30	2N656, 2N508	24, 24
2N656A	NPN	Si AF	5W	60	500	200	30*	200			10	30	2N656A	24
2N657	NPN	Si AF	4W	100	500	200	30*	200			10	30	2N657	24
2N657A	NPN	Si AF	5W	100	500	200	30*	200			10	30	2N657A	24
2N658	PNP		175	−16	−1A	85	25*	−1	2.5		−6	−12	2N394	24
2N659	PNP		175	−14	−1A	85	40*	−1	5.0		−25	−25	2N396	24
2N660	PNP		175	−11	−1A	85	60*	−1	10		−25	−25	2N397	24
2N661	PNP		175	−9	−1A	85	80*	−1	15		−25	−25		
2N662	PNP		175	−11	−1A	85	30*	−1	4		−25	−25	2N396	24
2N665	PNP		35W	−80*	5A (IE)	95	40*	−.5A	20 Kc		−2 ma	−30 @ 71°C		
2N679	NPN		150	20		85	20*	30	2		25	25		

JEDEC No.	Type	Use	MAXIMUM RATINGS Pc mw @ 25°C	BVCE BVCB*	Ic ma	TJ °C	ELECTRICAL PARAMETERS MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE	Dwg. No.
2N680	NPN		150	20	50	85J	35T				14		2N1413	24
2N695	PNP-M		75	15	50	100J	40T		350					
2N696	NPN-PL	Sw	600	60*		175J	20*				1.0	30	2N696	3
2N696A	NPN-PL	Sw	800	60*		200J	45T		150		.10		2N2194A	3
2N697	NPN-PL	Sw	600	60*		175J	40*				1.0	30	2N697	3
2N697A	NPN-M		800	60*		200	70T		150		.10		2N2193A	3
2N698	NPN-PL	Sw	800	120*		200J	40T*		70.0		.005	75	2N698	3
2N699	NPN-PL	Sw	600	120*		175J	40*				2.0	60	2N699	3
2N699A	NPN-M		800	120*		200	70T		180		.10		2N1893	3
2N699B	NPN-PL		870	120*		200J	80T		120		.01		2N1893	3
2N700	PNP-M		75	25	50	100J	10T		500	23				
2N702	NPN		600	25	50	175	20*	10			0.5	10	2N706	16
2N703	NPN		600	25	50	175	10*	10			0.5	10	2N753	16
2N705	PNP	Sw	300	15*	50	100	25*							
2N705A	PNP-A		175	40	200	85J	75T		2.00	44				
2N706	NPN-PEP	Sw	300	25*	200	175J	20				0.5		2N706	16
2N706A	NPN-PEP	Sw	300	25*		175J	40T		750		0.5		2N706A	16
2N706B	NPN-M	Sw	300	25*		175J	40T*		400		10		2N914	16
2N707	NPN		1W	28			9*	10			3.5	15	2N915	16
2N707A	NPN-M		300	70	200	175	30T*		500		5.0		2N915	16
2N708	NPN-PEP	Sw	360	40		200J	50T*		500		.025		2N708	16
2N710	PNP-M	Sw	300	15	50	100	25*							
2N711	PNP-M	Sw	150	12	50	100J	30T*		360	22	3.0			
2N711A	PNP-M	Sw	150	15*	100	100S	25*				1.5	5		
2N711B	PNP-M	Sw	150	18*	100	100S	30*				1.5	10		
2N715	NPN-M		500	50		175J	30T*		150		.01		2N915	16
2N716	NPN-M		500	70		175J	30T*		150		10		2N915	16
2N717	NPN-PL	Sw	400	60		175J	40T*		150		1.0		2N717	16
2N718	NPN-PL	Sw	400	60		175J	75T*		150		1.0		2N718	16
2N718A	NPN-PL	Sw	500	75		200J	70T*		160		.01		2N718A	16
2N719	NPN-PL	Sw	400	120		175J	30T*		180		2.0		2N719	16
2N719A	NPN-PL	Sw	300	120		200J	30T*		100		.01		2N719A	16
2N720	NPN-PL	Sw	400	120		175J	65T*		180		2.0		2N720	16
2N721A	NPN-PL	Sw	500	120		200J	65T*		110		.01		2N720A	16
2N725	NPN-M		150	15	50		20T*							
2N728	NPN-D		500	30		175	40T*		150		5.0		2N706	16
2N729	NPN-D		500	15	3.0	175	40T*		150		5.0		2N717	16
2N735	NPN-D		1000	80	50	175	40T		40.0		1.0			
2N736	NPN-D		1000	80	50	175			50.0		1.0			
2N741	PNP-M		150	15	100	100J	25T*		360	22				
2N741A	PNP-M		150	20	100	100	25T*		360	22	3.0			
2N743	NPN-EM		300	25	200	300S	40T*						2N914	16

JEDEC No.	Type	Use	MAXIMUM RATINGS Pc mw @ 25°C	BVCE BVCB*	Ic ma	TJ °C	ELECTRICAL PARAMETERS MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE	Dwg. No.
2N744	NPN-EM		300	25	200	300S	80T*						2N914	16
2N753	NPN-PEP	Sw	300	25		175J	80T		750				2N753	16
2N754	NPN-M		300	60	50	175J	50T		45.0		1.0		2N915	16
2N758	NPN-M		500	45	100	200A	50T		50.0				2N759	16
2N759	NPN-PL	AF	500	45	100	200A	65T		50.0				2N759	16
2N760	NPN-PL	AF	500	45	100	200A	150T		50.0				2N760	16
2N761	NPN-M		500	45	100	200A	35T*		50.0				2N759	16
2N762	NPN-M		500	45	100	200A	70T*		50.0				2N759	16
2N768	PNP-MD		35	12	100	100	40T*		175		25			
2N769	PNP-M		35	12	100	100J	55T*		900		3.0			
2N779	PNP-MD		60	15	50	100	90T*		480		25		2N964	16
2N779A	PNP-MD		60	15	100	100	60T*		450		3.0		2N994	16
2N780	NPN-M		300	45		175J	20T		30.0				2N760	16
2N781	PNP-EM		150	15	200	100	25T				3.0		2N781	16
2N782	PNP-EM		150	12	200	100	20T				3.0		2N782	16
2N783	NPN-EM		300	40	200	175	40T				.25		2N914	16
2N784	NPN-EM		300	30	200	175	25T				.25		2N914	16
2N796	PNP-M		150	13	100	85A	75T*		80.0		3.0			
2N815	NPN-FA		75	25	200		80T*		8.00	14	10			
2N816	NPN-FA		75	25	200	100J	80T*		8.00	14	10			
2N818	NPN-FA		75	30	400	85J	25T		2.50		10			
2N819	NPN-FA		75	30	400	85J	30T		5.00		10			
2N820	NPN-FA		75	30	400	85J	30T		5.00		10			
2N821	NPN-FA		75	30	400	85J	70T*		10.0		10			
2N822	NPN		75	30	400	85J	70T*		10.0		10			
2N823	NPN		75	25	400	85J	40T		12.0		5.0			
2N824	NPN		75	25	400	85J	40T		12.0		5.0			
2N828	PNP-D		150	15	200	150S	40T*		400		3.0			
2N834	NPN-PEP	Sw	300	40	200	175J	40T*		500		.50		2N834	16
2N835	NPN-M		300	25	200	175	40T*		450		.50		2N834	16
2N839	NPN-M		300	45	50	175J	35T		30.0		1.0		2N759	16
2N840	NPN-M		300	45	50	175	70T		30.0		1.0		2N759	16
2N841	NPN-M		300	45	50	175	140T		40.0		1.0		2N760	16
2N844	NPN-M		300	60	50	175	80T*		50.0	14	1.0		2N718A	16
2N845	NPN-M		300	100	50	175	80T*		50.0	14	1.0		2N720A	16
2N846	PNP-MD		60	15	50	100S	35T*		450		25			
2N849	NPN-M		450	25		175J	40T*				10		2N706	16
2N850	NPN-M		450	25		175J	80T*				10		2N753	16
2N870	NPN-PL		500	100		200J	70T*		110		.01			
2N871	NPN		500	100		200J	120T*		130		.01		2N871	16
2N909	NPN-D		400	60		175J	55T		160		1.0		2N956	16
2N910	NPN-PL		500	100		200J	100T		60.0		.025			

JEDEC No.	Type	Use	Pc mw @ 25°C	BVce BVcb*	Ic ma	Tj °C	MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ Vcb	Closest GE	Dwg. No.
2N911	NPN-PL		500	100		200J	50T		50.0		.025			
2N912	NPN-PL		500	100		200J	30T		40.0		.025			
2N914	NPN-PEP	Sw	360	40		200J	30T		400		.025		2N914	16
2N915	NPN-PL	AF	360	70		200J	40T		400		.01		2N915	16
2N916	NPN-PL	AF	360	45		200J	50T		500		.01		2N916	16
2N929	NPN-PL		300	45		175J	40		30.0		.01		2N915	16
2N930	NPN-PL		300	45		175J	100		30.0		.01		2N915	16
2N956	NPN-PL		500	75		200J	100T		200		.01		2N956	16
2N960	PNP	Sw	150	15		100	20T		460					
2N961	PNP-EM	Sw	150	12		100	20T		460					
2N962	PNP-EM	Sw	150	12		100	20T		460					
2N964	PNP-EM	Sw	150	15		100	40T*		460					
2N965	PNP-EM	Sw	150	12		100	40T*		460					
2N966	PNP-EM	Sw	150	12		100	40T*		460					
2N968	PNP		150	15		100J	20T*		320		3.0			
2N969	PNP		150	12		100	20T*		320					
2N970	PNP		150	12		100	20T*		320		3.0			
2N971	PNP		150	7.0		100	20T*		320		10			
2N972	PNP		150	15		100	40T*		320		3.0			
2N973	PNP		150	12		100	40T*		320		3.0			
2N974	PNP		150	12		100	40T*		320		3.0			
2N975	PNP		150	7.0		100	40T*		320		10			
2N994	PNP	Sw	200	15	150	150S	75*				3.0			
2N1000	NPN-A		150	40		100S	35T*		7.00		15			
2N1008	PNP-A		167	20	300	75J	90T		1.00				2N1415	24
2N1008A	PNP		167	40	300	85J	90T		1.00				2N526	24
2N1008B	PNP		167	60	300	85J	90T		1.00				2N1925	24
2N1009	PNP-A		150	25	20	85A	40T		.50		800		2N395	24
2N1010	NPN		20	10	2	85	35T	−.3	2T		10	10	2N1694	24
2N1012	NPN-A		150	40		100S	50T		3.00		25			
2N1015	NPN		150 @ 45°C	30	75A	150	10*	2A	20T Kc		20 ma	30		
2N1015A	NPN		150 @ 45°C	60	75A	150	10*	2A	20T Kc		20 ma	60		
2N1015B	NPN		150 @ 45°C	100	7.5A	150	10*	2A	20T Kc		20 ma	100		
2N1015C	NPN		150 @ 45°C	150	7.5A	150	10*	2A	20T Kc		20 ma	150		
2N1015D	NPN		150 @ 45°C	200	7.5A	150	10*	2A	20T Kc		20 ma	200		
2N1015E	NPN		150 @ 45°C	250	7.5A	150	10*	2A	20T Kc		20 ma	250		
2N1015F	NPN		150 @ 45°C	300	7.5A	150	10*	2A	20T Kc		20 ma	300		
2N1016	NPN		150 @ 45°C	30	7.5A	150	10*	5A	20T Kc		20 ma	30		
2N1016A	NPN		150 @ 45°C	60	7.5A	150	10*	5A	20T Kc		20 ma	60		
2N1016B	NPN		150 @ 45°C	100	7.5A	150	10*	5A	20T Kc		20 ma	100		
2N1016C	NPN		150 @ 45°C	150	7.5A	150	10*	5A	20T Kc		20 ma	150		
2N1016D	NPN		150 @ 45°C	200	7.5A	150	10*	5A	20T Kc		20 ma	200		

JEDEC No.	Type	Use	Pc mw @ 25°C	BVce BVcb*	Ic ma	Tj °C	MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ Vcb	Closest GE	Dwg. No.
2N1016E	NPN		150 @ 45°C	250	7.5A	150	10*	5A	20T Kc		20 ma	250		
2N1016F	NPN		150 @ 45°C	300	7.5A	150	10*	5A	20T Kc		20 ma	300		
2N1017	PNP		150	−10	−400	85	70*	1	15		−25	−30		
2N1021	PNP		50W	−100	−5	95	70T*	−1A			−2 ma	−100		
2N1022	PNP		50W	−120	−5	95	70T*	−1A			−2 ma	−120		
2N1038	PNP		20W	−40	−3A	95	35*	−1A			−125	.5		
2N1039	PNP		20W	−60	−3A	95	35*	−1A			−125	.5		
2N1040	PNP		20W	−80	−3A	95	35*	−1A			−125	.5		
2N1041	PNP		20W	−100	−3A	95	35*	−1A			−125	.5		
2N1046	PNP		15W	−8	−3A	65	70*	−0.5A			−1 ma	−40		
2N1047	NPN		40W @ 25°C	80*	500	200	12*	500			15	30	7E1	11
2N1048	NPN		40W @ 25°C	120*	500	200	12*	500			15	30	7E3	11
2N1049	NPN		40W @ 25°C	80*	500	200	30*	500			15	30	7E2	11
2N1050	NPN		40W @ 25°C	120*	500	200	30*	500			15	30	2N2204	11
2N1056	PNP	Obsolete	240	−50	−300	100	18*	−20	.5		−25	−70	2N1614, 2N1924	23, 24
2N1057	PNP	Sw	240	−45	−300	100	34*	−20	.5		−16	−45	2N1057, 2N1924	23, 24
2N1058	NPN		50	20	50	75	10	1	4	22.5	50	18	2N292	22
2N1059	NPN		180	15	100	75	50*	35	10 Kc	25	50	40		
2N1067	NPN		5W	30	.5A	175	15*	200	.75		500	60		
2N1068	NPN		10W	30	1.5A	175	15*	750	.75		500	60		
2N1069	NPN		50W	45	4A	175	10*	1.5A	.5		1 ma	60		
2N1070	NPN		50W	45	4A	175	10*	1.5A	.5		1 ma	60		
2N1086	NPN	Osc	65	9	20	85	17*	1	8T	24T	3	5	2N1086	22
2N1086A	NPN	Osc	65	9	20	85	17*	1	8T	24T	3	5	2N1086A	22
2N1087	NPN	Osc	65	9	20	85	17*	1	8T	26T	3	5	2N1087	22
2N1090	NPN		120	15	400	85	50*	20	5		8	12		
2N1091	NPN		120	12	400	85	40*	20	10		8	12		
2N1092	NPN		2W	30	500	175	15*	200	.75		500	60		
2N1093	PNP-A		150	30	250	85J	125T		8.00		6.0		2N1307	24
2N1097	PNP	AF Out	140	−16	−100	85	55T	1			−16	−16	2N1097	24
2N1098	PNP	AF Out	140	−16	−100	85	45T	1			−16	−16	2N1098	24
2N1099	PNP		30W	80*		95	35*	5A	10 Kc		8 ma	−80		
2N1100	PNP		30W	100*		95	25*	5A	10 Kc		8 ma	−100		
2N1101	NPN		180	15	100	75	25*	35	10 Kc		50	20		
2N1102	NPN		180	25	100	75	25*	35	10 Kc		50	40		
2N1107	PNP		30	16*	5	85	33	−0.5	40		−10	−12		
2N1108	PNP		30	16*	5	85	30	−0.5	35		−10	−12		
2N1109	PNP		30	16*	5	85	15	−0.5	35		−10	−12		
2N1110	PNP		30	16*	5	85	26	−0.5	35		−10	−12		
2N1111	PNP		30	20*	5	85	22	−0.5	35		−10	−12		
2N1114	NPN-A		150	25	200	100J	110T*		10.0		30			
2N1115	PNP	Sw	150	−20	−125	85	35	−60	5		−6	−20	2N1115, 2N396A	23, 24

JEDEC No.	Type	Use	MAXIMUM RATINGS Pc mw @ 25°C	BVce BVcb*	Ic ma	Tj °C	ELECTRICAL PARAMETERS MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ Vcb	Closest GE	Dwg. No.
2N1115A	PNP	Sw	150	−35	−125	85	35	−60	5		−6	−20	2N1115A, 2N656A	23, 24
2N1116	NPN-GD		5000	60		175A	70T*		4.00				2N656A	24
2N1117	NPN-GD		5000	60		175A	70T*		4.00				2N656A	24
2N1118	PNP		150	−25	−50	140	9				1.0	−25		
2N1118A	PNP		150	−25	−50	140	15	1			0.1	−10		
2N1119	PNP		150	−10	−50	140	6*	−15			0.1	−10		
2N1121	NPN	IF	65	15	20	85	34*	1	8 Kc		5	15	2N1121	22
2N1122	PNP		−25 @ 45°C	−10	−50	85	35	1.0			5	−5		
2N1122A	PNP		−25 @ 45°C		−50	85	35	1.0			5	−5		
2N1123	PNP		750	−40	−400	100	40*	−100	3		−25	−45		
2N1128	PNP-A		150	25	250	85J	120T		1.25		20		2N324	3
2N1129	PNP-A		150	25	250	85J	165T*		.75		25		2N508	24
2N1130	PNP-A		150	30	250	85J	110T*		.75		25		2N1926	24
2N1141	PNP		750		100	100	12	−10	750T		−5	−15		
2N1142	PNP		750		100	100	10	−10	600T		−5	−15		
2N1143	PNP		750		100	100	8	−10	480T		−5	−15		
2N1144	PNP	AF Out	140	−16	−100	85	55T	1			−16	−16	2N1144, 2N1097	24, 24
2N1145	PNP	AF Out	140	−16	−100	85	45T	1			−16	−16	2N1145, 2N1098	24, 24
2N1149	NPN		150	45*	25	175	−0.9	−1	4T	35T	2	30	2N1276	3
2N1150	NPN		150	45*	25	175	−0.948	−1	5T	39T	2	30	2N1277	3
2N1151	NPN		150	45*	25	175	−0.948	−1	8T	39T	2	30	2N1278	3
2N1152	NPN		150	45*	25	175	−0.9735	−1	6T	42T	2	30	2N1278	3
2N1153	NPN		150	45*	25	175	−0.987	−1	7T	42.5T	2	30	2N1279	3
2N1154	NPN		750	50*	60	150	−0.9	−5		30	5	50	2N333	3
2N1155	NPN		750	80*	50	150	−0.9	−5		30	6	80	2N333	3
2N1156	NPN		750	120*	40	150	−0.9	−5		30	8	120		
2N1157	PNP			−60*		95	38*	−10A			−7.0 ma	−60		
2N1157A	PNP			−80*		95	38*	−10A			−20 ma	−80		
2N1159	PNP		20W @ 71°C	80*	−65	−65	30*	3A	10T Kc		8 ma	−80		
2N1160	PNP		20W @ 71°C	80*		−65	20*	5A	10T Kc		8 ma	−80		
2N1168	PNP		45W	−50*	5A (IE)	95	110T	1A	10T Kc	37T	−8 ma	−50		
2N1171	PNP			−12	400	85	30*	1	10		5	−12	2N397	24
2N1172	PNP			40*		−65	30	100		34T	0.2 ma	−40		
2N1175	PNP-A		200	35	200	85J	90T*		4.20		12		2N1175	24
2N1175A	PNP-A		200	35	200	85J	90T*		4.20		12		2N1175A	24
2N1177	PNP		80	−30*	−10	71	100		140		−12	−12		
2N1178	PNP		80	−30*	−10	71	40		140		−12	−12		
2N1179	PNP		80	−30*	−10	71	80		140		−12	−12		
2N1180	PNP		80	−30*	−10	71	80		100		−12	−12		
2N1183	PNP		1W	−20	−3.0	100	20*	−400	500 Kc	−250	−250	−45		
2N1183A	PNP		1W	−30	−3.0	100	20*	−400	500 Kc		−250	−80		
2N1183B	PNP		1W	−40	−3.0	100	20*	−400	500 Kc		−250	−80		

JEDEC No.	Type	Use	MAXIMUM RATINGS Pc mw @ 25°C	BVce BVcb*	Ic ma	Tj °C	ELECTRICAL PARAMETERS MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ Vcb	Closest GE	Dwg. No.
2N1184	PNP		1W	−20	−3.0	100	40*	−400	500 Kc		−250	−45		
2N1184A	PNP		1W	−30	−3.0	100	40*	−400	500 Kc		−250	−80		
2N1184B	PNP		1W	−40	−3.0	100	40*	−400	500 Kc		−250	−80		
2N1186	PNP		200	60		100J	50T		1.50				2N1924	24
2N1187	PNP		200	60		100J	85T		2.00				2N1926	24
2N1188	PNP		200	60		100J	155T		2.50				2N1926	24
2N1191	PNP-A		175	40	200	85J	40T		1.50	42			2N1414	24
2N1192	PNP-A		175	40	200	85J	75T		2.00	44			2N1175	24
2N1193	PNP-A		175	40	200	85J	160T		2.50	46			2N508	24
2N1198	NPN	Sw	65	25	75	85	17*	8	5		1.5	15	2N1198, 2N167	22, 22
2N1199	NPN		100	20	100	150	12*	20			0.7	−10		
2N1202	PNP			−60		95	40*	−0.5A			−2.0 ma	−80		
2N1203	PNP			−70		95	25*	−2A			−2.0 ma	−120		
2N1213	PNP		75	−25	−100	71					−5	−12		
2N1214	PNP		75	−25	−100	71					−5	−12		
2N1215	PNP		75	−25	−100	71					−5	−12		
2N1216	PNP		75	−25	−100	71					−5	−12		
2N1217	NPN		75	20	25		40*	.5	6.0		29	15	2N1217	22
2N1224	PNP		120	−40	−10	100	20	−1.5	30	15	−12	−12		
2N1225	PNP		120	−40	−10	100	20	−1.5	100	15	−12	−12		
2N1226	PNP		120	−60	−10	100	20	−1.5	30	15	−12	−12		
2N1228	PNP		400	−15		160	14		1.2T		−0.1	−12		
2N1229	PNP		400	−15		160	28		1.2T		−0.1	−12		
2N1230	PNP		400	−35		160	14		1.2T		−0.1	−30		
2N1231	PNP		400	−35		160	28		1.2T		−0.1	−30		
2N1232	PNP		400	−60		160	14		1.0T		−0.1	−50		
2N1233	PNP		400	−60		160	28		1.0T		−0.1	−50		
2N1234	PNP		400	−110		160	14		8T		−0.1	−90		
2N1238	PNP		1W free air	−15		160	14		1.2T		−0.1	−12		
2N1239	PNP		1W free air	−15		160	28		1.2T		−0.1	−12		
2N1240	PNP		1W free air	−35		160	14		1.2T		−0.1	−30		
2N1241	PNP		1W free air	−35		160	28		1.2T		−0.1	−30		
2N1242	PNP		1W free air	−60		160	14		1.0T		−0.1	−50		
2N1243	PNP		1W free air	−60		160	28		1.0T		−0.1	−50		
2N1244	PNP		1W free air	−110		160	14		.8T		−0.1	−90		
2N1247	NPN		200	6.0		175A	25T		5.00					
2N1248	NPN		200	6.0		175A	20T		5.00					
2N1251	NPN		150	15	100	85	70		7.5		50	20		
2N1252	NPN		2W	20		175	15*	150			10	20		
2N1253	NPN		2W	20		175	40*	150			10	20		
2N1261	PNP			−45		95	20*							
2N1262	PNP			−45		95	30*				−2.0	−60		

JEDEC No.	Type	Use	MAXIMUM RATINGS: P_C mw @ 25°C	BV_{CE} BV_{CB}*	I_C ma	T_J°C	ELECTRICAL PARAMETERS: MIN. h_{fe}-h_{FE}*	@ I_C ma	MIN. f_{hfb} mc	MIN. G_e db	MAX. I_{CO} (μa)	@ V_{CB}	Closest GE	Dwg. No.
2N1263	PNP			−45		95	45*				−20	−60		
2N1264	PNP		50	−20*	50	75	15	1.5			50	−20		
2N1265	PNP		50	−10*	100	85	25	1	600		100		2N1097	24
2N1266	PNP		80	−10*		85	10	1			100	−10	2N1098	24
2N1273	PNP-A		150	15	150	85J	50T		2.00				2N1097	24
2N1274	PNP-A		150	25	150	85J	50T		2.00				2N1414	24
2N1276	NPN	Si AF	150	30	25	150	10T	10	15	37T	1	30	2N1276	3
2N1277	NPN	Si AF	150	30	25	150	20T	10	15	39T	1	30	2N1277	3
2N1278	NPN	Si AF	150	30	25	150	33T	10	15	44T	1	30	2N1278	3
2N1279	NPN	Si AF	150	30	25	150	80T	10	15	45T	1	30	2N1279	3
2N1280	PNP		200	16	400	85	40	−20	5		−10	−10	2N396	24
2N1281	PNP		200	12	400	85	60	−20	7		−10	−10	2N396	24
2N1282	PNP		200	6	400	85	70	−20	10		−10	−10	2N397	24
2N1284	PNP		150	15	400	85	30	−10	5		−6	−20	2N396	24
2N1287	PNP		165	20*	300	85	40		1.00		10		2N526	24
2N1287A	PNP		165	20*	300	85	40		1.00		10		2N527	24
2N1288	NPN	Obsolete	75	5	50	85	50*	10	40		5	5		
2N1289	NPN	Obsolete	75	.15	50	85	50*	10	40		5	15		
2N1291	PNP		20W	30	3	85	40*	0.5			5	−2		
2N1293	PNP		20W	60	3	85	40*	0.5			5	−2		
2N1295	NPN		20W	80	3	85	40*	0.5			5	−2		
2N1297	PNP		20W	100	3	85	40*	0.5			5	−2		
2N1299	NPN		150	20	200	100	35*	50	4.0		100	40		
2N1300	PNP		150	−12	−100	85	50	−10			−3			
2N1301	PNP		150	−12	−100	85	50	−10			−3			
2N1302	NPN		150	25*	300	100	50		3.00		6.0			
2N1303	PNP		150	30*	300	100	50		3.00		6.0		2N1303	24
2N1304	NPN	Sw	300	20	300	100	40*	10	5		6	25		
2N1305	PNP		150	30*	300	100	70		5.00		6.0		2N1305	24
2N1306	NPN	Sw	300	15	300	100	60*	10	10		6	25		
2N1307	PNP		150	30*	300	100	100		10.0		6.0		2N1307	24
2N1308	NPN	Sw	300	15	300	100	80*	10	15		6	25		
2N1309	PNP		150	30*	300	100	150		15.0		6.0		2N1309	24
2N1310	NPN		120	90			20*	5	1.5T		7	5	2N1510	22
2N1313	PNP		180	−15	400	100	40*		6		2.5	−0.5	2N396	24
2N1316	PNP		200	15	400	85	50*		10		−5	−12	2N397	24
2N1317	PNP		200	12	400	85	45*		10		−6	−12	2N397	24
2N1318	PNP		200	6	400	85	40*		10		−7	−10	2N397	24
2N1343	PNP		150	16	400	85	15*	−50	4		−6	−15	2N395	24
2N1344	PNP		150	10	400	85	60*	−20	7		10	−15	2N397, 2N396	24, 24
2N1345	PNP		150	8	400	85	30*	−400	10		−6	−12	2N397	24
2N1346	PNP		150	10	400	85	40*	−14	10		−5	−5	2N397	24

JEDEC No.	Type	Use	MAXIMUM RATINGS: P_C mw @ 25°C	BV_{CE} BV_{CB}*	I_C ma	T_J°C	ELECTRICAL PARAMETERS: MIN. h_{fe}-h_{FE}*	@ I_C ma	MIN. f_{hfb} mc	MIN. G_e db	MAX. I_{CO} (μa)	@ V_{CB}	Closest GE	Dwg. No.
2N1347	PNP		150	12	200	85	30*	10	5		−6	−12	2N396	24
2N1348	PNP		200	40*	400	85	95*		5.0		10		2N1305	24
2N1352	PNP		150	20	200	85	40*		2.5T		−5	−30	2N526, 2N1925	24, 24
2N1353	PNP		200	10	200	85	25*	10	1.5		6	10	2N394, 2N397	24, 24
2N1354	PNP		200	15	200	85	25*	10	3		6	15	2N395	24
2N1355	PNP		200	20	200	85	30*	10	5		6	20	2N396	24
2N1356	PNP		200	30*	200	85	80*		8.0		6.0		2N397	24
2N1357	PNP		200	15	200	85	40*	10	10		6	15	2N397	24
2N1358	PNP			80*		95	40*	1.2	100					
2N1366	PNP	Sw	150	20*			70*		10.0				2N397	24
2N1367	NPN	Sw	150	20*			70*		10.0					
2N1370	PNP		150	25*	150	100	80*		2.0				2N1415	24
2N1371	PNP		150	45*	150	100	80		2.0				2N1415	24
2N1372	PNP		210	25*	200	100	45		2.0				2N1415	24
2N1373	PNP		250	45*	200	100	45		2.0				2N1924	24
2N1374	PNP		250	25*	200	100	70		2.0				2N1415	24
2N1375	PNP		250	45*	200	100	70		2.0				2N1925	24
2N1376	PNP		250	25*	200	100	95		2.0				2N1175	24
2N1377	PNP		250	45*	200	100	95		2.0				2N1926	24
2N1378	PNP		250	12*	200	100	200		2.0				2N508	24
2N1379	PNP		250	25*	200	100	200		2.0				2N1175	24
2N1380	PNP		250	12*	200	100	100		2.0				2N1097	24
2N1381	PNP		250	25*	200	100	100		2.0				2N1414	24
2N1382	PNP		200	25*	200	85	80		2.0				2N1415	24
2N1383	PNP		200	25*	200	85	50		2.0				2N1414	24
2N1389	NPN		250	50*	50	175			25	15			2N696	3
2N1404	PNP		150	25*	300	85	100*		4.00		5.0		2N404	24
2N1408	PNP		150	50*		100	25						2N1924	24
2N1411	PNP		25 @ 45°C	−5	−50	85	20*	−50			5	−5		
2N1413	PNP	AF Sw	200	−25	−200	85	25*	−20	0.8		−12	−30	2N1413	24
2N1414	PNP	AF Sw	200	−25	−200	85	34*	−20	1.0		−12	−30	2N1414	24
2N1415	PNP	AF Sw	200	−25	−200	85	53*	−20	1.3		−12	−30	2N1415	24
2N1420	NPN-M		600	60*		175	140*		250				2N1711	3
2N1420A	NPN-PL		800	60*		200	120*		200				2N1711	3
2N1427	PNP		25 @ 45°C	−6	−50	85	20*	−50			5	−6		
2N1428	PNP		100	−6	−50	140	12*	−5			0.1	−6		
2N1429	PNP		100	−6	−50	140	12*	−5			0.1	−6		
2N1431	NPN		180	15	100	75	75*	35			50	20		
2N1432	PNP		100	−45	10	100	30	2			15	−45		
2N1433	PNP			−50	3.5	95	20*	2	5		0.1	−2		
2N1434	PNP			−50	3.5	95	45*	2	5		0.1	−2		
2N1435	PNP			−50	3.5	95	30*	2	5		0.1	−2		

JEDEC No.	Type	Use	MAXIMUM RATINGS: Pc mw @ 25°C	BVce BVcb*	Ic ma	Tj °C	ELECTRICAL PARAMETERS: MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ Vcb	Closest GE	Dwg. No.
2N1436	PNP		50	−15*	−50	100	20*	−10						
2N1446	PNP		200	25	400	85	16*	20	.8		10	30	2N524	24
2N1447	PNP		200	25	400	85	35*	20	1.5		10	30	2N525	24
2N1448	PNP		200	25	400	85	50*	20	2		10	30	2N526	24
2N1449	PNP		200	25	400	85	70*	20	2.5		10	30	2N527	24
2N1450	PNP		120	30*	100	85	20*	10			10	7		
2N1451	PNP		200	45*	400	85	45*		1.50		15		2N1413	24
2N1452	PNP		200	45*	400	85	60*		2.20		15		2N1414	24
2N1471	PNP		200	12*	200	85	160*		5.0		5.0		2N508	24
2N1472	NPN		100	25	100	150	20	10			0.5	10		
2N1473	NPN			20	400	75	25*	400	4		100	40		
2N1478	PNP		250	−30*	−400	100	40*	−100	3		5	1.5	2N396, 2N1415	24, 24
2N1479	NPN		4W	60*	1.5	175	15*	200	1.5	60	10	30	2N497A	16
2N1480	NPN		4W	100*	1.5	175	15*	200	1.5	100	10	30	2N497A	16
2N1481	NPN		4W	60*	1.5	175	35*	200	1.5	60	10	30	2N656A	16
2N1482	NPN		4W	100*	1.5	175	35*	200	1.5	100	10	30	2N656A	16
2N1483	NPN		15W	60*	3	175	15*	750	1.25		15	30		
2N1484	NPN		15W	100*	3	175	15*	750	1.25		15	30		
2N1485	NPN		15W	60*	3	175	35*	750	1.25		15	30		
2N1486	NPN		15W	100*	3	175	35*	750	1.25		15	30		
2N1487	NPN		60W	60*	6	175	10*	1.5	1		25	30		
2N1488	NPN		60W	100*	6	175	10*	1.5	1		25	30		
2N1489	NPN		60W	60*	6	175	25*	1.5	1		25	30		
2N1490	NPN		60W	100*	6	175	25*	1.5	1		25	30		
2N1499	PNP		25	−25*	−50	85	20*	−10			5	−5		
2N1499A	PNP		60	20*	50	100	50*		110		3.0			
2N1500	PNP		50	−15*	−50	100	20*	−50			5	−5		
2N1501	PNP			−60*		95	25*	−2A			−2	−60		
2N1502	PNP			−40*		95	25*	−2A			−2	−40		
2N1507	NPN		0.6W	60*	500	175	100*	150			1	30		
2N1510	NPN	Neon Indicator	75	70	20	85	8*	1			5	75	2N1510	22
2N1514	NPN		2.5	100V	8.0 Amps	175	75*		1000 Kc		25	30	2N1924	24
2N1524	PNP		80	24*	10	85	60*		33.0		16		2N1924	24
2N1525	PNP		80	24*	10	85	60*		33.0		16		2N1925	24
2N1564	NPN		1200	80*	50	175	70		40		1.0		2N698	3
2N1565	NPN		1200	80*	50	175	120		50		1.0		2N699	3
2N1566	NPN		1200	80*	50	175	120		50		1.0		2N699	3
2N1566A	NPN		600	80	100	200	125		200		.50		2N699	3
2N1572	PNP		600	125			35						2N698	3
2N1573	PNP		600	125			70*						2N699	3
2N1574	PNP		600	125			140*						2N699	3
2N1586	NPN		150	15	25		18		4.0				2N1276	3

JEDEC No.	Type	Use	MAXIMUM RATINGS: Pc mw @ 25°C	BVce BVcb*	Ic ma	Tj °C	ELECTRICAL PARAMETERS: MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ Vcb	Closest GE	Dwg. No.
2N1587	NPN		150	30	25		18		4.0				2N1276	3
2N1588	NPN		150	60	25		18		4.0				2N332	3
2N1589	NPN		150	15	25		50		6.0				2N1277	3
2N1590	NPN		150	30	25		50		6.0				2N1277	3
2N1591	NPN		150	60	25		50		6.0				2N334	3
2N1592	NPN		150	15	25		140		7.0				2N1279	3
2N1593	NPN		150	30	25		140		7.0				2N1279	3
2N1594	NPN		150	60	25		140		7.0				2N337	3
2N1605	NPN		150	24	100	100	40*	20	4		5	12		
2N1605A	NPN		200	40	100	100	60*		6.0		10			
2N1613	NPN-PL	Sw	800	75		200	80*		160		.01		2N1613	3
2N1614	PNP	Sw	240	−65*	−300	85	18*	−20	0.5		−25	−65	2N1614	23
2N1624	NPN		150	25		100	120*		8.0		10			
2N1644	NPN		600	60		175	75*		150		1.0		2N697	3
2N1644A	NPN		600	60*		175	75*		150		1.0		2N697	3
2N1646	PNP		150	15*		100S	20*				3.0			
2N1671	PN	Si Uni				SEE G-E SPECIFICATIONS SECTION							2N1671	31
2N1671A	PN	Si Uni				SEE G-E SPECIFICATIONS SECTION							2N1671A	31
2N1671B	PN	Si Uni				SEE G-E SPECIFICATIONS SECTION							2N1671B	31
2N1672	NPN		120	40*			50		2.0		25			
2N1672A	NPN		120	40*		85	20*		2.0					
2N1684	PNP		100	25*	100	100			8.0		20		2N397	24
2N1694	NPN		75	20*	25	85S	30*		9.0		1.5		2N1694	24
2N1700	NPN		5000	60*	1.0 Amp	200	20		1.20		75		2N656A	24
2N1705	PNP		200	18*	400	100	110		4.0		10		2N527	24
2N1706	PNP		200	25*	400	100	90		3.0		10		2N527	24
2N1707	PNP		200	30*	400	100	95		3.0		15		2N527	24
2N1711	NPN		800	30*	500	175	35		230				2N1711	3
2N1714	NPN		7.5	90	1.0 Amp	175			16				7D2	10
2N1715	NPN		7.5	150	1.0 Amp	175			16				7D4	10
2N1716	NPN		7.5	90	1.0 Amp	175			16				7D13	10
2N1717	NPN		7.5	150	1.0 Amp	175			16				7D4	10
2N1718	NPN		7.5	90	1.0 Amp	175			16				7G2	
2N1719	NPN		7.5	150	1.0 Amp	175			16				7G4	
2N1720	NPN		7.5	90	1.0 Amp	175			16				7G13	
2N1721	NPN		7.5	150	1.0 Amp	175			16				7G4	
2N1726	PNP		60	20	50	100	120*		150					
2N1727	PNP		60	20	50	100	150*		150					
2N1728	PNP		60	20	50	100	100*		150					
2N1754	PNP		50	13*	100	85	50*		75					
2N1779	NPN		100	25*	100	100	40*		5.0		10			
2N1780	NPN		100	25*	100	100	40*		8.0		10			

JEDEC No.	Type	Use	MAXIMUM RATINGS Pc mw @ 25°C	BVCE BVCB*	Ic ma	TJ °C	ELECTRICAL PARAMETERS MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE	Dwg. No.
2N1781	NPN		100	25*	100	100	60*		6.0		20			
2N1785	PNP		45	10*	50	85	60*		125		10			
2N1786	PNP		45	10*	50	85	60*		125		10			
2N1787	PNP		45	15*	50	85	60*		125		10			
2N1808	NPN		150	25*	300	100S	60*		4.0		5.0			
2N1889	NPN-PL		800	100*		200J	70*		110		.01			
2N1890	NPN-PL		800	100*		200J	120*		130		.01			
2N1893	NPN-PL	Sw	800	120*		200J	85*		110		.01		2N1893	3
2N1924	PNP	AF	225	−60*	−500	85	30*	−100	1.0		−10	45	2N1924	24
2N1925	PNP	AF	225	−60*	−500	85	47*	−100	1.3		−10	45	2N1925	24
2N1926	PNP	AF	225	−60*	−500	85	65*	−100	1.5		−10	45	2N1926	24
2N1954	PNP		200	60*	1.0 Amp	100J	120				20		2N1926	24
2N1955	PNP		200	60*	1.0 Amp	100J	200				20		2N1926	24
2N1956	PNP		200	60*	1.0 Amp	100J	120				20		2N1926	24
2N1958	NPN		600	60*	500	175	45				.50		2N2194A	3
2N1959	NPN		600	60*	500	175	80				.50		2N2193A	3
2N1960	PNP		150	15*	200	100	25				3.0			
2N1961	PNP		150	12*	200	100	20				3.0			
2N1969	PNP		150	30*	400	100	125		10		5.0		2N1307	24
2N1973	NPN		800	100*		200J	100		60		.025			
2N1974	NPN		800	100*		200J	50		50		.025			
2N1975	NPN		800	100*		200J	30		40		.025			
2N1986	NPN		600	50*		150J	150*		50.0		5.0		2N697	3
2N1987	NPN		600	50*		150J	50*		50.0		5.0		2N696	3
2N1997	PNP		250	45*	500	100S	75*		3.0		6.0		2N527	24
2N1998	PNP		250	35*	500	100S	100*		6.50		6.0		2N527	24
2N2000	PNP	Sw	300	15	1.0A	100S	50*	100	2		10	30		
2N2001	PNP	Sw	300	15	1.0A	100S	100*	100	6		6	15		
2N2002	PNP	Ch	250	5	100	200S					.01	4.5		
2N2003	PNP	Ch	250	5	100	200S					.03	4.5		
2N2004	PNP	Ch	250	15	100	175S	12*	1			.0015	10		
2N2005	PNP	Ch	250	15	100	200S		1			.05	10		
2N2006	PNP	Ch	250	35	100	200S		1			.02	30		
2N2007	PNP	Ch	250	35	100	200S		1			.05	30		
2N2008	NPN	Pwr	3W	110	500	200J	30*	10			.05	100		
2N2009	PNPN	Sw			1.0A	150S							3N84	28
2N2010	PNPN	Sw			1.0A	150S							3N85	28
2N2011	PNPN	Sw			1.0A	150S							3N85	28
2N2012	PNPN	Sw			1.0A	150S								
2N2013	PNPN	Sw			1.0A	150S								
2N2014	PNPN	Sw			1.0A	150S								
2N2015	NPN	Pwr	150W	50	10A	200	15*	5A			200	40		

JEDEC No.	Type	Use	MAXIMUM RATINGS Pc mw @ 25°C	BVCE BVCB*	Ic ma	TJ °C	ELECTRICAL PARAMETERS MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE	Dwg. No.
2N2016	NPN	Pwr	150W	65	10A	200	15*	5A			200	40		
2N2017	NPN	AF	5W	60	1A	200	35/20*	10/1A			10	30		
2N2020	NPN	Pwr	40W	150*	2A	175S	25*	100			100	100	2N2150	15
2N2021	NPN	Pwr	40W	200*	2A	175S	25*	100			100	100	2N2150	15
2N2022	PNP		150	15*	50	100J	35				3.0			
2N2032	NPN	Pwr	85W	45	5A	200S	20*	2A			20ma	45		
2N2033	NPN	Pwr		60	3A	200	20*	500			150	80		
2N2034	NPN	Pwr		60	3A	200	20*	1A			150	80		
2N2035	NPN	Pwr		60	3A	200	20*	1.5A			150	80		
2N2036	NPN	Pwr		60	3A	200	20*	2A			150	80		
2N2038	NPN	AF		45	500	200S	12*	200			15	30	2N497	5
2N2039	NPN	AF		75	500	200S	12*	200			15	30	2N498	5
2N2040	NPN	AF		45	500	200S	30*	200			15	30	2N656	5
2N2041	NPN	AF		75	500	200S	30*	200			15	30	2N657	5
2N2042	PNP		200	105*			50		.50				2N1925	24
2N2042A	PNP		200	105*	200	100	50		.50		25		2N1925	24
2N2043	PNP		200	105*			113		.75				2N1926	24
2N2043A	PNP		200	105*	200	100	113		.75		25		2N1926	24
2N2048	PNP	Sw	150	15	100	100S	50*	10			5	5		
2N2048A	PNP	Sw	150	20	100	100S	50*	10			3	15		
2N2049	NPN-PL		800	75*		200J	60*		50		.01			
2N2059	PNP	Sw	60	10*	50	100S	20*	10			5	5		
2N2060	NPN-PL	Diff	500	100*		200J	35*	.01			.002	80	2N2060	16
2N2061	PNP	Sw		10	3A	85S	10*	500	2kc		2ma	20		
2N2062	PNP	Sw		10	3A	85S	20*	2A	2kc		2ma	20		
2N2063	PNP	Sw		15	3A	95S	10*	2A	2kc		400	2		
2N2064	PNP	Sw		15	3A	95S	20*	2A	2kc		400	2		
2N2065	PNP	Sw		25	3A	95S	10*	2A	2kc		400	8		
2N2066	PNP	Sw		25	3A	95S	20*	2A	2kc		400	2		
2N2067	PNP	AF		25	3A	95S	20*	500		28	3ma	40		
2N2068	PNP	AF		55	3A	95S	20*	500		28	3ma	80		
2N2069	PNP	AF		40*	12A	95S	30*	5A	1.5kc		15ma	40		
2N2070	PNP	AF		80*	12A	95S	30*	5A	1.5kc		15ma	80		
2N2071	PNP	AF		40*	12A	95S	30*	5A	1.5kc		15ma	40		
2N2072	PNP	AF		80*	12A	95S	30*	5A	1.5kc		15ma	80		
2N2074	PNPN	Sw	200	50	1.0A	150S							3N85	28
2N2083	PNP	MF	100	30*	10	85S	25*	1			12	12		
2N2084	PNP	HF	125	20	10	100S	40	1			8	6		
2N2085	NPN		150	33*	500	100	100		8.0		5.0			
2N2086	NPN		600	120*	500	300S	70*		225		2.0		2N2194	3
2N2087	NPN		600	120*	500	300S	65*		225		2.0		2N2193	3
2N2101	NPN	Pwr		40	3A	200S	15*	1A	25kc		30	30	2N1724	14

JEDEC No.	Type	Use	MAXIMUM RATINGS: Pc mw @ 25°C	BVce / BVcb*	Ic ma	Tj °C	ELECTRICAL PARAMETERS: MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ Vcb	Closest GE	Dwg. No.
2N2102	NPN	Sw	5W	65	1A	200J	40*	150			.002	60	2N2193A	5
2N2104	PNP	Sw		35	600	200J	25*	150			.010	30		
2N2105	PNP	Sw		35	600	200J	15*	150			.010	30		
2N2106	NPN-M	AF	125	60*		150J			15MC		.20	30	2N2106	24
2N2107	NPN-M	AF	125	60*		150J			15MC		.20	30	2N2107	24
2N2108	NPN-M	AF	125	60*		150J			15MC		.20	30	2N2108	24
2N2150	NPN	Pwr		80	2A	200S	20*	1A			10	120	2N2150	15
2N2151	NPN	Pwr		80	2A	200S	40*	1A			10	120	2N2151	15
2N2160		Si Uni				SEE G-E	SPECIFICATIONS SECTION						2N2160	31
2N2161	NPN	Sw	200	35	50	175S	70*	10			.01	45	2N1711	5
2N2162	PNP	Ch	150	30	50	140S	3.5	1			.01	10		
2N2163	PNP	Ch	150	15	50	140S	3.5	1			.01	4.5		
2N2164	PNP	Ch	150	8	50	140S	6	1			.02	4.5		
2N2165	PNP	Ch	150	30	50	140S	2.5	1			.02	10		
2N2166	PNP	Ch	150	15	50	140S	2.5	1			.02	4.5		
2N2167	PNP	Ch	150	8	50	140S	4	1			.02	4.5		
2N2168	PNP	Sw	60	15	100	100S	50*	10			3	5		
2N2169	PNP		60	15*		100S	85*				3.0			
2N2170	PNP	Sw	60	10	100	100S	20*	10			5	5		
2N2171	PNP	AF	500	50*	400	100S	110*	20			10	25	2N508A	24
2N2172	PNP	AF	200	15	400	85S	30*	10			6	20	2N524	24
2N2173	PNP	Sw	240	15	750	100S	30*	200			10	10	2N527	24
2N2175	PNP	AF	100	6	50	175S	30*	.02			.001	4.5		
2N2176	PNP	AF	100	6	50	175S	30*	.02			.001	4.5		
2N2177	PNP	AF	100	6	50	160S	35*	.05			.005	4.5		
2N2178	PNP	AF	100	6	50	160S	35*	.05			.005	4.5		
2N2180	PNP	Sw	50	6	50	100S	70*	50			1	5		
2N2181	PNP	Ch	150	25	50	140S	10*	5			.01	10		
2N2182	PNP	Ch	150	25	50	140S	10*	5			.01	10		
2N2183	PNP	Ch	150	15	50	140S	10*	5			.01	10		
2N2184	PNP	Ch	150	15	50	140S	10*				.01	10		
2N2185	PNP	Ch	150	30	50	140S	1	1			.001	10		
2N2186	PNP	Ch	150	30	59	149S					.001	10		
2N2187	PNP	Ch	150	30	50	140S					.001	10		
2N2192	NPN-PEP	Sw	800	60	1.0 Amp	300S	100*	150			10 mμa	30	2N2192	3
2N2192A	NPN-PEP	Sw	800	60	1.0 Amp	300S	100*	150			10 mμa	30	2N2192A	3
2N2193	NPN-PEP	Sw	800	80	1.0 Amp	300S	40*	150			10 mμa	30	2N2193	3
2N2193A	NPN-PEP	Sw	800	80	1.0 Amp	300S	40*	150			10 mμa	30	2N2193A	3
2N2193B	NPN	Sw	800	80*	1A	200J	40*	150			.01	60	2N2193B	5
2N2194	NPN-PEP	Sw	800	60	1.0 Amp	300S	20*	150			10 mμa	30	2N2194	3
2N2194A	NPN-PEP	Sw	800	60	1.0 Amp	300S	20*	150			10 mμa	30	2N2194A	3
2N2194B	NPN	Sw	800	60*	1A	200J	20*	150			.01	30	2N2194B	5

JEDEC No.	Type	Use	MAXIMUM RATINGS: Pc mw @ 25°C	BVce / BVcb*	Ic ma	Tj °C	ELECTRICAL PARAMETERS: MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ Vcb	Closest GE	Dwg. No.
2N2195	NPN-PEP	Sw	600	45	1.0 Amp	300S	20*	150			100 mμa	60	2N2195	3
2N2195A	NPN-PEP	Sw	600	45	1.0 Amp	300S	20*	150			100 mμa	60	2N2195A	3
2N2195B	NPN	Sw	800	45*	1A	200J	20*	150			.1	30	2N2195B	5
2N2196	NPN	Power	2W	80*		175	10*		15T		75	80	2N2196	8
2N2197	NPN	Power	2W	80*		175	20*		15T		75	80	2N2197	8
2N2198	NPN	Pwr		80	200	200S	35	100			15	80	2N657A	5
2N2201	NPN	Power	15W	120*		175J	30*		15MC		50	120	2N2201	8
2N2202	NPN	Power	15W	120*		175J	30*		15MC		50	120	2N2202	9
2N2203	NPN	Power	15W	120*		175J	30*		15MC		50	120	2N2203	10
2N2204	NPN	Power	15W	120*		175J	30*		15MC		50	120	2N2204	11
2N2303	PNP	IF	0.6W	35	500	175J	75	1			−1	−30		
2N2304	NPN	Pwr	25WC	40	3A	200S	20*	300			100	30		
2N2305	NPN	Pwr	75WC	40	6A	200S	15*	800			200	30		
2N2306	NPN	Sw	13WC	50	2A	175S	12*	350			1 ma	75		
2N2307		Si Uni	250			SEE	G-E SPECIFICATION SECTION						2N1671	31
2N2308	NPN	Pwr	25WC	80	3A	200S	20*	1A			250	100		
2N2309	NPN	AF Out	600	30	500	175J	40	0.2			.005	4	2N2192	5
2N2310	NPN	AF	350	60	500	175J	12*	200			.025	60	2N2353	4
2N2311	NPN	AF	350	100	500	175J	12*	200			.025	100	2N2364	4
2N2312	NPN	AF	350	60	500	175J	30*	200			.025	60	2N2351	4
2N2313	NPN	AF	350	100	500	175J	30*	200			.025	100	2N2364	4
2N2314	NPN	AF	350	60*	500	175J	20*	150			.025	30	2N2352	4
2N2315	NPN	AF	350	60*	500	175J	40*	150			.025	30	2N2351	4
2N2316	NPN	AF	350	120*	500	175J	40*	150			.025	60		
2N2317	NPN	AF	350	75*	500	175J	40*	150			.010	60	2N2351	4
2N2318	NPN	Sw	360	30*		200S	40*	20			.050	20		
2N2319	NPN	Sw	300	30*		200S	40*	20			.050	20		
2N2320	NPN	Sw	600	30*		200S	40*	20			.050	20		
2N2322	PNPN	Sw		REFER TO G. E. SILICON CONTROLLED RECTIFIER MANUAL									2N2322	
2N2323	PNPN	Sw		REFER TO G. E. SILICON CONTROLLED RECTIFIER MANUAL									2N2323	
2N2324	PNPN	Sw		REFER TO G. E. SILICON CONTROLLED RECTIFIER MANUAL									2N2324	
2N2325	PNPN	Sw		REFER TO G. E. SILICON CONTROLLED RECTIFIER MANUAL									2N2325	
2N2326	PNPN	Sw		REFER TO G. E. SILICON CONTROLLED RECTIFIER MANUAL									2N2326	
2N2327	PNPN	Sw		REFER TO G. E. SILICON CONTROLLED RECTIFIER MANUAL									2N2327	
2N2328	PNPN	Sw		REFER TO G. E. SILICON CONTROLLED RECTIFIER MANUAL									2N2328	
2N2329	PNPN	Sw		REFER TO G. E. SILICON CONTROLLED RECTIFIER MANUAL									2N2329	
2N2330	NPN	Ch	800	20	500	175S	50*	10			.001	4.5		
2N2331	NPN	Ch	500	20	500	175S	50*	10			.001	4.5	2N929	16
2N2332	PNP	Ch	150	15*	100	200S					−.010	−4.5		
2N2333	PNP	Ch	150	15*	100	200S					−.030	−4.5		
2N2334	PNP	Ch	150	30*	100	200S					.010	4.5		
2N2335	PNP	Ch	150	30*	100	200S					.050	4.5		

JEDEC No.	Type	Use	MAXIMUM RATINGS Pc mw @ 25°C	BVCE BVCB*	Ic ma	TJ °C	ELECTRICAL PARAMETERS MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE	Dwg. No.
2N2336	PNP	Ch	150	50*	100	200S					.020	30		
2N2337	PNP	Ch	150	50*	100	200S					.050	30		
2N2338	NPN	Pwr	150WC	40	7.5A	200S	7*	6A						
2N2339	NPN	Pwr	40WC	40	2.5A	200S	6*	1.5A					2N1049B	6
2N2340	NPN	Pwr		40	1.0A	175S	10*	750					7B1	8
2N2341	NPN	Pwr		40	1.0A	175S	40*	750					7B13	8
2N2342	NPN	Pwr		60	1.0A	175S	10*	750					7B1	8
2N2343	NPN	Pwr		40	1.0A	175S	40*	750					7B13	8
2N2344	PNPN	Sw	REFER TO G. E. SILICON CONTROLLED RECTIFIER MANUAL										2N2344	
2N2345	PNPN	Sw	REFER TO G. E. SILICON CONTROLLED RECTIFIER MANUAL										2N2345	
2N2346	PNPN	Sw	REFER TO G. E. SILICON CONTROLLED RECTIFIER MANUAL										2N2346	
2N2347	PNPN	Sw	REFER TO G. E. SILICON CONTROLLED RECTIFIER MANUAL										2N2347	
2N2348	PNPN	Sw	REFER TO G. E. SILICON CONTROLLED RECTIFIER MANUAL										2N2348	
2N2349	NPN	AF	150	24	25	200S	120*	10			1	12		
2N2350	NPN	Sw	400	40	1A	200J	75*	10			.010	30	2N2350	4
2N2351	NPN	Sw	400	50	1A	200J	30*	10			.010	60	2N2351	4
2N2352	NPN	Sw	400	40	1A	200J	15*	10			.010	30	2N2352	4
2N2353	NPN	Sw	350	25	1A	200J	20*	150			.100	30	2N2353	4
2N2354	NPN	AF	180	20*	150	85S	50*	35		25	10	10		
2N2356	NPN(2)	Ch-Inv	600	25*	500	200J	2.5	50			.010	20	2N2356	32
2N2357	PNP	Sw	170WC	30	50A	110S	30*	20A			50 ma	60		
2N2358	PNP	Sw	170WC	60	50A	110S	30*	20A			50 ma	100		
2N2359	PNP	Sw	170WC	80	50A	110S	30*	20A			50 ma	120		
2N2360	PNP	VHF	60	20*	50	125J	10*	2		14	10	10		
2N2361	PNP	VHF	60	20*	50	125J	10*	2		14	10	10		
2N2362	PNP	VHF	60	20*	50	100J					10	10		
2N2363	PNP	VHF/UHF	75	20	50	100S	10*	2			5	12		
2N2364	NPN	Sw	400	80	1A	200J	40*	150			.010	60	2N2364	4
2N2365	NPN	Sw	800	60		175J	100*	150			.010	60		
2N2368	NPN	Sw	360	15	500	200J	20*	10			.4	20		
2N2369	NPN	Sw	360	15	500	200J	40*	10			.4	20		
2N2370	PNP	AF	200	15	100	200S	15*	.025			.005	4		
2N2371	PNP	AF	200	15	100	200S	20*	.025			.005	4		
2N2372	PNP	AF	150	15	100	200S	15*	.025			.005	4		
2N2373	PNP	AF	150	15	100	200S	15*	.025			.005	4		
2N2374	PNP	AF	250	35*	500	100S	100*	100			5	2	2N508A	24
2N2375	PNP	AF	250	35*	500	100S	35*	100			5	2	2N526	24
2N2376	PNP	AF	250	35*	500	100S	35*	100			5	2	2N526	24
2N2377	PNP	IF	150	25	50	140S	10*	5			1	25		
2N2378	PNP	Sw	150	10	50	140S	15*	15			.1	10		
2N2379	PNP	Pwr	150WC	100*	15A	100S	25*	5A			8 ma	100		
2N2380	NPN	Sw	600	40	500	175J	20*	150			4	40		

JEDEC No.	Type	Use	MAXIMUM RATINGS Pc mw @ 25°C	BVCE BVCB*	Ic ma	TJ °C	ELECTRICAL PARAMETERS MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE	Dwg. No.
2N2381	PNP	Sw	300	15	500	100S	40*	200			7	5		
2N2382	PNP	Sw	300	20	500	100S	40*	200			7	5		
2N2383	NPN		85WC	60	5A	200S	20*	1.5A			1 ma	80		
2N2384	NPN		85WC	60	5A	200S	20*	1.5A			1 ma	80		
2N2387	NPN	AF	300	45	30	175J	60	1			.010	45	2N915	16
2N2388	NPN	AF	300	45	30	175J	150	1			.010	45	2N929	16
2N2389	NPN	AF	450	75*	500	200J	30	1			.010	60	2N911	16
2N2390	NPN	AF	450	75*	500	200J	50	1			.010	60	2N910	16
2N2391	PNP	AF	300	20	50	175J	15	10			10	25		
2N2392	PNP	AF	300	20	50	175J	30	10			10	25		
2N2393	PNP	AF	450	35	300	175J	15	1			1	30		
2N2394	PNP	AF	450	35	300	175J	25	1			1	30		
2N2395	NPN	AF	450	40	300	200J	20*	150			.010	30		
2N2396	NPN	AF	450	40	300	200J	40*	150			.010	30		
2N2397	NPN	Sw	300	15	200	200J	25*	10			.1	15		
2N2398	PNP	VHF	60	20*	50	100J	10*	2		16	10	10		
2N2399	PNP	VHF MXR	60	20*	50	100J	10*	2		16	10	10		
2N2400	PNP	Sw	150	7	100	100S	30*	10			3	5		
2N2401	PNP	Sw	150	10	100	100S	50*	10			1.5	5		
2N2402	PNP	Sw	150	12	100	100S	60*	10			1.5	5		
2N2403	NPN	Sw	1W	60	1A	200S	20*	600			1	30	2N2195	5
2N2404	NPN	Sw	1W	60	1A	200S	40*	600			1	30	2N2192	5
2N2405	NPN		1W	90	1A	200S	60*	150			.010	100	2N657	5
2N2410	NPN	Sw	800	30	800	200J	30*	150			.3	30		
2N2411	PNP	Sw	300	20	100	200J	20*	10			.010	25		
2N2412	PNP	Sw	300	20	100	200J	40*	10			.010	25		
2N2413	NPN	IF	300	18	200	300S	30*	10			.1	20		
2N2414	NPN	Diff.	600	28	500	200J	50	5			.025	60	12A8	21
2N2415	PNP	IF	75	10	20	100J	15	2			5	10		
2N2416	PNP	IF	75	10	20	100J	10	2			5	10		
2N2417		Si Uni	SEE G. E. SPECIFICATION SECTION										2N2417	30
2N2418		Si Uni	SEE G. E. SPECIFICATION SECTION										2N2418	30
2N2419		Si Uni	SEE G. E. SPECIFICATION SECTION										2N2419	30
2N2420		Si Uni	SEE G. E. SPECIFICATION SECTION										2N2420	30
2N2423	PNP	Pwr Sw	90WC	100*	5A	100S	20*	2A			5 ma	100		
2N2424	PNP	Sw	375	40*	50	160S	30*	5			0.1	30		
2N2425	PNP	Sw	375	30*	50	160S	25*	5			0.1	30		
2N2426	NPN	Lo PA	150	40*	200	100S	35	1		35	20	40		
2N2427	NPN	IF/RF	500C	40	50	200S	20*	.010			0.5	40	2N760	16
2N2428	PNP	Lo Pwr	500	32*	100	75S	50*	2			10	10		
2N2429	PNP	Lo Pwr	500	32*	100	75S	65*	2			10	10		
2N2430	PNP	Lo Pwr	280	32*	300	75S	60*	100			10	10	2N527	24

JEDEC No.	Type	Use	MAXIMUM RATINGS: Pc mw @ 25°C	BVCE BVCB*	Ic ma	TJ °C	ELECTRICAL PARAMETERS: MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE	Dwg. No.
2N2431	PNP	Lo PO	550	10*	1A	90S	60*	300			10	10		
2N2432	NPN	Ch	300	30	100	175	50*	1			0.01	25		
2N2433	NPN	Sw	800	45	1A	200	30	1			.001	60	2N2352	4
2N2434	NPN	Sw	800	45	1A	200	50	1			.001	60	2N2350	4
2N2435	NPN	Sw	800	80	500	200	30	1			.001	90	2N2364	4
2N2436	NPN	Sw	800	80	500	200	50	1			.001	90	2N2350	4
2N2437	NPN	Ampl	800	75	500	200	18	1			.001	75	2N2353	4
2N2438	NPN	Ampl	800	75	500	200	36	1			.001	75	2N2364	4
2N2439	NPN	Ampl	800	75	500	200	76	1			.001	75	2N2350	4
2N2440	NPN	Sw	800	80	500	200	50	1			.001	90	2N2353	4
2N2443	NPN	A Pwr	4W	100		200S	30	1			.0015	90	2N2243	
2N2444	PNP	Ampl	85WC	80	10A	110S	50	0.5A			20 ma	80		
2N2445	PNP	Ampl	90WC	50	15A	100S	30	0.5A			20 ma	100		
2N2446	PNP	Sw	90WC	60	7A	125S	15*	5A			0.5 ma	30		
2N2447	PNP	AF	75	24	100	85S	25	1			10	20	2N1415	24
2N2448	PNP	AF	75	24	100	85S	25	1			10	20	2N1415	24
2N2449	PNP	AF	75	20	100	85S	50	1			10	20	2N527	24
2N2450	PNP	AF	75	20	100	85S	50	1			10	20	2N527	24
2N2451	PNP	Sw		5	50	85S	25*	10			5	6		
2N2453	NPN(2)	Diff	200	30	50	200	150*	1			.005	50	2N2453	21
2N2453A	NPN(2)	Diff	200	50	50	200	150*	1			.005	60	2N2453A	21
2N2454	PNPN	SCR, Sw												
2N2455	PNP	Sw	150	8	200	100S	40*	30			2	6		
2N2456	PNP	Sw	150	8	200	100S	40*	30			2	6		
2N2459	NPN Si	Lo PA	400	60	50	275S	20*	1			.002	80	2N2353	4
2N2460	NPN Si	Lo PA	400	60	50	275S	35*	1			.002	80	2N2353	4
2N2461	NPN Si	Lo PA	400	60	50	275S	70*	1			.002	80	2N2350	4
2N2462	NPN Si	Lo PA	400	60	50	275S	100*	1			.002	80	2N2350	4
2N2463	NPN Si	Lo PA	500	60	50	275S	20*	1			.002	80	2N720	16
2N2464	NPN Si	Lo PA	500	60	50	275S	35*	1			.002	80	2N720	16
2N2465	NPN Si	Lo PA	500	60	50	275S	70*	1			.002	80	2N956	16
2N2466	NPN Si	Lo PA	500	60	50	275S	100*	1			.002	80	2N956	16
2N2467	PNP	A Pwr	5W	30	3A	110S	20*	1A			10 ma	60		
2N2468	PNP	A Pwr	5W	60	3A	110S	20*	1A			10 ma	100		
2N2469	PNP	A Pwr	5W	100	3A	110S	20*	1A			10 ma	200		
2N2472	NPN	Ampl	1W	100	1A	175S	30*	200			50	120		
2N2473	NPN	Ampl	1W	100	1A	175S	30*	200			50	120		
2N2474	PNP	Lo PA	250	15	50	160	8*	0.1			.001	30		
2N2476	NPN	Sw	600	20		300S	20*	150			0.2	30	2N2195	5
2N2477	NPN	Sw	600	20		300S	40*	150			0.2	30	2N2195	5
2N2478	NPN	Sw	600	40	500	175	30*	150			2	60	2N2193	5
2N2479	NPN	Sw	600	40	500	175	30*	150			4	40	2N2193	5

JEDEC No.	Type	Use	MAXIMUM RATINGS: Pc mw @ 25°C	BVCE BVCB*	Ic ma	TJ °C	ELECTRICAL PARAMETERS: MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE	Dwg. No.
2N2480	NPN(2)	Diff	300	40	500	200	30*	1			.05	60	2N2480	21
2N2480A	NPN(2)	Diff	300	40	500	200	50*	1			.02	60	2N2480A	21
2N2481	NPN	Sw	360	15	500	300S	40*	10			.05	20		
2N2482	NPN	IF/RF	150	12	100	100S	25*	2			5	6	16L3	1
2N2483	NPN	AS	360	60	50	200	175*	1			.001	45		
2N2484	NPN	AS	360	60	50	200	250*	1			.001	45		
2N2485	NPN	VHF/UHF	8.8WC	120	1A	200S	10*	500			500	120		
2N2486	NPN	VHF/UHF	8.8WC	140	1A	200S	10*	500			500	140		
2N2487	PNP	Sw	60	10	100	100S	20*	10			3	5		
2N2488	PNP	Sw	60	10	100	100S	20*	50			3	5		
2N2489	PNP	Sw	60	15	100	100S	20*	10			2.5	15		
2N2490	PNP	Pwr Sw	170WC	70*	12A	110S	20*	5A			.2 ma	2		
2N2491	PNP	Pwr Sw	170WC	60*	12A	110S	35*	5A			.2 ma	2		
2N2492	PNP	Pwr Sw	170WC	80*	12A	110S	25*	5A			.2 ma	2		
2N2493	PNP	Pwr Sw	170WC	100*	12A	110S	25*	5A			.2 ma	2		
2N2494	PNP	IF/RF	83	20*	10	75S	25*	1			6	6		
2N2495	PNP	IF/RF	83	20*	10	75S	25*	1			6	6		
2N2496	PNP	IF/RF	83	20*	10	75S	25*	1			6	6		
2N2501	NPN	Sw	360	20		200	10*	10			.025	20	2N708	16
2N2509	NPN	Sw	360	80	200	300S	40*	10			.005	100	2N720A	16
2N2510	NPN	Sw	360	65	200	300S	150*	10			.005	80		
2N2511	NPN	Sw	360	50	200	300S	240*	10			.005	60		
2N2512	PNP	Vi Ampl	150	70*	30	75S	20	1			5	6		
2N2514	NPN	A	400	60	100	200S	15*	5			.005	50		
2N2515	NPN	A	400	60	100	200S	30*	5			.005	50	2N2352	4
2N2516	NPN	A	400	60	100	200S	60*	5			.005	50	2N2352	4
2N2517	NPN	Lo PA	400	80	50	200S	15*	5			.005	80	2N2364	4
2N2518	NPN	Lo PA	400	80	50	200S	30*	5			.005	80	2N2364	4
2N2519	NPN	Lo PA	400	80	50	200S	60*	5			.005	80	2N2364	4
2N2520	NPN	Lo PA	400	60	100	200S	12.5*	1			.005	45	2N2353	4
2N2521	NPN	Lo PA	400	60	100	200S	25*	1			.005	45	2N2353	4
2N2522	NPN	Lo PA	400	60	100	200S	50*	1			.005	45	2N2353	4
2N2523	NPN	Lo PA	400	45		300S	40*	.010			.002	45		
2N2524	NPN	Lo PA	400	45		300S	100*	.010			.002	45		
2N2525	NPN	VHF		80	1A	200	10*	350			5	28		
2N2526	PNP	Pwr Sw	85WC	80	10A	110S	20*	3A			150	2		
2N2527	PNP	Pwr Sw	85WC	120	10A	110S	20*	3A			150	2		
2N2528	PNP	Pwr Sw	85WC	160	10A	110S	20*	3A			150	2		
2N2529	NPN	Lo PA	150	40	25	175S	10	1			.050	30	2N759	16
2N2530	NPN	Lo PA	150	40	25	175S	12	1			.050	30	2N759	16
2N2531	NPN	Lo PA	150	40	25	175S	20	1			.050	30	2N759	16
2N2532	NPN	Lo PA	150	40	25	175S	45	1					2N760	16

JEDEC No.	Type	Use	MAXIMUM RATINGS P_C mw @ 25°C	BV_{CE} BV_{CB}*	I_C ma	T_J °C	ELECTRICAL PARAMETERS MIN. h_{fe}-h_{FE}*	@ I_C ma	MIN. f_{hfb} mc	MIN. G_e db	MAX. I_{CO} (μa)	@ V_{CB}	Closest GE	Dwg. No.
2N2533	NPN	Lo PA	150	40	25	175S	20*	10			.050	30	2N759	16
2N2534	NPN	Lo PA	150	40	25	175S	45*	10			.050	30	2N759	16
2N2535	PNP	Sw	10WC	30	3A	100S	40	400			0.25 ma	60		
2N2536	PNP	Sw	10WC	40	3A	100S	40	400			0.25 ma	80		
2N2537	NPN	Sw	800	30	800	200	50*	150			0.25	40	2N2193	5
2N2538	NPN	Sw	800	30	800	200	100*	150			0.25	40	2N2192	5
2N2539	NPN	Sw	500	30	800	200	50*	150			0.25	40		
2N2540	NPN	Sw	500	60	800	200	100*	150			0.25	40	2N956	16
2N2541	PNP	Sw	215	30	1A	100	60*	50			5	12		
2N2542	PNPN			SEE G. E. SILICON CONTROLLED RECTIFIER MANUAL									2N2542	
2N2543	PNPN			SEE G. E. SILICON CONTROLLED RECTIFIER MANUAL									2N2543	
2N2544	PNPN			SEE G. E. SILICON CONTROLLED RECTIFIER MANUAL									2N2544	
2N2545	PNPN			SEE G. E. SILICON CONTROLLED RECTIFIER MANUAL									2N2545	
2N2546	PNPN			SEE G. E. SILICON CONTROLLED RECTIFIER MANUAL									2N2546	
2N2547	PNPN			SEE G. E. SILICON CONTROLLED RECTIFIER MANUAL									2N2547	
2N2548	PNPN			SEE G. E. SILICON CONTROLLED RECTIFIER MANUAL									2N2548	
2N2549	PNPN			SEE G. E. SILICON CONTROLLED RECTIFIER MANUAL									2N2549	
2N2550	PNPN			SEE G. E. SILICON CONTROLLED RECTIFIER MANUAL									2N2550	
2N2551	PNP	AF	400	150	1A	200	15*	100			.1	100		
2N2552	PNP	Pwr	20WC	40	3A	100	20*	1A			125	20		
2N2553	PNP	Pwr	20WC	60	3A	100	20*	1A			125	30		
2N2554	PNP	Pwr	20WC	80	3A	100	20*	1A			125	40		
2N2555	PNP	Pwr	20WC	100	3A	100	20*	1A			125	50		
2N2556	PNP	Pwr	20WC	40	3A	100	20*	1A			125	20		
2N2557	PNP	Pwr	20WC	60	3A	100	20*	1A			125	30		
2N2558	PNP	Pwr	20WC	80	3A	100	20*	1A			125	40		
2N2559	PNP	Pwr	20WC	100	3A	100	20*	1A			125	50		
2N2560	PNP	Pwr	20WC	40	3.5A	100	20*	3A			125	20		
2N2561	PNP	Pwr	20WC	60	3.5A	100	20*	3A			125	30		
2N2562	PNP	Pwr	20WC	80	3.5A	100	20*	3A			125	40		
2N2563	PNP	Pwr	20WC	100	3.5A	100	20*	3A			125	50		
2N2564	PNP	Pwr	20WC	40	3.5A	100	20*	3A			125	20		
2N2565	PNP	Pwr	20WC	60	3.5A	100	20*	3A			125	30		
2N2566	PNP	Pwr	20WC	80	3.5A	100	20*	3A			125	40		
2N2567	PNP	Pwr	20WC	100	3.5A	100	20*	3A			125	50		
2N2568	NPN	Pwr	1WC	35	100	100	15*	40		10	2	15		
2N2569	NPN	Ch	300	20	500	200	50*	100			.010	15		
2N2570	NPN	Ch	300	20	500	200	50*	100			.010	15		
2N2571	NPN	Ch	300	20	500	200	50*	100			.010	15		
2N2572	NPN	Ch	300	20	500	200	50*	100			.010	15		
2N2580	NPN	Pwr		400	5A	200	10*	5A	30kc		5ma	400		

JEDEC No.	Type	Use	MAXIMUM RATINGS P_C mw @ 25°C	BV_{CE} BV_{CB}*	I_C ma	T_J °C	ELECTRICAL PARAMETERS MIN. h_{fe}-h_{FE}*	@ I_C ma	MIN. f_{hfb} mc	MIN. G_e db	MAX. I_{CO} (μa)	@ V_{CB}	Closest GE	Dwg. No.
2N2581	NPN	Pwr		400	10A	200	25*	5A	30kc		5ma	400		
2N2582	NPN	Pwr		500	5A	200	10*	5A	30kc		5ma	500		
2N2583	NPN	Pwr		500	10A	200	25*	5A	30kc		5ma	500		
2N2584	NPN	Pwr		600	5A	200	10*	5A	30kc		5ma	600		
2N2585	NPN	Pwr		600	10A	200	25*	5A	30kc		5ma	600		
2N2586	NPN	AF	300	60	30	200	120*	10μa			.002	45	2N930	16
2N2587	PNP	IF	150	30	100	100	15*	8			5	15		
2N2588	PNP	IF	150	40	30	100	50*	1.5		13	3	12		
2N2589	NPN	Pwr		150	7A	200	17*	7A			2ma	150		
2N2590	PNP	Vid	400	100	50	200	40	5			.025	80		
2N2591	PNP	Vid	400	100	50	200	70	5			.025	80		
2N2592	PNP	Vid	400	100	50	200	115	5			.025	80		
2N2593	PNP	Vid	400	100	50	200	160	5			.025	80		
2N2594	NPN	Pwr	1W	80	1A	200	50*	100	40		.1	60	2N699	5
2N2595	PNP	Vid	400	80	50	200	15*	5			.025	50		
2N2596	PNP	Vid	400	80	50	200	30*	5			.025	50		
2N2597	PNP	Vid	400	80	50	200	60*	5			.025	50		
2N2598	PNP	Vid	400	80	50	200	15*	5			.025	80		
2N2599	PNP	Vid	400	80	50	200	30*	5			.025	80		
2N2600	PNP	Vid	400	80	50	200	60*	5			.025	80		
2N2601	PNP	Vid	400	60	50	200	12.5*	1			.025	45		
2N2602	PNP	Vid	400	60	50	200	25*	1			.025	45		
2N2603	PNP	Vid	400	60	50	200	50*	1			.025	45		
2N2604	PNP	Vid	400	60	30	200	40*	10μa			.010	45		
2N2605	PNP	Vid	400	60	30	200	100*	10μa			.010	45		
2N2610	NPN	AF	150	45	25	150	9	1			2	30	2N332	3
2N2611	NPN	Pwr	2W	120	1A	175	12*	200			50	120	2N2611	8
2N2612	PNP	Pwr	75WC	65	15A	100	85*	10A			10ma	30		
2N2613	PNP	AF	120	30	50	100	120	.5			5	12		
2N2614	PNP	AF	120	40	50	100	100	1			5	20		
2N2615	NPN	Osc	300	30		200	20*	3		9	.001	15	2N917	17
2N2616	NPN	Osc	300	30	50	200	20*	3		15	.010	15	2N918	17
2N2617	PNP	AF	250	25	100	150	25	1			.1	6		
2N2618	NPN	Vid	600	60	750	200	25*	10			.1	25	2N696	5
2N2621	PNP		150	15	100	110	15*	1			16	12		
2N2622	PNP		150	24	100	110	15*	1			12	12		
2N2623	PNP		150	32	100	110	20*	1			8	12		
2N2624	PNP		150	15	100	110	15*	1			16	12		
2N2625	PNP		150	24	100	110	15*	1			12	12		
2N2626	PNP		150	32	100	110	20*	1			8	12		
2N2627	PNP		150	15	100	110	15*	1			12	20		
2N2628	PNP		150	24	100	110	15*	1			14	12		

JEDEC No.	Type	Use	MAXIMUM RATINGS P_C mw @ 25°C	BV_{CE} BV_{CB}*	I_C ma	T_J °C	ELECTRICAL PARAMETERS MIN. h_{fe}-h_{FE}*	@ I_C ma	MIN. f_{hfb} mc	MIN. G_e db	MAX. I_{CO} (μa)	@ V_{CB}	Closest GE	Dwg. No.
2N2629	PNP		150	32	100	110	10*	1			10	12		
2N2630	PNP	Sw	300	18	100	100	25*	100			5	15		
2N2631	NPN	RF		80	1.5A	200	8*	200		8.7	.1	30		
2N2632	NPN	Pwr		90	5A	175	40*	1A			.1	60		
2N2633	NPN	Pwr		120	5A	175	40*	1A			.1	60		
2N2634	NPN	Pwr		150	5A	175	40*	1A			.1	60		
2N2635	PNP	Sw	150	30	100	100	45*	50			5	25		
2N2636	PNP	Pwr	100W	100	25A	110	20*	25A			10ma	100		
2N2637	PNP	Pwr	100W	100	25A	110	20*	25A			10ma	100		
2N2638	PNP	Pwr	100W	100	25A	110	20*	25A			10ma	100		
2N2639	NPN	Diff	600	45	30	200	50*	10μa			.010	45		
2N2640	NPN	Diff	600	45	30	200	50*	10μa			.010	45		
2N2642	NPN	Diff	600	45	30	200	100*	10μa			.010	45		
2N2643	NPN	Diff	600	45	30	200	100*	10μa			.010	45		
2N2644														
2N2645	NPN	AF	500	75		200	100*	150			.010	60	2N956	16
2N2646	PN	Si Uni	SEE G. E. SPECIFICATION SECTION										2N2646	29
2N2647	PN	Si Uni	SEE G. E. SPECIFICATION SECTION										2N2647	29
2N2648	PNP	Pwr	5WC	35	1A	100	80*	1A			100	35		
2N2649	NPN		8.7WC	65	1A	200	10*	500			500	65		
2N2650	NPN		8.7WC	140	1A	200	10*	500			500	140		
2N2651	NPN	Sw	1.2WC	40	500	200	25*	10			.030	20		
2N2652	NPN	Diff	600	100	500	200	35*	100μa			.010	50	2N2652	21
2N2654	PNP		100	25	10	75	25*	1.0		20	8.0	10		
2N2655	NPN	Pwr	15WC	100V	500	200	30*	200	4		10	100		
2N2656	NPN	RF	360	25	200	200	40*	.1		10	.5	15	2N918	17
2N2657	NPN	Pwr	1.25W	80	5A	200	40*	1A			.1	60	2N657	5
2N2658	NPN	Pwr	1.25W	100	5A	200	40*	1A			.1	60	2N657	5
2N2659		Pwr		50*		100	30-90*	500	30		20 ma	20		
2N2660	PNP	Pwr	15W	70*	3A	100	30-90*	500	30		20 ma	20		
2N2661	PNP	Pwr	15W	90*	3A	100	30-90*	500	30		20 ma	25		
2N2662	PNP	Pwr	15W	50*	3A	100	30-90*	500	30		20 ma	25		
2N2663	PNP	Pwr	15W	70*	3A	100	30-90*	500	30		20 ma	25		
2N2664	PNP	Pwr	15W	90*	3A	100	30-90*	500	30		20 ma	25		
2N2665	PNP	Pwr	15W	50*	3A	100	50-150*	500	30		20 ma	25		
2N2666	PNP	Pwr	15W	70*	3A	100	50-150*	500	30		20 ma	25		
2N2667	PNP	Pwr	15W	90*	3A	100	50-150*	500	30		20 ma	25		
2N2668	PNP	Pwr	15W	50*	3A	100	50-150*	500	30		20 ma	25		
2N2669	PNP	Pwr	15W	70*	3A	100	50-150*	500	30		20 ma	25		
2N2670	PNP	Pwr	15W	90*	3A	100	50-150*	500	30		20 ma	25		
2N2671	PNP	AF	100	25*	10	75	40	1		12	8	6		
2N2672	PNP	AF	100	25*	10	75	40	1		40	8	6		

JEDEC No.	Type	Use	MAXIMUM RATINGS P_C mw @ 25°C	BV_{CE} BV_{CB}*	I_C ma	T_J °C	ELECTRICAL PARAMETERS MIN. h_{fe}-h_{FE}*	@ I_C ma	MIN. f_{hfb} mc	MIN. G_e db	MAX. I_{CO} (μa)	@ V_{CB}	Closest GE	Dwg. No.
2N2672A	PNP	AF	100	25*	10	75	40	1		40	8	6		
2N2673	NPN	AF	250	60*	25	200	8-22*	1	2.5		.100	30	2N2673	4
2N2674	NPN	AF	250	60*	25	200	12-40*	1	5.0		.100	30	2N2674	4
2N2675	NPN	AF	250	60*	25	200	22-76*	1	10		.100	30	2N2575	4
2N2676	NPN	AF	250	60*	25	200	45-290*	1	10		.100	30	2N2676	4
2N2677	NPN	AF	250	45*	25	200	20-55*	1	10		.100	30	2N2677	4
2N2678	NPN	AF	250	45*	25	200	45-150*	1	20		.100	30	2N2678	4
2N2679	PNPN	Sw	SEE G. E. SPECIFICATION SECTION										3N84	28
2N2680	PNPN	Sw	SEE G. E. SPECIFICATION SECTION										3N81	28
2N2681	PNPN	Sw	SEE G. E. SPECIFICATION SECTION										3N82	28
2N2682	PNPN	Sw												
2N2683	PNPN	Sw	SEE G. E. SPECIFICATION SECTION										3N83	28
2N2684	PNPN	Sw	SEE G. E. SPECIFICATION SECTION										3N81	28
2N2685	PNPN	Sw												
2N2686	PNPN	Sw	SEE G. E. SPECIFICATION SECTION										3N84	28
2N2687	PNPN	Sw	SEE G. E. SPECIFICATION SECTION										3N84	28
2N2688	PNPN	Sw	SEE G. E. SPECIFICATION SECTION										3N81, 3	28
2N2689	PNPN	Sw	SEE G. E. SPECIFICATION SECTION										3N82, 4	28
2N2690	PNPN	Sw												
2N2691	PNP	Pwr	100W	100*	20A	110C	30-100*	20A	6		5 ma	100		
2N2692	NPN	Amp/Sw	300	45*	50	200	90-360*	100μa	45		10 Na	25	2N929	16
2N2693	NPN	Sw	1000	30	50	200	60	100μa			10 Na	25	2N929	16
2N2694	NPN	Sw	1000	20	50	200	30	100μa			10 Na	25	2N929	16
2N2695	PNP	Sw	2W	25	500	200	30-130*	50			25 Na	10		
2N2696	PNP	Sw	1.2W	25	500	200	30-130*	50			25μa	10		
2N2697	NPN	Pwr Sw	10W	60	5A	200	40-120*	1A			.1	60		
2N2698	NPN	Pwr Sw	10W	80	5A	200	40-120*	1A			.1	60		
2N2699	PNP	Sw	150	15*	100	100	40-200	10			3	6		
2N2706	PNP	A	500	32*	200	75	80-290*	2	1.3		10	.5		
2N2708	NPN	HF	200	20		200	30-180*	2	700	15	.01	15	2N918	17
2N2709	PNP	A	240	35	50	200	10-22*	.2	.2		1.0	30		
2N2710	NPN	Sw	360	20	500	200	40*	10			.03	20		
2N2711	NPN	A	200	18	100	125	30-120	2			.5	18	2N2711	1
2N2712	NPN	A	200	18	100	125	80-300	2			.5	18	2N2712	1
2N2713	NPN	A	200	18	200	125	30-120	2			.5	18	2N2713	1
2N2714	NPN	A	200	18	200	125	80-300	2			.5	18	2N2714	1
2N2715	NPN	A	200	18	50	125	30-120	2			.5	18	2N2715	1
2N2716	NPN	A	200	18	50	125	80-300	2			.5	18	2N2716	1
2N2717	PNP	Sw	100	15	30	75	50*	30			1.4	.5		
2N2718	PNP	Sw	240	12	400	100	25*	170	150		7	5		
2N2719	NPN	Sw	300	8	200	175	30*	60	200		100	25	2N914	16
2N2720	NPN	Diff	600	60	40	200	30-120*	.100			.010	60	2N2919	21

JEDEC No.	Type	Use	Pc mw @ 25°C	BV_{CE} BV_{CB}*	Ic ma	T_J °C	MIN. hfe-h_{FE}*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ V_{CB}	Closest GE	Dwg. No.
			MAXIMUM RATINGS				ELECTRICAL PARAMETERS							
2N2721	NPN	Diff	600	60	40	200	30-120*	.100			.010	60	2N2919	21
2N2722	NPN	Diff	600	45	40	200	50-250*	.001			.001	30	2N2916	21
2N2726	NPN	Pwr	1W	200*	500	200	30-90*	200	5		1	100	2N2726	5
2N2727	NPN	Pwr	1W	200*	500	200	75-150*	200	10		1	100	2N2727	5
2N2728	PNP	Pwr	170W	5	50A	110	40-130*	20A						
2N2729	NPN	HF	300	15	50	200	20-200	3	600		.01	15		
2N2730	PNP	Pwr Sw	80W	60	65A	110	30-120*	25A			5 na	80		
2N2731	PNP	Pwr Sw	80W	45	65A	110	30-120*	25A			5 na	60		
2N2732	PNP	Pwr Sw	80W	30	65A	110	30-120*	25A			5 na	40		
2N2733	PNP	Pwr Sw	66	60	65A	110	30-120*	25A			5 na	80		
2N2734	PNP	Pwr Sw	66	45	65A	110	30-120*	25A			5 na	60		
2N2735	PNP	Pwr Sw	66	30	65A	110	30-120*	25A			5 na	40		
2N2736	PNP	Pwr Sw	66	60	65A	110	30-120*	25A			5 na	80		
2N2737	PNP	Pwr Sw	66	45	65A	110	30-120*	25A			5 na	60		
2N2738	PNP	Pwr Sw	66	30	65A	110	30-120*	25A			5 na	40		
2N2739	NPN	Pwr	200W	50	20A	175	10*	10A						
2N2740	NPN	Pwr	200W	100	20A	175		10A						
2N2741	NPN	Pwr	200W	150	20A	175		10A						
2N2742	NPN	Pwr	200W	200	20A	175		10A						
2N2743	NPN	Pwr	200W	250	20A	175		10A						
2N2744	NPN	Pwr	200W	300	20A	175		10A						
2N2745	NPN	Pwr	200W	50	20A	175		15A						
2N2746	NPN	Pwr	200W	100	20A	175		15A						
2N2747	NPN	Pwr	200W	150	20A	175		15A						
2N2748	NPN	Pwr	200W	200	20A	175		15A						
2N2749	NPN	Pwr	200W	250	20A	175		15A						
2N2750	NPN	Pwr	200W	300	20A	175		15A						
2N2751	NPN	Pwr	200W	50	20A	175		20A						
2N2752	NPN	Pwr	200W	100	20A	175		20A						
2N2753	NPN	Pwr	200W	150	20A	175		20A						
2N2754	NPN	Pwr	200W	200	20A	175		20A						
2N2755	NPN	Pwr	200W	250	20A	175		20A						
2N2756	NPN	Pwr	200W	300	20A	175		20A						
2N2757	NPN	Pwr	200W		20A	175	10*							
2N2758	NPN	Pwr	200W		20A	175	10*							
2N2759	NPN	Pwr	200W		20A	175	10*							
2N2760	NPN	Pwr	200W		20A	175	10*							
2N2761	NPN	Pwr	200W		20A	175	10*							
2N2762	NPN	Pwr	200W		20A	175	10*							
2N2763	NPN	Pwr	200W		20A	175	10*							
2N2764	NPN	Pwr	200W		20A	175	10*							
2N2765	NPN	Pwr	200W		20A	175	10*							

JEDEC No.	Type	Use	Pc mw @ 25°C	BV_{CE} BV_{CB}*	Ic ma	T_J °C	MIN. hfe-h_{FE}*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ V_{CB}	Closest GE	Dwg. No.
			MAXIMUM RATINGS				ELECTRICAL PARAMETERS							
2N2766	NPN	Pwr	200W		20A	175	10*							
2N2767	NPN	Pwr	200W		20A	175	10*							
2N2768	NPN	Pwr	200W		20A	175	10*							
2N2769	NPN	Pwr	200W		20A	175	10*							
2N2770	NPN	Pwr	200W		20A	175	10*							
2N2771	NPN	Pwr	200W		20A	175	10*							
2N2772	NPN	Pwr	200W		20A	175	10*							
2N2773	NPN	Pwr	200W		20A	175	10*							
2N2774	NPN	Pwr	200W		20A	175	10*							
2N2775	NPN	Pwr	200W		20A	175	10*							
2N2776	NPN	Pwr	200W		20A	175	10*							
2N2777	NPN	Pwr	200W		20A	175	10*							
2N2778	NPN	Pwr	200W		20A	175	10*							
2N2779	NPN	Pwr	200W		20A	175	10*							
2N2780	NPN	Pwr	200W		20A	175	10*							
2N2780	NPN	Pwr Sw	200W	300*	30A	200S	10*	25A						
2N2781	NPN	VHF/UHF	2.0W	75*	2.0A	175S	7.5*	350		12.5	500	28		
2N2782	NPN	VHF/UHF	2.0W	100*	2.0A	175S	7.5*	350		12.5	500	28		
2N2783	NPN	VHF/UHF	2.0W	100*	2.0A	175S	7.5*	350			10	28		
2N2784	NPN	Lo Pwr	300	15*		200	40*	10			.005	5	2N918	17
2N2785	NPN	DA	500	60*		175	2000*	100			.005	30	2N2785	5
2N2786	PNP	HF	260	35*	150	90S	33*	100		10	10	10		
2N2786A	PNP	HF	260	35*	150	90S	33*	100		10	10	10		
2N2787	NPN	Sw	800	75*	800	175	12*	1.0			.01	50	2N2195	5
2N2788	NPN	Sw	800	75*	800	175	20*	0.1			.01	50	2N2195	5
2N2789	NPN	Sw	800	75*	800	175	35*	0.1			.01	50	2N2192	5
2N2790	NPN	Sw	500	75*	800	175	12*	1.0			.01	50	2N760	16
2N2791	NPN	Sw	500	75*	800	175	20*	0.1			.01	50	2N760	16
2N2792	NPN	Sw	500	75*	800	175	35*	0.1			.01	50	2N760	16
2N2793	PNP	Pwr Amp	170W	75*	60A	110	12*	50A	2kc					
2N2794	P-FET	A	300			200S								
2N2795	PNP	Sw	75	25*	100	100S	50*	10			25	25		
2N2796	PNP	Sw	75	20*	100	100S	30*	10			25	20		
2N2797	PNP	Sw	75	40*	100	100S	50*	10			25	40		
2N2798	PNP	Sw	75	60*	100	100S	30*	10			25	60		
2N2799	PNP	Sw	75	30*	100	100S	30*	10			25	30		
2N2800	PNP	Sw	800	50*	800	300S	20*	0.1			10	50		
2N2801	PNP	Sw	800	50*	800	300S	30*	0.1			10	50		
2N2802	PNP	Diff	250	25*	30	200S	15*	.01			.01	25		
2N2803	PNP	Diff	250	25*	30	200S	15*	.01			.01	25		
2N2804	PNP	Diff	250	25*	30	200S	15*	.01			.01	25		
2N2805	PNP	Diff	250	25*	30	200S	30*	.01			.01	25		

JEDEC No.	Type	Use	MAXIMUM RATINGS Pc mw @ 25°C	BVCE BVCB*	Ic ma	TJ °C	ELECTRICAL PARAMETERS MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE	Dwg. No.
2N2806	PNP	Diff	250	25*	30	200S	30*	.01			.01	25		
2N2807	PNP	Diff	250	25*	30	200S	30*	.01			.01	25		
2N2808	NPN	VHF/UHF	200	30*	25	200	20*	2.0		20	.01	15		
2N2808A	NPN	VHF/UHF	200	30*	25	200	20*	2.0		22	.01	15		
2N2809	NPN	VHF/UHF	200	30*	25	200	20*	2.0		17	.01	15		
2N2809A	NPN	VHF/UHF	200	30*	25	200	20*	2.0		20	.01	15		
2N2810	NPN	VHF/UHF	200	30*	25	200	20*	2.0		17	.01	15		
2N2810A	NPN	VHF/UHF	200	30*	25	200	20*	2.0		20	.01	15		
2N2811	NPN	Pwr	40W	80*	10A	200	10*	10			0.1	60	2N1724	14
2N2812	NPN	Pwr	40W	80*	10A	200	10*	10			0.1	60	2N1724	14
2N2813	NPN	Pwr	40W	120*	10A	200	10*	10			0.1	60	2N1724	14
2N2814	NPN	Pwr	40W	120*	10A	200	10*	10			0.1	60	2N1724	14
2N2815	NPN	Sw	200W	80*	20A	200S	10*	10A						
2N2816	NPN	Sw	200W	100*	20A	200S	10*	10A						
2N2817	NPN	Sw	200W	150*	20A	200S	10*	10A						
2N2818	NPN	Sw	200W	200*	20A	200S	10*	10A						
2N2819	NPN	Sw	200W	80*	25A	200S	10*	15A						
2N2820	NPN	Sw	200W	100*	25A	200S	10*	15A						
2N2821	NPN	Sw	200W	150*	25A	200S	10*	15A						
2N2822	NPN	Sw	200W	200*	25A	200S	10*	15A						
2N2823	NPN	Sw	200W	80*	30A	200S	10*	20A						
2N2824	NPN	Sw	200W	100*	30A	200S	10*	20A						
2N2825	NPN	Sw	200W	150*	30A	200S	10*	20A						
2N2826	PNP	A	7.5W	15	1.0A	110S	75*	100	4					
2N2827	PNP	A	7.5W	30	1.0A	110S	75*	100	4					
2N2828	NPN	Sw	40W	80*	3.0A	200S	20*	500					2N1724	14
2N2829	NPN	Sw	40W	80*	3.0A	200S	20*	1.0					2N1724	14
2N2831	NPN	Vid	360	40*	200	200	25*	10			.03	15	2N760	16
2N2832	PNP	Sw		80*	20A	110S	25*	10A			10 ma	80		
2N2833	PNP	Sw		120*	20A	110S	25*	10A			10 ma	120		
2N2834	PNP	Sw		140*	20A	110S	25*	10A			10 ma	140		
2N2835	PNP	Pwr	16W	32*	1.0A	90S	30*	1.0A	0.3		25	0.5		
2N2836	PNP	Pwr	37.5W	55*	3.5A	100S	30*	1.0A	0.250		50	0.5		
2N2837	PNP	Sw	500	50*	800	300S	20*	0.1						
2N2838	PNP	Sw	500	50*	800	300S	30*	0.1			10	50		
2N2840		Si Uni	SEE G. E. SPECIFICATION SECTION										2N2840	29
2N2845	NPN	Sw	360	60*		200	10*	500				30	2N956	16
2N2846	NPN	Sw	800	60*		200	10*	500				30	2N1711	1
2N2847	NPN	Sw	360	60*		200	40*	150				30	2N718	16
2N2848	NPN	Sw	800	60*		200	40*	150				30	2N697	5

JEDEC No.	Type	Use	MAXIMUM RATINGS Pc mw @ 25°C	BVCE BVCB*	Ic ma	TJ °C	ELECTRICAL PARAMETERS MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE	Dwg. No.
2N2849	NPN	Sw	850	100*	3A	200S	100*	1A						
2N2850	NPN	Sw	850	100*	3A	200S	40*	1A					2N2192A	5
2N2851	NPN	Sw	850	100*	3A	200S	40*	1A					2N2192A	5
2N2852	NPN	Sw	850	100*	3A	200S	20*	1A					2N2243A	
2N2853	NPN	Sw	850	60*	3A	200S	40*	1A					2N2193A	5
2N2854	NPN	Sw	850	60*	3A	200S	100*	1A					2N2192A	5
2N2855	NPN	Sw	850	60*	3A	200S	40*	1A					2N2192A	5
2N2856	NPN	Sw	850	60	3A	200S	20*	1A					2N2193A	5
2N2857	NPN	HF	200	30*	20	200S	20	2		12	.01	15	2N918	17
2N2858	NPN	Sw	8.75W	100*	3A	200S	20	1A						
2N2859	NPN	Sw	8.75W	120*	3A	200S	20	1A						
2N2860	PNP	Sw	150	18*	150	100	40	40			6.0	12		
2N2861	PNP		300	25*	100	200	50	1.0			.01			
2N2862	PNP		300	25*	100	200	25	1.0			.01			
2N2863	NPN		800	60*	1A	200	30*	200			0.5		2N2193	5
2N2864	NPN		800	60*	1A	200	20*	200			0.5		2N2193	5
2N2865	NPN		200	25*	50	200	20	4.0			.01		2N918	17
2N2866	NPN	Pwr	20W	120*	3A	200S	15*	2.0A					2N3220	15
2N2867	NPN	Pwr	20W	120*	3A	200S	30*	2.0A					2N3221	15
2N2868	NPN	Sw	800	60*	1A	200	40*	150			.01	30		
2N2869	PNP	Pwr	30W	−60*	10A	100S	30*	5A						
2N2870	PNP	Pwr	30W	−80*	10A	100S	30*	5A						
2N2871	PNP	Ch	400	60*		200S	15*	1.0	0.5		0.1	−50		
2N2872	PNP	Ch	400	110*		200S	15*	1.0	0.5		0.1	−90		
2N2873	PNP	VHF	115	35*	10	100S	40*	1.0	3.7		−12	−12		
2N2874	NPN	UHF	2W	75*	2A	175S	7.5*	350		10	10	28	2N656	5
2N2875	PNP	Pwr	20W	60*	2A	200S	15*	50	25		−1.0	−30		
2N2876	NPN	VHF	17.5W	80*	2.5A	200S	5*	2.5A		7	0.1	30		
2N2877	NPN	Pwr	30W	80*	5A	200	15*	10			0.1	60	2N3221	15
2N2878	NPN	Pwr	30W	80*	5A	200	30*	10			0.1	60	2N3221	15
2N2879	NPN	Pwr	30W	100*	5A	200	15*	10			0.1	60	2N3221	15
2N2880	NPN	Pwr	30W	100*	5A	200	30*	10			0.1	60	2N3221	15
2N2881	PNP	Pwr	8.75W	60*	1.5A	200S	20*	500	25kc		100	30		
2N2882	PNP	Pwr	8.75W	100*	1.5A	200S	20*	500	25kc		100	50		
2N2883	NPN	UHF	800	40*	300	200	20*	100			0.5	20	2N697	5
2N2884	NPN	UHF	800	40*	300	200	20*	100			0.5	20	2N697	5
2N2885	NPN	Sw	150	40*	50	175	30*	10			0.025	20		
2N2886	NPN	A	800	50*	500	200	22*	5.0			0.1	30	2N699	5
2N2887	NPN	VHF	25W	100*	1.2A	200S	6	350						
2N2888	PNPN	Sw	SEE G. E. SILICON CONTROLLED RECTIFIER MANUAL										2N2888	
2N2889	PNPN	Sw	SEE G. E. SILICON CONTROLLED RECTIFIER MANUAL										2N2889	
2N2890	NPN	Pwr	800	100*		200	50*	1.0A						

JEDEC No.	Type	Use	MAXIMUM RATINGS Pc mw @ 25°C	BVCE BVCB*	Ic ma	TJ °C	ELECTRICAL PARAMETERS MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE	Dwg. No.
2N2891	NPN	Pwr	800	100*		200	30*	1.0A						
2N2892	NPN	Pwr	30W	100*	5.0A	200	50*	1.0A					2N3221	15
2N2893	NPN	Pwr	30W	100*	5.0A	200	30*	1.0A					2N3221	15
2N2894	PNP	Sw	360	−12*	200	200	40*	30			10	6		
2N2895	NPN		500	120*	1.0A	200S	10*	.01			.002	60		
2N2896	NPN		500	140*	1.0A	200S	35*	1.0			.01	60		
2N2897	NPN		500	60*	1.0A	200S	35*	1.0			.05	60		
2N2898	NPN		500	120*	1.0A	200S	10*	.01			.002	60	2N2364	4
2N2899	NPN		500	140*	1.0A	200S	35*	1.0			.01	60	2N2364	4
2N2900	NPN	Ampl	1.8WC	60*	1000	200	50	150			.05	60	2N2353	4
2N2901	NPN	Ch	.36WC	20*	20	200	12	10			.025	15	2N2356	32
2N2902	NPN	Ampl	240WC	120*	750	200	30	50				120	7F4	12
2N2903	NPN	Diff	1.2WC	60*	50	200	60	10μa			10 na	50		
2N2904	PNP	Sw	3W	60*	600	200	40	150			20 na	50		
2N2905	PNP	Sw	3W	60*	600	200	75	150			20 na	50		
2N2906	PNP	Sw	600	60*	600	200	40	150			20 na	50		
2N2907	PNP	Sw	600	60*	600	200	75	150			20 na	50		
2N2908	NPN	Ampl	78W	80*	2000	200	12	1000				45		
2N2909	NPN	Ampl	400	60*	1000	200	30	150			10 na	30		
2N2910	NPN	Diff	2W	45*		200	70	.1			10 na	20	2N2910	21
2N2911	NPN	Sw	5W	150*	3000	200	20	1000				150		
2N2912	PNP	Pwr	75W	15*	25A	110	100	5A				15		
2N2913	NPN	Diff	1.5W	45*	30	200	60	10μa			10 na	45	2N2913	21
2N2914	NPN	Diff	1.5W	45*	30	200	150	10μa			10 na	45	2N2914	21
2N2915	NPN	Diff	1.5W	45*	30	200	60	10μa			10 na	45	2N2915	21
2N2916	NPN	Diff	1.5W	45*	30	200	150	10μa			10 na	45	2N2916	21
2N2917	NPN	Diff	1.5W	45*	30	200	60	10μa			10 na	45	2N2917	21
2N2918	NPN	Diff	1.5W	60*	30	200	150	10μa			10 na	45	2N2918	21
2N2919	NPN	Diff	1.5W	60*	30	200	60	10μa			2 na	45	2N2919	21
2N2920	NPN	Diff	1.5W	60*	30	200	150	10μa			2 na	45	2N2920	21
2N2921	NPN	A	200	25*	100	125	35	2			.5	25	2N2921	1
2N2922	NPN	A	200	25*	100	125	55	2			.5	25	2N2922	1
2N2923	NPN	A	200	25*	100	125	90	2			.5	25	2N2923	1
2N2924	NPN	A	200	25*	100	125	150	2			.5	25	2N2924	1
2N2925	NPN	A	200	25*	100	125	235	2			.5	25	2N2925	1
2N2926	NPN	A	200	25*	100	125	35	2			.5	25	2N2926	1
2N2927	PNP	Sw	3W	25*	500	200	30	50			25 na	10		
2N2928	PNP	UHF	150	15*	100	100	10	2			5	10		
2N2929	PNP	IF/RF	750	25*	100	100	10	10			5	10		
2N2930	PNP	Sw	250	30*	500	100	60	10			7	15		
2N2931	NPN	A	37.5	5*	50	125	30	.2			15 na	2	11B552	18

JEDEC No.	Type	Use	MAXIMUM RATINGS Pc mw @ 25°C	BVCE BVCB*	Ic ma	TJ °C	ELECTRICAL PARAMETERS MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE	Dwg. No.
2N2932	NPN	A	37.5	5*	50	125	70	.2			15 na	2	11B555	18
2N2933	NPN	A	37.5	5*	50	125	45	.2			15 na	2	11B555	18
2N2934	NPN	A	37.5	45*	50	125	30	.2			15 na	30	11B552	18
2N2935	NPN	A	37.5	45*	50	125	70	.2			15 na	30	11B555	18
2N2936	NPN	Diff	600	60*		175	100	10μa			10 na	60	2N2916	21
2N2937	NPN	Diff	600	60*		175	100	10μa			10 na	60	2N2914	21
2N2938	NPN	Sw	300	25*	500	200	10	1			25 na	20		
2N2939	NPN	Ampl	800	75*	1000	200	60	150		10	25 na	60	2N2193	5
2N2940	NPN	Ampl	800	120*	1000	200	60	150		10	25 na	90		
2N2941	NPN	Ampl	800	150*	1000	200	60	150		10	25 na	100		
2N2942	PNP	Sw	150	50*	100	100	50	10			2	25		
2N2943	PNP	Sw	150	30*	100	100	30	10			3	15		
2N2944	PNP	Ch	400	15*	100	200	80	1			.1 na	15		
2N2945	PNP	Ch	400	25*	100	200	40	1 ma			.2 na	25		
2N2946	PNP	Ch	400	40*	100	200	30	1 ma			.5 na	40		
2N2947	NPN	Ampl	25W	60	1.5A	175	2.5	1000			1	50		
2N2948	NPN	Ampl	25W	40	1.5A	175	2.5	1000			1	30		
2N2949	NPN	Ampl	6W	60	700	175	5	400			.1	50		
2N2950	NPN	Ampl	6W	60	700	175	5	400			.1	50		
2N2951	NPN	Ampl	3W	60	250	175	20	150			.1	50	2N2193	5
2N2952	NPN	Ampl	1.8W	60	250	175	20	150			.1	50		
2N2953	PNP	A	100	30	150	100	100	50			5	20		
2N2954	NPN	Ampl	200	30*	500	200	25	2		15	50 na	10	2N918	17
2N2955	PNP	Sw	150	40	100	100	20	10			10	25		
2N2956	PNP	Sw	150	40	100	100	30	10			10	25		
2N2957	PNP	Sw	150	40	100	100	60	10			10	25		
2N2958	NPN	Sw	3W	60*	600	200	40	150			25 na	50	2N2193	5
2N2959	NPN	Sw	3W	60*	600	200	100	150			25 na	50	2N2192	5
2N2960	NPN	Sw	3W	60*	600	200	75	10			25 na	50	2N2192	5
2N2961	NPN	Sw	3W	60*	600	200	30	500			25 na	50	2N2192	5
2N2962	PNP	Ampl	3W	40*	300	100				6	5	10		
2N2963	PNP	Ampl	3W	40*	300	100				5	5	10		
2N2964	PNP	Ampl	3W	30*	300	100				6	5	10		
2N2965	PNP	Ampl	3W	30*	300	100				5	5	10		
2N2966	PNP	Ampl	60	20*	100	100	8	3			5	10		
2N2967	NPN	Sw	300	12*		200	20	10			50 na	5		
2N2968	PNP	Ch	150	30*	50	140	15	.1			10 na	15		
2N2968	PNP	Ch	150	30*	50	140	15	.1			10 na	15		
2N2970	PNP	Ch	150	30*	50	140	10	.1			10 na	15		
2N2971	PNP	Ch	150	30*	50	140	10	.1			10 na	15		
2N2972	NPN	Diff	750	45*	30	200	60	10μa			10 na	45		
2N2973	NPN	Diff	750	45*	30	200	150	10μa			10 na	45		

JEDEC No.	Type	Use	MAXIMUM RATINGS: Pc mw @ 25°C	BVCE BVCB*	Ic ma	TJ °C	ELECTRICAL PARAMETERS: MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE	Dwg. No.
2N2974	NPN	Diff	750	45*	30	200	60	10μa			10 na	45		
2N2975	NPN	Diff	750	45*	30	200	150	10μa			10 na	45		
2N2976	NPN	Diff	750	45*	30	200	60	10μa			10 na	45		
2N2977	NPN	Diff	750	45*	30	200	150	10μa			10 na	45		
2N2978	NPN	Diff	750	60*	30	200	60	10μa			2 na	45		
2N2979	NPN	Diff	750	60*	30	200	150	10μa			2 na	45		
2N2980	NPN	Diff	750	100*	500	200	50	10 ma			2 na	80		
2N2981	NPN	Diff	750	100*	500	200	50	10 ma			10 na	80		
2N2982	NPN	Diff	750	100*	500	200	50	10 ma			10 na	80		
2N2983	NPN	Ampl	1W	155*	3000	200	20	1000				150		
2N2984	NPN	Ampl	1W	185*	3000	200	20	1000				180		
2N2985	NPN	Ampl	1W	155*	3000	200	40	1000				150		
2N2986	NPN	Ampl	1W	185*	3000	200	40	1000				180		
2N2987	NPN	Ampl	15W	95*	1000	200	25	200				90	2N2203	13
2N2988	NPN	Ampl	1.5W	155*	1000	200	25	200				90	2N2203	13
2N2989	NPN	Ampl	1.5W	95*	1000	200	60	200				150		
2N2990	NPN	Ampl	1.5W	155*	1000	200	60	200				150		
2N2991	NPN	Ampl	15000	95*	1000	200	20	500			ICEO .10μa	50	7F1	12
2N2992	NPN	Ampl	15000	155*	1000	200	20	500			ICEO .10μa	90	7F3	12
2N2993	NPN	Ampl	15000	95*	1000	200	40	500			ICEO .10μa	50	7F2	12
2N2994	NPN	Ampl	15000	155*	1000	200	40	500			ICEO .10μa	90	7F4	12
2N2995	NPN	Ampl	15000	120*	1000	175	10	1000			50μa	120	2N2995	13
2N2996	PNP	Ampl	75FA	15*	50	100	25	4			5μa	10		
2N2997	PNP	Ampl	75FA	30*	50	100	40	4			5μa	12		
2N2998	PNP	Ampl	75FA	15*	20	100	15	3			5μa	10		
2N2999	PNP	Ampl	75FA	15*	20	100	10	3			5μa	10		
2N3001	PNPN	Sw				SEE G. E. SPECIFICATION SECTION							3N84	28
2N3002	PNPN	Sw				SEE G. E. SPECIFICATION SECTION							3N83	28
2N3003	PNPN	Sw				SEE G. E. SPECIFICATION SECTION							3N82	28
2N3004	PNPN	Sw				SEE G. E. SPECIFICATION SECTION								
2N3005	PNPN	Sw				SEE G. E. SPECIFICATION SECTION							3N84	28
2N3006	PNPN	Sw				SEE G. E. SPECIFICATION SECTION							3N83	28
2N3007	PNPN	Sw				SEE G. E. SPECIFICATION SECTION							3N82	28
2N3008	PNPN	Sw				SEE G. E. SPECIFICATION SECTION								
2N3009	NPN	Sw	1200	40*	200	200	30	30				20		
2N3010	NPN	Sw	300	15*	50	200	15	30				11		
2N3011	NPN	Sw	1200	30*	200	200	30	10				20	2N2369	16
2N3012	PNP	Sw	1200	12*	200	200	30	30				6		

JEDEC No.	Type	Use	MAXIMUM RATINGS: Pc mw @ 25°C	BVCE BVCB*	Ic ma	TJ °C	ELECTRICAL PARAMETERS: MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE	Dwg. No.
2N3013	NPN	Sw	1200	40*	200	200	30	30				20		
2N3014	NPN	Sw	1200	40*	200	200	30	30				20		
2N3015	NPN	Sw	3000	60*		200	30	150				30	2N2193	5
2N3016	NPN	Ampl	5000	100*	500	150	60	1000			.1	60		
2N3017	NPN	Ampl	10000	100*	1000	150	60	1000			.1	60		
2N3018	NPN	Ampl	5000	100*	2000	150	60	1000			.1	60		
2N3019	NPN	Ampl	5000	140*	1000	200	100	150			10 na	90	2N2192	5
2N3020	NPN	IF/RF	5W	80	1A	200	30	1			10 na	90		
2N3021	NPN	Sw	25W	30	3A	175	20	1A						
2N3022	NPN	Sw	25W	45	3A	175	20	1A						
2N3023	NPN	Sw	25W	60	3A	175	20	1A						
2N3024	NPN	Sw	25W	30	3A	175	50	1A						
2N3025	NPN	Sw	25W	45	3A	175	50	1A						
2N3026	NPN	Sw	25W	60	3A	175	50	1A						
2N3033	NPN	Sw	300	160*	200	200					5			
2N3034	NPN	Sw	300	120*	200	200					5			
2N3035	NPN	Sw	300	90	200	200					5	BVCBO less 15V		
2N3036	NPN	AF	5W	80	1200	200	50*	150			10 na	60		
2N3037	NPN	AF	360	70	500	200	40*	150			10 na	60		
2N3038	NPN	AF	360	60	500	200	80*	150			10 na	60		
2N3039	PNP	AF	360	35	500	200	20*	150			25 na	30		
2N3040	PNP	AF	360	30	500	200	40*	150			25 na	30		
2N3043	NPN	Diff	350	45	30	200	130*	1			10 na	45		
2N3044	NPN	Diff	350	45	30	200	130*	1			10 na	45		
2N3045	NPN	AF	350	45	30	200	130*	1			10 na	45		
2N3046	NPN	Diff	350	45	30	200	65*	1			10 na	45		
2N3047	NPN	Diff	350	45	30	200	65*	1			10 na	45		
2N3048	NPN	AF	350	45	30	200	65*	1			10 na	45		
2N3049	PNP	Diff	350	20	100	200	30*	1			10 na	25		
2N3050	PNP	Diff	350	20	100	200	30*	1			10 na	25		
2N3051	PNP	AF	350	20	100	200	30*	1			10 na	25		
2N3052	NPN	Sw	350	15	200	200	25*	10			25 na	20		
2N3053	NPN	AF	5W	40	700	200	50*	150			.25	60		
2N3054	NPN	AF	25W	90*	4A	200	25*	500						
2N3055	NPN	AF	115W	100*	15A	200	20*	4A						
2N3056	NPN	RF	5W	60	1A	200	40*	150			10 na	60	2N2364	4
2N3057	NPN	RF	5W	60	1A	200	100*	150			10 na	60		
2N3058	PNP	AF	400	6	100	200	40*	.1μa			.1 na	6		
2N3059	PNP	AF	400	10	100	200	100*	10μa			.1 na	6		
2N3060	PNP	AF	400	60	100	200	30*	1			5 na	60		
2N3061	PNP	AF	400	60	100	200	60*	1			5 na	60		

JEDEC No.	Type	Use	MAXIMUM RATINGS P_C mw @ 25°C	BV_{CE} BV_{CB}*	I_C ma	T_J °C	ELECTRICAL PARAMETERS MIN. h_{fe}-h_{FE}*	@ I_C ma	MIN. f_{hfb} mc	MIN. Ge db	MAX. I_{CO} (μa)	@ V_{CB}	Closest GE	Dwg. No.
2N3062	PNP	AF	400	80	100	200	20*	1			10 na	80		
2N3063	PNP	AF	400	80	100	200	50*	1			10 na	80		
2N3064	PNP	AF	400	100	100	200	15*	1			100 na	100		
2N3065	PNP	AF	400	100	100	200	30*	1			100 na	100		
2N3072	PNP	Sw	3W	60	500	200	30*	50						
2N3073	PNP	Sw	1.2W	60	500	200	30*	50						
2N3076	NPN	Sw	125W	50	10A	200	30*	7A						
2N3077	NPN	AF	360	60	50	200	200*	1			10 na	45		
2N3078	NPN	AF	360	60	50	200	150*	1			10 na	45		
2N3079	NPN	Sw	150W	200	5A	200	7*	5A						
2N3080	NPN	Sw	150W	300	5A	200	7*	5A						
2N3081	PNP	Sw	2W	50	600	300	30*	150						
2N3082	NPN	Ch	1.8W	7	100	200	100*	250μa					2N3082	33
2N3083	NPN	Ch	1.8W	7	100	200	100*	250μa					2N3083	33
2N3108	NPN	Sw	5W	60	1A	200	25*	500			10 na	60		
2N3110	NPN	Sw	5W	40	1A	200	25*	500			10 na	60		
2N3114	NPN	IF	5W	150	200	200	30*	30			10 na	100		
2N3117	NPN	AF	1.2W	60	50	20	400*	1			10 na	45		
2N3118	NPN	RF	1W	60	500	200	50*	25			.1	30		
2N3119	NPN	IF	1W	80	500	200	50*	100			50 na	60		
2N3120	PNP	IF	3W	45	500	200	30*	50			10 na	30		
2N3121	PNP	IF	1.2W	45	500	200	30*	50			10 na	30		
2N3122	NPN	AF	3W	30	500	200	25*	300			2	30	7A31	5
2N3123	NPN	Sw	3W	30	800	175	100*	150			100 na	50		
2N3124	PNP	AF	90W	40*	15A	100	60*	3A			20 ma	40		
2N3125	PNP	AF	90W	80*	3.3A	100	30*	3A			15 ma	80		
2N3126	PNP	AF	90W	100*	15A	100	25*	1A			3 ma	65		
2N3127	PNP	IF/RF	100	20	50	100	20	3	400	17	5	10		
2N3128	NPN	IF	150	20	100	150	70*	1			10 na	16		
2N3129	NPN	IF	150	45	100	150	150*	1			10 na	36		
2N3130	NPN	IF	150	60	100	150	100*	1			10 na	48		
2N3131	NPN	Sw	150	15	100	150	30*	10			25 na	20		
2N3133	PNP	Sw	3W	35	600	300	40*	150			50 na	30		
2N3134	PNP	Sw	3W	35	600	300	100*	150			50 na	30		
2N3135	PNP	Sw	1.8W	35	600	300	40*	150			50 na	30		
2N3136	PNP	Sw	1.8W	35	600	300	100*	150			50 na	30		
2N3137	NPN	RF	1W	20	150	200	20*	50			50 na	20		
2N3138	NPN	RF	20W	65	2A	200	10*	1A			500	60		
2N3139	NPN	RF	20W	140	2A	200	10*	1A			500	140		
2N3140	NPN	AF	20W	65*	2A		10*	1A			500	65		
2N3141	NPN	AF	20W	140*	2A		10*	1A			500	140		
2N3142	NPN	AF	25W	65*	2A		10*	1A			500	65		

JEDEC No.	Type	Use	MAXIMUM RATINGS P_C mw @ 25°C	BV_{CE} BV_{CB}*	I_C ma	T_J °C	ELECTRICAL PARAMETERS MIN. h_{fe}-h_{FE}*	@ I_C ma	MIN. f_{hfb} mc	MIN. Ge db	MAX. I_{CO} (μa)	@ V_{CB}	Closest GE	Dwg. No.
2N3143	NPN	AF	25W	140*	2A		10*	1A			500	140		
2N3144	NPN	AF	25W	65*	2A		10*	1A			500	65		
2N3145	NPN	AF	25W	140*	2A		10*	1A			500	140		
2N3146	PNP	Pwr	150W	150*	15A		25*	−10A			−10 ma	−150		
2N3147	PNP	Pwr	150W	180*	15A		25*	−10A			−10 ma	−180		
2N3148	PNP	Sw		11*	50		60*	−50			5	−5		
2N2149	NPN	Sw			70A		10*	50A						
2N3150	NPN	Sw			70A		10*	50A						
2N3151	NPN	Sw			70A		10*	50A						
2N3152	NPN	Sw		120*	100		40*	30			50 @ 100°C	20		
2N3153	NPN	Sw		15	100	200					10 na	15	2N760	16
2N3154	PNP	Sw	37.5W		3A		60*	0.5A			100	2		
2N3155	PNP	Sw	37.5W		3A		60*	0.5A			100	2		
2N3156	PNP	Sw	37.5W		3A		60*	0.5A			100	2		
2N3157	PNP	Sw	37.5W		3A		60*	0.5A			100	2		
2N3158	PNP	Sw	37.5W		3A		30*	0.5A			100	2		
2N3159	PNP	Sw	37.5W		3A		30*	0.5A			100	2		
2N3160	PNP	Sw	37.5W		3A		30*	0.5A			100	2		
2N3161	PNP	Sw	37.5W		3A		30*	0.5A			100	2		
2N3162	NPN	Diff	1.5W	45*		200	15*	100μa			10 na	30	2N2915	21
2N3163	PNP	Pwr	85W		−3A		12*	−1A						
2N3164	PNP	Pwr	85W		−3A		12*	−1A						
2N3165	PNP	Pwr	85W		−3A		12*	−1A						
2N3166	PNP	Pwr	85W		−3A		12*	−1A						
2N3167	PNP	Pwr	86W		−3A		12*	−1A						
2N3168	PNP	Pwr	85W		−3A		12*	−1A						
2N3169	PNP	Pwr	85W		−3A		12*	−1A						
2N3170	PNP	AF	85W		−3A		12*	−1A						
2N3171	PNP	AF	75W		−3A		12*	−1A						
2N3172	PNP	AF	75W		−3A		12*	−1A						
2N3173	PNP	AF	75W		−3A		12*	−1A						
2N3174	PNP	AF	75W		−3A		12*	−1A						
2N3175	PNP	AF	85W		−5A		10*	−2A						
2N3176	PNP	AF	85W		−5A		10*	−2A						
2N3177	PNP	AF	85W		−5A		10*	−2A						
2N3178	PNP	AF	85W		−5A		10*	−2A						
2N3179	PNP	AF	85W		−5A		10*	−2A						
2N3180	PNP	AF	85W		−5A		10*	−2A						
2N3181	PNP	AF	85W		−5A		10*	−2A						
2N3182	PNP	AF	85W		−5A		10*	−2A						
2N3183	PNP	AF	75W		−5A		10*	−2A						

JEDEC No.	Type	Use	MAXIMUM RATINGS: Pc mw @ 25°C	BVCE BVCB*	Ic ma	TJ °C	ELECTRICAL PARAMETERS: MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE	Dwg. No.
2N3184	PNP	AF	75W		−5A		10*	−2A						
2N3185	PNP	AF	75W		−5A		10*	−2A						
2N3186	PNP	AF	75W		−5A		10*	−2A						
2N3187	PNP	AF	85W		−5A		10*	−3A						
2N3188	PNP	AF	85W		−5A		10*	−3A						
2N3189	PNP	AF	85W		−5A		10*	−3A						
2N3190	PNP	AF	85W		−5A		10*	−3A						
2N3191	PNP	AF	85W		−5A		10*	−3A						
2N3192	PNP	AF	85W		−5A		10*	−3A						
2N3193	PNP	AF	85W		−5A		10*	−3A						
2N3194	PNP	AF	85W		−5A		10*	−3A						
2N3195	PNP	AF	75W		−5A		10*	−3A						
2N3196	PNP	AF	75W		−5A		10*	−3A						
2N3197	PNP	AF	75W		−5A		10*	−3A						
2N3198	PNP	AF	75W		−5A		10*	−3A						
2N3199	PNP	AF	40W		−3A		20*	−1A						
2N3200	PNP	AF	40W		−3A		20*	−1A						
2N3201	PNP	AF	40W		−3A		20*	−1A						
2N3202	PNP	AF	8.75W		−3A		20*	−1A						
2N3203	PNP	AF	8.75W		−3A		20*	−1A						
2N3204	PNP	AF	8.75W		−3A		20*	−1A						
2N3205	PNP	AF	40W		−2A		20*	−500						
2N3206	PNP	AF	40W		−2A		20*	−500						
2N3207	PNP	AF	40W		−2A		20*	−500						
2N3208	PNP	AF	8.75W		−2A		20*	−500						
2N3209	PNP	Sw	1.2W	−20*	200	200	15*	100						
2N3210	NPN	Sw	1.2W	40*	500	200	30*	10			10 na	20	2N708	16
2N3211	NPN	Sw	1.2W	40*	500	200	10*	500						
2N3212	PNP	Sw	12.1W		5A		30*	−5A 3A						
2N3213	PNP	Sw	12.1W		5A		30*	−5A 3A						
2N3214	PNP	Sw	12.1W		5A		30*	−5A 3A						
2N3215	PNP	Sw	12.1W		5A		25*	−5A 3A						
2N3217	PNP	Sw			100						.001	15		
2N3218	PNP	Sw			100						.001	25		
2N3219	PNP	Sw			100						.001	40		
2N3220	NPN	AF			2A		20*	1A					2N3220	15
2N3221	NPN	AF			2A		40*	1A					2N3221	15
2N3222	NPN	AF			2A		20*	1A					2N3222	15

JEDEC No.	Type	Use	MAXIMUM RATINGS: Pc mw @ 25°C	BVCE BVCB*	Ic ma	TJ °C	ELECTRICAL PARAMETERS: MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE	Dwg. No.
2N3223	NPN	AF			2A		40*	1A					2N3223	15
2N3224	PNP	Vid					20*	−50			−0.1	−80		
2N3225	PNP	Vid		−100*			40*	−50			−0.1	−80		
2N3227	NPN	Sw	1.2W	40*	200	200	100*	10			0.4	20		
2N3228	PNPN	Sw			3.2A									
2N3229	NPN	AF	17.5W	105*	2.5A		5*	2.5A		8.75	0.1	30		
2N3230	NPN	Sw	25W	80*	7A	200	1000	50			2	50		
2N3231	NPN	Sw	25W	100*	7A	200	1000	50			2	60		
2N3244	PNP	Sw	5W	40*	1A	200	25*	750			50 na	30		
2N3245	PNP	Sw	5W	50*	1A	200	20*	1.A			50 na	50		
2N3246	NPN	AF	.35W	60*	50		300*	100μa			.001	40	2N930A	16
2N3247	NPN	AF	.15W	60*	50		150*	1.0μa			.001	40		
2N3254	PNPN	Sw				SEE G. E. SPECIFICATION SECTION							3N84	28
2N3255	PNPN	Sw				SEE G. E. SPECIFICATION SECTION							3N84	28
2N3256	PNPN	Sw				SEE G. E. SPECIFICATION SECTION							3N81, 3N83	28
2N3257	PNPN	Sw				SEE G. E. SPECIFICATION SECTION							3N84	28
2N3258	PNPN	Sw				SEE G. E. SPECIFICATION SECTION							3N84	28
2N3259	PNPN	Sw				SEE G. E. SPECIFICATION SECTION							3N81, 3N83	28
2N3262	NPN	Pwr	8.75W	80	1.5A	200S	40*	50					2N1068	7
2N3263	NPN	Pwr		60	25A	200	20*	15A						
2N3264	NPN	Pwr		90	25A	200	20*	15A						
2N3265	NPN	Pwr		60	25A	200	20*	15A						
2N3266	NPN	Pwr		90	25A	200	20*	15A						
2N3267	PNP	RF/IF	75	−8	20	100S	15	−3						
2N3268	NPN	AF	150	45	25	200S	12	10	2.5					
2N3273	PNPN	Sw				SEE G. E. SPECIFICATION SECTION							3N82, 3N85	28
2N3305	PNP	AF	600	−40		200S	40*	−.1			−.05	−30		
2N3306	PNP	AF	600	−40		200S	100*	−.1			−.05	−40		
2N3307	NPN	RF/IF	300	35	50	200	20*	2.0		17	.01	15	2N918	17
2N3308	NPN	RF/IF	300	25	50	200	10*	2.0		17	.01	15	2N917	17
2N3309	NPN	Pwr	3.5W	50*	500	175	5*	30			0.5	25	7A30	5
2N3311	PNP	Pwr	170W	20	500	110	60*	3A			5na	30		
2N3312	PNP	Pwr	170W	30	500	110	60*	3A			5ma	45		
2N3313	PNP	Pwr	170W	40	500	110	60*	3A			5ma	60		
2N3314	PNP	Pwr	170W	20	500	110	100*	3A			5ma	30		
2N3315	PNP	Pwr	170W	30	500	110	100*	3A			5ma	45		
2N3316	PNP	Pwr	170W	40	500	110	100*	3A			5ma	60		
2N3323	PNP	Pwr	150	35*	100	100	30	3			10	10		

JEDEC No.	Type	Use	MAXIMUM RATINGS Pc mw @ 25°C	BVCE BVCB*	Ic ma	TJ °C	ELECTRICAL PARAMETERS MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE	Dwg. No.
2N3324	PNP	Pwr	150	35*	100	100	30	3			10	10		
2N3325	PNP	Pwr	150	35*	100	100	30*	3			10	10		
2N3347	PNP	Diff	600	−45		200	40*	−.010			−.010	−45		
2N3348	PNP	Diff	600	−45		200	40*	−.010			−.010	−45		
2N3349	PNP	Diff	600	−45		200	40*	−.010			−.010	−45		
2N3350	PNP	Diff	600	−45		200	100*	−.010			−.010	−45		
2N3351	PNP	Diff	600	−45		200	100*	−.010			−.010	−45		
2N3352	PNP	Diff	600	−45		200	100*	−.010			−.010	−45		
2N3371	PNP	RF/F	150	−10	100	125S	25	−12			−7	−6		
2N3372	NPN	Obsolete	200	18	100	100	250*	2			.1	18	2N3391	1
2N3373	NPN	Obsolete	200	18	100	100	250*	2			.1	18	2N3391A	1
2N3390	NPN	AF	200	25	100	100	400*	2			0.1	18	2N3390	1
2N3391	NPN	AF	200	25	100	100	250*	2			0.1	25	2N3391	1
2N3391A	NPN	AF	200	25	100	100	250*	2			0.1	25	2N3391A	1
2N3392	NPN	AF	200	25	100	100	150*	2			0.1	25	2N3392	1
2N3393	NPN	AF	200	25	100	100	90*	2			0.1	25	2N3393	1
2N3394	NPN	AF	200	25	100	100	55*	2			0.1	25	2N3394	1
2N3395	NPN	AF	200	25	100	100	150*	2			0.1	18	2N3395	1
2N3396	NPN	AF	200	25	100	100	90*	2			0.1	18	2N3396	1
2N3397	NPN	AF	200	25	100	100	55*	2			0.1	18	2N3397	1
2N3398	NPN	AF	200	25	100	100	55*	2			0.1	18	2N3398	1
2N3399	PNP	RF								8.2				
2N3401	PNP	Ch	250	25	100	150	4				0.1	20		
2N3402	NPN	AF	560	25	500	150	75	2			0.1	25	2N3402	2
2N3403	NPN	AF	560	25	500	150	100	2			0.1	25	2N3403	2
2N3404	NPN	AF	560	25	500	150	75	2			0.1	25	2N3404	2
2N3405	NPN	AF	560	25	500	150	100	2			0.1	25	2N3405	2
							14*	10						
2N3413	PNP	AF	400	150	200	200	10*	50		8	0.1	100		
2N3414	NPN	AF	360	25	500	150	75	2			0.1	25	2N3414	1
2N3415	NPN	AF	360	25	500	150	100	2			0.1	25	2N3415	1
2N3416	NPN	AF	360	25	500	150	75	2			0.1	25	2N3416	1
2N3417	NPN	AF	360	25	500	150	100	2			0.1	25	2N3417	1
							20*	100						
2N3418	NPN	Pwr Sw	800	60	3A	175	10*	5A				80		
							20*	100						
2N3419	NPN	Pwr Sw	800	80	3A	175	10*	5A				120		
							40*	100						
2N3420	NPN	Pwr Sw	800	60	3A	175	15*	5A				80		
							40*	100						
2N3421	NPN	Pwr Sw	800	80	3A	175	15*	5A				120		
2N3449	PNP	Sw	150	6	100	100	20*	10			3	5		

JEDEC No.	Type	Use	MAXIMUM RATINGS Pc mw @ 25°C	BVCE BVCB*	Ic ma	TJ °C	ELECTRICAL PARAMETERS MIN. hfe-hFE*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ VCB	Closest GE	Dwg. No.
4D20	NPN	Sw	150	40*	25	150J	33*			1.0			4D20	3
4D21	NPN	Sw	150	40*	25	150J	88*			1.0			4D21	3
4D22	NPN	Sw	150	40*	25	150J	185*			1.0			4D22	3
4D24	NPN	Sw	125	15*	25	125J	33*			1.0			4D24	3
4D25	NPN	Sw	125	15*	25	125J	88*			1.0			4D25	3
4D26	NPN	Sw	125	15*	25	125J	133*			1.0			4D26	3
4C28	NPN	Sw	150	40*	25	125J	15		12.0	2.0			4C28	3
4C29	NPN	Sw	150	40*	25	125J	30		12.0	2.0			4C29	3
4C30	NPN	Sw	150	40*	25	125J	55		12.0	2.0			4C30	3
4C31	NPN	Sw	150	40*	25	125J	115		12.0	2.0			4C31	3
7B1	NPN	Power	15W	80*		175	12*		15T		50	80	7B1	8
7C1	NPN	Power	15W	80*		175	12*		15T		50	80	7C1	9
7D1	NPN	Power	15W	80*		175	12*		15T		50	80	7D1	10
7E1	NPN	Power	15W	80*		175	12*		15T		50	80	7E1	11
7F1	NPN	Power	7W	80*		175	12*		15T		50	80	7F1	12
7B2	NPN	Power	15W	80*		175	30*		15T		50	80	7B2	8
7C2	NPN	Power	15W	80*		175	30*		15T		50	80	7C2	9
7D2	NPN	Power	15W	80*		175	30*		15T		50	80	7D2	10
7E2	NPN	Power	15W	80*		175	30*		15T		50	80	7E2	11
7F2	NPN	Power	7W	80*		175	30*		15T		50	80	7F2	12
7B3	NPN	Power	15W	120*		175	12*		15T		50	120	7B3	8
7C3	NPN	Power	15W	120*		175	12*		15T		50	120	7C3	9
7D3	NPN	Power	15W	120*		175	12*		15T		50	120	7D3	10
7E3	NPN	Power	15W	120*		175	12*		15T		50	120	7E3	11
7F3	NPN	Power	7W	120*		175	12*		15T		50	120	7F3	12

ABBREVIATIONS

A–Audio
AF–Audio Frequency Amplifier and General Purpose
AF Out–High Current AF Output
AF Sw–Low Frequency Switch
Ampl–Amplifier
AS–Audio Signal
C–Case Temperature ≦25°C
Ch–Chopper
DA–Darlington Amplifier
Diff–Differential Amplifier
GD–Grown Diffused
HF–High Frequency Amplifier
IF–Intermediate Frequency Amplifier
Inv–Inverter
J–Operating Junction Temperature
LoIF–Low IF (262 Kc) Amplifier
LoPA–Low Power Audio
LoPO–Low Power Output
MF–Medium Frequency Amplifier
Mxr–Mixer
NPN-A–NPN Alloyed
NPN-D–NPN Diffused
NPN-EM–NPN Epitaxial Mesa
NPN-FA–NPN Fused Alloy
NPN-G–NPN Grown
NPN-GD–NPN Grown Diffused
NPN-M–NPN Mesa
NPN-PL–NPN Planar
NPN-PEP–NPN Planar Epitaxial Passivated
NPN-PM–NPN Planar Epitaxial Mesa
Osc–High Gain High Frequency RF Oscillator
PNP-A–PNP Alloyed
PNP-D–PNP Diffused
PNP-EM–PNP Epitaxial Mesa
PNP-M–PNP Mesa
PNP-MD–PNP Micro-Alloyed Diffused
Pt–Point Contact Types
Pwr–Power Output 1 Watt or More
Pwr Sw–Power Switch
RF–Radio Frequency Amplifier
S–Storage Temperature
Si–Silicon High Temp. Transistors (all others germanium)
Sw–High Current, High Frequency Switch
T–Typical Values
UHF–Ultra High Frequency Amplifier
UNI–Unijunction Transistor
VHF–Very High Frequency Amplifier
Vid–Video Amplifier
W–Watts

NOTE: *Closest GE types* are given only as a general guide and are based on available published electrical specifications. However, General Electric Company makes no representation as to the accuracy and completeness of such information. Since manufacturing techniques are not identical, the General Electric Company makes no claim, nor does it warrant, that its transistors are exact equivalents or replacements for the types referred to.

APPLICATION LITERATURE— SALES OFFICES

CHAPTER 20

APPLICATION NOTES AND ARTICLE REPRINTS

(Available Upon Request From Semiconductor Products Department, Advertising & Sales Promotion, Building 7, Electronics Park, Syracuse, New York)

PUBLICATION NO.	TITLE
90.2	Transistorized Flashers
90.3	Efficient High Quality Program Amplifier Circuits Using The Industrial Silicon Series 2N2107, 2N2108, and 2N2196
90.5	Silicon Transistor Chopper For High Impedance Sources
90.6	Use of Complementary Transistors in Switching Circuits
90.7	Silicon Transistor Chopper for Low Impedance Sources
90.8	A High Performance Portable Broadcast Receiver Using Silicon Planar Passivated Transistors
90.9	The Use of Charge Control Parameters
90.10	Notes on the Application of the Silicon Unijunction Transistor
90.12	Unijunction Temperature Compensation
90.13	Some Large Signal Properties of Planar and Planar Epitaxial Transistors
90.14	Tape Erase and Bias Oscillator
90.15	An Integrated Reference Amplifier For Precision Power Supplies
90.16	Silicon Controlled Switches
90.17	Understanding Snap Diodes
90.20	A Precision Current Supply Using the Reference Amplifier
90.21	How to Suppress Rate Effect in PNPN Devices
	General Consideration of Tunnel Diode Amplifiers
	Tunnel Diodes as Amplifiers and Switches
90.33	Tunnel Diode Sinewave Oscillators
90.34	A Survey of UHF and Microwave Tunnel Diode Applications
90.36	Predicting Reverse Recovery Time of High Speed Semiconductor Junction Diodes
90.41	Article: Designing with Tunnel Diodes
90.42	Tunnel Diode UHF-TV Tuner
90.43	A Tunnel Diode R.F. Radiation Detector
90.44	Practical Tunnel Diode Converter Circuit Considerations
90.45	On the Subject of Tunnel Diode Sinewave Oscillators
90.46	Tunnel Diode Remote Control Transmitter
90.47	The Logarithmic and Temperature Coefficient Characteristics of the 1N3605-1N3606 Diodes
90.48	Tunnel Diodes — A Four Part Series
90.80	Microelectronics Using General Electric Emitter-coupled Logic Operators

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Room 253, 121 Broadway St.
Area Code: 714
234-0329

San Francisco 94304
(Palo Alto)
701 Welch Road
Area Code: 415
DAvenport 1-6771

COLORADO
Denver 80201
201 University Blvd.
P.O. Box 2331
Area Code: 303
DUdley 8-5771

CONNECTICUT
Bridgeport 06602
1285 Boston Ave.
Bldg. 21—ES
Area Code: 203
EDison 4-1012

DISTRICT OF COLUMBIA
Washington 20005
777-14th St., N.W.
Area Code: 202
EXecutive 3-3600

FLORIDA
Orlando 32806
14 W. Gore St.
Area Code: 305
425-8634

ILLINOIS
Chicago 60641
3800 N. Milwaukee Ave.
Area Code :312
SPring 7-1600

INDIANA
Indianapolis 46200
3750 N. Meridian St.
Area Code: 317
WAlnut 3-7221

KENTUCKY
Owensboro 42301
316 E. 9th St.
Area Code: 502
683-2401

MASSACHUSETTS
Boston (Newtonville) 02160
701 Washington St.
Area Code: 617
DEcatur 2-7120

MICHIGAN
Detroit (Southfield) 48076
17220 W. Eight Mile Rd.
Area Code: 313
ELgin 6-1075

MINNESOTA
Minneapolis
7710 Computer Ave., Rm. 104
Area Code: 612
927-5456

NEW JERSEY
Clifton (New York City) 07014
200 Main Ave.
Area Code: 201
GRegory 2-8100
(Dial direct from New York City WIsconsin 7-4065)

NEW YORK
Buffalo 14211
1495 Fillmore Ave.
Area Code: 716
TX 2-8000 Ext. 205

Syosset, L. I., N. Y. 11791
175 Jericho Turnpike
Area Code: 516
WAlnut 1-8840

New York City
(Clifton, N. J. 07014)
200 Main Ave.
Area Code: 201
GRegory 2-8100
(Dial direct from New York City WIsconsin 7-4065)

Schenectady 12305
Building 267
Area Code: 518
FRanklin 4-2211
Ext. 52339

Syracuse 13201
Bldg. 7, Electronics Park
Area Code: 315
456-2062

OHIO
Cleveland 44121
211 S. Green Road
Area Code: 216
382-5650
Dayton 45402
118 W. First St.
Area Code: 513
223-7151

PENNSYLVANIA
Philadelphia
(Bala Cynwyd) 19004
1 Belmont Ave., Room 1103
Area Code: 215
TEnnyson 9-6075

TEXAS
Dallas 75205
4447 N. Central Expressway
Area Code: 214
LA 6-0426

VIRGINIA
Lynchburg
P.O. Box 4217
(Carroll Ave. Plant)
Area Code: 703
VI 6-7311

WASHINGTON
Seattle 98108
220 S. Dawson St.
Area Code: 206
PArkway 5-6800

DIRECT GOVERNMENT SALES OFFICES

ALABAMA
Huntsville 35801
3322 Memorial Parkway
South, Suite 13
Area Code: 205
881-1640

CALIFORNIA
Los Angeles 90064
11840 W. Olympic Blvd.
Area Code: 213
GRanite 9-7763
BRadshaw 2-8566

DISTRICT OF COLUMBIA
Washington 20005
777-14th St., N.W.
Area Code: 202
EXecutive 3-3600

NEW JERSEY
Red Bank 07701
43 W. Front St.
Area Code: 201
741-8484

NEW YORK
Syracuse, N. Y. 13201
Bldg. 7, Electronics Park
Area Code: 315
456-3063

OHIO
Dayton 45402
118 W. First St.
Area Code: 513
223-7151

OUTSIDE THE CONTINENTAL UNITED STATES (EXCLUDING HAWAII and ALASKA)
Electronic Component Sales
IGE Export Div.
159 Madison Ave.
New York, N. Y. 10016
Area Code: 212
PLaza 1-1311

IN CANADA
Canadian General Electric Co.
189 Dufferin St.
Toronto, Ontario, Canada
Area Code: 416
534-6311

AUTHORIZED FULL-LINE GENERAL ELECTRIC SEMICONDUCTOR DISTRIBUTORS

ALABAMA
Electronic Wholesalers, Inc.
2310 Bob Wallace Ave., S.W.
Huntsville, 534-2461

ARKANSAS
Carlton-Bates Co.
1210 E. 6th St.
Little Rock

ARIZONA
Kierulff Electronics, Inc.
917 North Seventh Street
Phoenix, AL 8-6121

CALIFORNIA
Brill Electronics
610 East Tenth Street
Oakland, TE 4-5888

Elmar Electronics
140 Eleventh Street
Oakland, TE 4-3311

Fortune Electronics
2280 Palou Avenue
San Francisco 24, VA 6-8811

Hollywood Radio & Electronics, Inc.
5250 Hollywood Boulevard
Hollywood 27, 466-3181

Kierulff Electronics, Inc.
2585 Commerceway
Los Angeles 22, (213) OV 5-5511

Kierulff Electronics, Inc.
2484 Middlefield Road
Mountain View, 968-6292

Radio Products Sales
1501 South Hill Street
Los Angeles 15, RI 8-1271

Santa Monica-Bell Electronic Corp.
306 E. Alondra Blvd.
Gardena, FA 1-5802

Western Radio & TV Supply
1415 India Street
San Diego, BE 9-0361

R. V. Weatherford Co.
6921 San Fernando Road
Glendale 1, VI 9-3451

COLORADO
L. B. Walker Radio Co.
300 Bryant Street
Denver 19, WEst 5-2401

Newark-Denver Electronic Supply Corp.
2170 South Grape Street
Denver, SK 7-3351

CONNECTICUT
Arrow Electronics
225 Main Street
Norwalk, VI 7-2423

Cramer Electronics, Inc.
60 Connolly Parkway
Hamden 14, 288-3581

Hatry of Hartford
100 High Street
Hartford 3, 527-1881

DELAWARE
Almo Industrial Electronics
112 French Street
Wilmington, OL 6-9467

DISTRICT OF COLUMBIA
Silberne Industrial Sales Corp.
3400 Georgia Avenue, N.W.
TU 2-5000

FLORIDA
Electronic Wholesalers
1301 Hibiscus Boulevard
Melbourne, PA 3-1441

Hammond Electronics
911 West Central Blvd.
Orlando, 241-6601

GEORGIA
Jackson Electronic Supply Co., Inc.
1135 Chattahoochee Ave., N.W.
Atlanta, 355-2223

ILLINOIS
Allied Electronics
100 North Western Avenue
Chicago, TA 9-9100

Electronic Distributors, Inc.
4900 North Elston Avenue
Chicago, AV 3-4800

Melvin Electronics, Inc.
541 Madison Street
Oak Park, ES 8-7741

Newark Electronics Corp.
223 West Madison Street
Chicago 6, ST 2-2944

INDIANA
Brown Electronics, Inc.
1032 Broadway
Fort Wayne, 742-7331

Graham Electronics, Inc.
122 South Senate Avenue
Indianapolis, ME 4-8486

IOWA
Deeco, Inc.
618 First Street, N.W.
Cedar Rapids, EM 5-7551

KANSAS
Interstate Electronics Supply Corp.
230 Ida Street
Wichita, AM 4-6318

KENTUCKY
P. I. Burks Co.
659 South Ninth Street
Louisville, 583-2871

LOUISIANA
Crescent Electronic Supply
537 South Clairborne Avenue
New Orleans, JA 2-8726

Radio Parts Company
1112 Magazine St.
New Orleans, 522-0217

MARYLAND

Almo Industrial Electronics
317 Park Heights Avenue
Salisbury, PI 2-1393

Kann-Ellert Electronics, Inc.
2050 Rockrose Avenue
Baltimore, TU 9-4242

Wholesale Radio Parts
308 W. Redwood Street
Baltimore, MU 5-2134

MASSACHUSETTS

Cramer Electronics, Inc.
320 Needham Street
Newton Upper Falls, WO 9-7700

T. F. Cushing, Inc.
1026 Bay Street
P. O. Box 2049
Springfield 1, 788-7341

Durrell Electronics, Inc.
922 Main Street
Waltham, 893-7020

Gerber Radio Supply Co., Inc.
1900 Columbus Avenue
Boston, GA 7-0411

Lafayette Industrial Electronics Corp.
1400 Worcester Street
Natick, 969-6100

MICHIGAN

Electronic Supply Corp.
P.O. Box 430
Battle Creek, Michigan
Enterprise 6379 **(For Most Michigan Areas)**

Radio Specialties Co.
12775 Lyndon Avenue
Detroit 27, BR 2-4212

MINNESOTA

Admiral Distributors, Inc.
5333 Cedar Lake Road
Minneapolis, LI 5-8811

Gopher Electronics Co.
2520 W. Larpenteur Ave.
St. Paul 13, 645-0241

Lew Bonn Company
1211 LaSalle Avenue
Minneapolis, 339-9461

MISSISSIPPI

Ellington Radio, Inc.
824 S. Gallatin Street
Jackson, FL 3-7877

MISSOURI

Electronic Components for Industry
2605 South Hanley Road
St. Louis, MI 7-5505

ECI Semiconductors, Inc.
3265 Gillham Road
Kansas City, WE 1-0829

Radio Lab, Inc.
1612 Grand Avenue
Kansas City, HA 1-0171

NEBRASKA

Radio Equipment Co.
625 North 18th Street
Omaha, 341-7700

Scott Electronics, Inc.
2201 "O" Street
Lincoln, 432-6558

NEW JERSEY

Almo Industrial Electronics
1133 Haddon Avenue
Camden, EM 5-4524

Atlas Electronics, Inc.
774 Pfeiffer Boulevard
Perth Amboy, HI 2-8000

Eastern Radio Corp.
312 Clifton Avenue
Clifton, GR 1-6600

Federated Purchaser, Inc.
155 U.S. Highway 22
Springfield, DR 6-8900

General Radio Supply Co., Inc.
600 Penn Street
Camden 2, WO 4-8560

NEW MEXICO

Kierulff Electronics, Inc.
6323 Acoma Road, S.E.
Albuquerque, AM 8-3901

Midland Specialty Co.
1712 Lomas Blvd., N.E.
Albuquerque, (505) 247-2486

NEW YORK

Arrow Electronics, Inc.
900 Broadhollow Road., Route 110
Farmingdale, L. I., MY 4-6800

Atlas-New York, Inc.
1460 Old Country Road
Plainview, MY 4-6969

Eastern Semiconductor Sales, Inc.
Pickard Building
East Molloy Road
Syracuse, (315) 454-9247

Harvey Radio Co., Inc.
103 West 43rd Street
New York 36, (212) JU 2-1500

Milo Electronics Corp.
530 Canal Street
New York, BE 3-2980

Peerless Radio Distributors, Inc.
19 Wilbur Street
Lynbrook, L. I., LY 3-2121

Rochester Radio Supply Company
140 West Main Street
Rochester, LO 2-9900

Stack Electronics, Inc.
45 Washington Street
Binghamton, RA 3-6326

Standard Electronics, Inc.
1501 Main Street
Buffalo, TT 3-5000

Terminal Hudson Electronics, Inc.
236 West 17th Street
New York, CH 3-5200

Valley Industrial Electronics, Inc.
Truck Route 5A
Yorkville, RE 6-3393

NORTH CAROLINA

Electronic Wholesalers, Inc.
938 Burke Street
Winston-Salem, 725-8711

Southeastern Radio Supply Co., Inc.
414 Hillsboro Street
Raleigh, 828-2311

OHIO

Buckeye Electronic Distributors, Inc.
242 East Long Street
Columbus, CA 8-3265

Hughes-Peters, Inc.
1128 Sycamore Street
Cincinnati, (513) 381-7625

Hughes-Peters, Inc.
481 East 11th Avenue
Columbus, AX 4-5351

Newark-Herrlinger Electronics Co.
112 East Liberty Street
Cincinnati, GA 1-5282

Pioneer-Standard Electronics, Inc.
5403 Prospect Avenue
Cleveland, 432-0010

Srepco Electronics, Inc.
314 Leo Street
Dayton, BA 4-3871

Warren Radio Co.
1002 Adams Street
Toledo, CH 8-3364

OKLAHOMA

Oil Capitol Electronics Corp.
708 South Sheridan Street
Tulsa, TE 6-2511

Radio, Inc.
1000 South Main Street
Tulsa, LU 7-9124

Trice Wholesale Electronics
800 North Hudson Street
Oklahoma City, JA 4-4411

PENNSYLVANIA

Almo Industrial Electronics, Inc.
412 North 6th Street
Philadelphia, WA 2-5918

Atlas Electronics, Inc.
125 Titus Avenue
Warrington, DI 3-1860

Radio Parts Co.
6401 Penn Avenue
Pittsburgh 6, 361-4600

Wholesale Radio Parts
1650 Whiteford Road
York, 755-2891

RHODE ISLAND

W. H. Edwards Co.
116 Hartford Avenue
Providence, 421-6158

SOUTH CAROLINA

Dixie Radio Supply Co., Inc.
1900 Barnwell Street
Columbia, 253-5333

Wholesale Radio Supply Co., Inc.
515 Bay Street
Charleston, 723-3626

TENNESSEE

Bondurant Brothers Co.
906 Sevier Avenue
Knoxville, 523-9144

Curle Radio Supply Co.
439 Broad Street
Chattanooga, 266-4729

Electra Distributing Co.
1914 West End Avenue
Nashville, AL 5-8444

Radio Electric Supply Co.
961 East Sullivan Street
Kingsport, CI 5-6106

TEXAS

Lenert Co.
1420 Hutchinson
Houston, CA 4-2663

McNicol, Inc.
811 North Estrella Street
El Paso, LO 6-2936

Sterling Electronics
1616 McKinney Street
Houston, CA 5-1321

Wholesale Electronic Supply
2809 Ross Avenue
Dallas, TA 4-3001

UTAH

S. R. Ross, Inc.
1212 South State Street
Salt Lake City, DA 8-0591

VIRGINIA

Meridian Electronics, Inc.
1001 West Broad Street
Richmond, 353-6648

Peoples Radio & TV Supply Co.
1015 Moorman Road
Roanoke, 342-8933

Virginia Radio Supply Co.
715 Henry Avenue
Charlottesville, 296-4184

WASHINGTON

C&G Electronics Co.
2600 2nd Avenue
Seattle, MA 4-4354

WEST VIRGINIA

Mountain Electronics
708 Bigley Avenue
Charleston, (304) 344-3411

WISCONSIN

Electronic Expeditors, Inc.
3501 Burleigh
Milwaukee, UP 1-3000

Marsh Radio Supply Co.
6047 West Beloit Road
West Allis, EV 3-2590

Radio Parts Co.
1314 North 7th Street
Milwaukee, BR 6-4160

OTHER GENERAL ELECTRIC PRODUCT DEPARTMENTS

Product	Department
Cadmium Sulfide Cells Control Elements Magnetic Reed Switches Tubes	G. E. Receiving Tube Department Owensboro, Kentucky
Capacitors	G. E. Capacitor Department Hudson Falls, New York
Silicon Controlled Rectifiers Rectifiers Zener Diodes	G. E. Rectifier Components Department Auburn, New York
Lamps	G. E. Lamp Department Nela Park, Cleveland, Ohio
Meters	G. E. Meter Department Somersworth, New Hampshire
Motors	G. E. Specialty Motor Department Fort Wayne, Indiana
Relays	G. E. Specialty Control Department Waynesboro, Virginia
Silicone Potting Compounds Silicone Grease	G. E. Silicone Products Department Waterford, New York
Thermistors	G. E. Metallurgical Products Department Edmore, Michigan
Transformers	G. E. Specialty Transformer Department Fort Wayne, Indiana
Wire & Cable	G. E. Wire and Cable Department Bridgeport, Connecticut

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